

Freescale Semiconductor



COMEXPRESS CARRIER

Page	Contents
1	Cover Page
2	General Information
3	System Block Diagram #1
4	System Block Diagram #2
5	Block Diagram Power_Clock
6	Block Diagram Reset_Debug
7	PCB Stackup
8	Power Entry, Chassis I/O
9	Standby (Hot) Power/2.5v
10	RESET_PLD_PART1
11	RESET_PLD_PART2
12	FPGA, pt. 1
13	FPGA, pt. 2
14	FPGA, pt. 3
15	FPGA, pt. 4
16	1588 SMAs and headers
17	PHY and IEEE 1588 Clocks
18	Configuration Switches
19	CAN Interface #1
20	CAN Interface #2
21	SERDES REF Clocks
22	SATA CONNECTOR
23	PHY RMI Interface
24	GIGe Connectors Part 1
25	GIGe Connectors Part 2
26	Management Bus Muxing
27	SSI CODEC INTERFACE
28	NORFlash, NANDFlash, PromJet
29	Serial Ports_Part1
30	Serial Ports_Part2
31	SDMedia, SPI Devices
32	I2C_Expander
33	USB Connector #1
34	USB Connector #2
35	USB Power Switch
36	IXXAT Interface
37	DVI_Interface
38	LCD Connector_A
39	LCD Connector_B
40	COMe_CONNECTOR SERDES

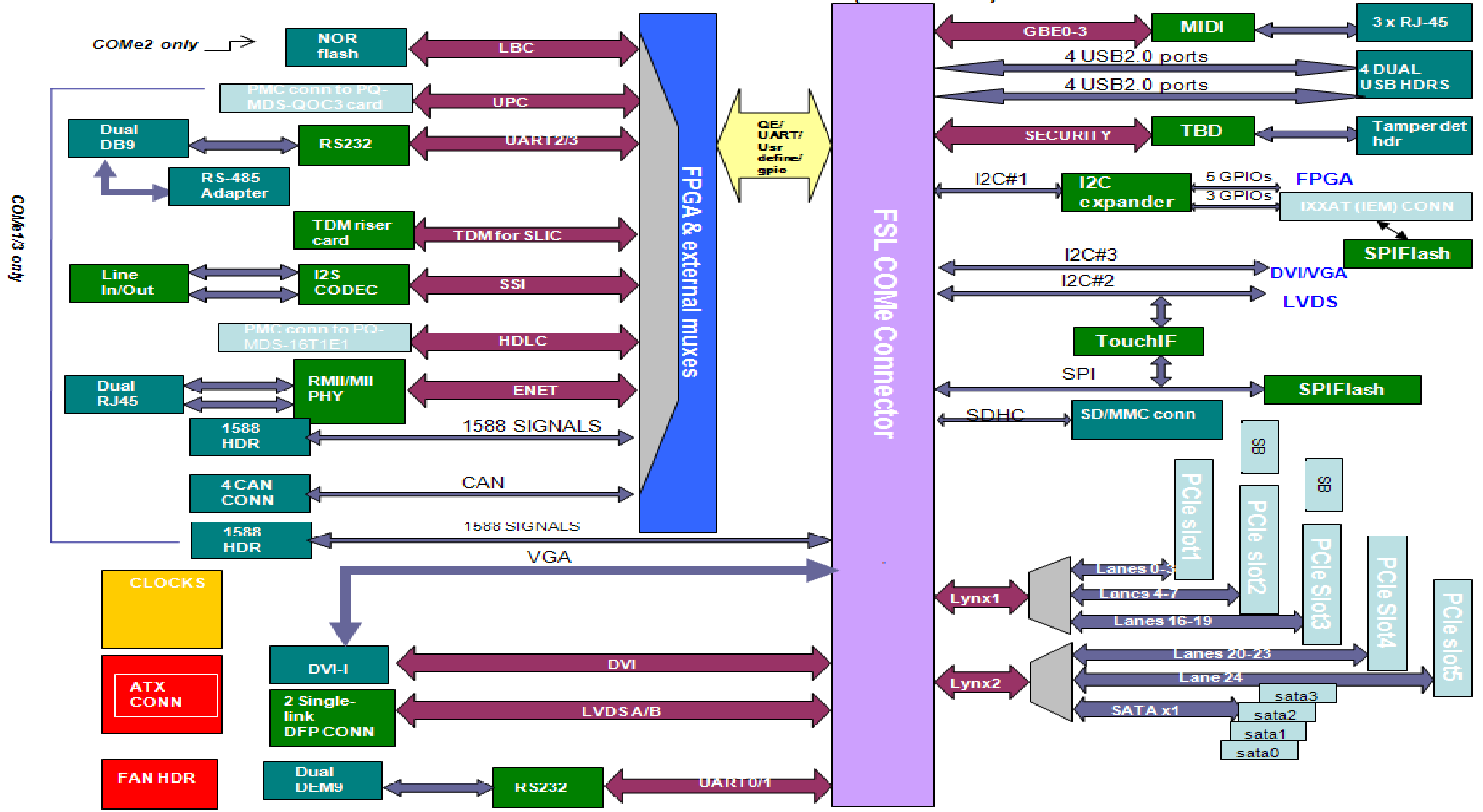
Page	Contents
41	PEX/SRIO x4 Slot #1
42	PEX/SGMII/SRIO x4 Slot #2
43	Slot #2 Sideband Connector
44	PEX/SGMII/XAUI x4 Slot #3
45	Slot #3 Sideband Connector
46	PEX x4 Slot #4
47	PEX x1 Slot #5
48	Tamper Detect
49	LEDs / Debug
50	Global Bypass Caps / Mech
51	MUX/DEMUX_PART1
52	MUX/DEMUX_PART2
53	MUX/DEMUX_PART3
54	MUX/DEMUX_PART4
55	IO_EXPANDER_PRESENT DETECT
56	PMC1_Connector_UTOPIA1
57	PMC1_Connector_UTOPIA2
58	PMC0_Connector_TDM1
59	PMC0_Connector_TDM2
60	TDM_RISER_CARD_CONNECTOR
61	COMe Connector_Part 1
62	COMe Connector_Part 2
63	COMe Connector_Part 3

Version Rev	DATE	Change
A	5/28/2010	FIRST PROTOTYPE
B	10/13/2010	RESPIN FOR PROTOTYPE B PER ECN
XXX	NA	XXX

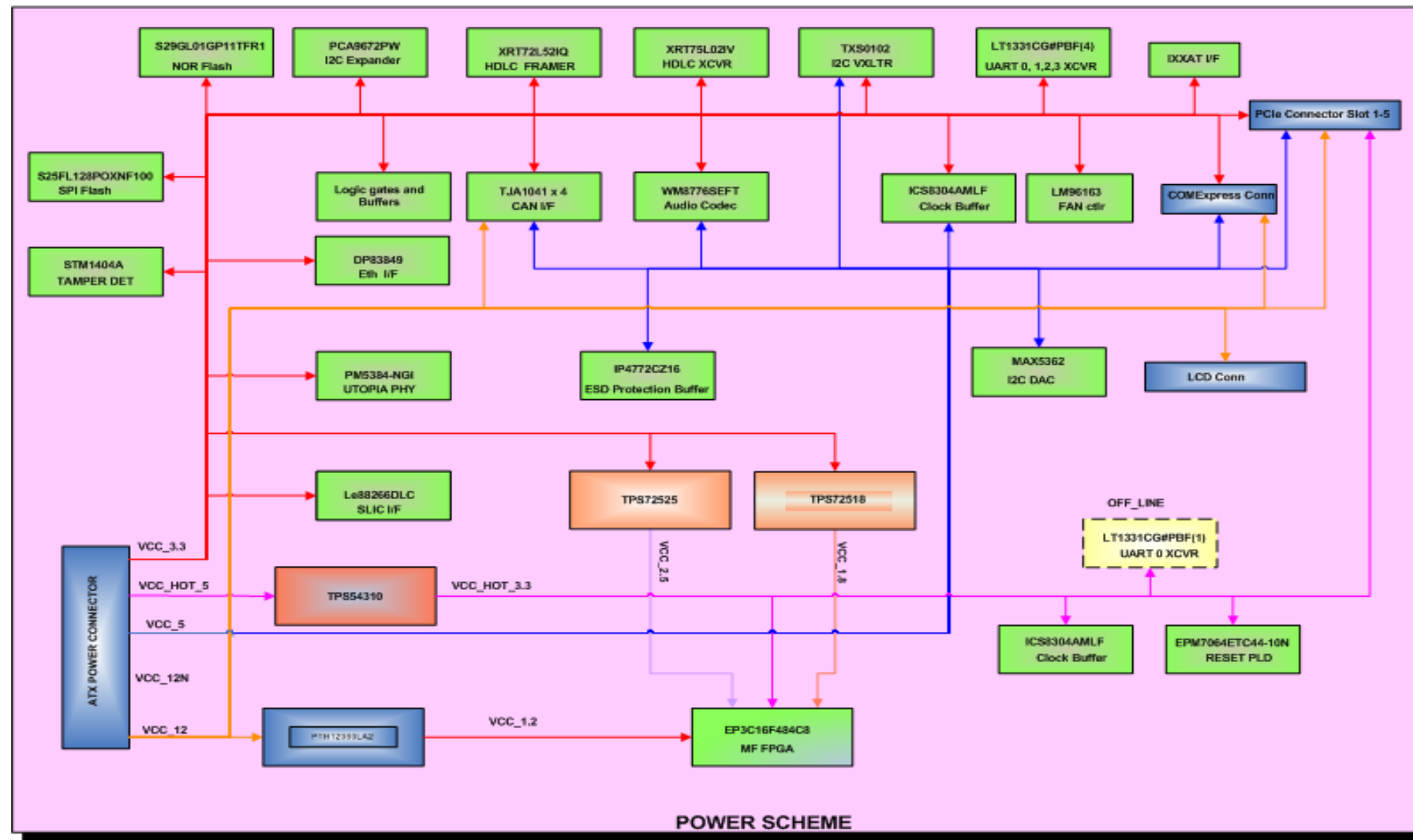
All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your Freescale representative to obtain the latest information on this product.

ICAP Classification: FCP:___ FIUO: X PUBL:___

COMEXPRESS CARRIER (COMe1/2/3)



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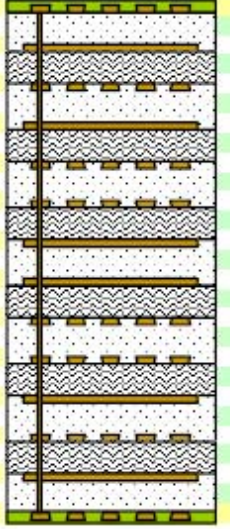
Part Number: Freescale_170-24679_via

Contact: Martin Thompson

Phone: 408-938-7231

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.00	0.5 oz			Foil, 0.5 oz
2	1.20	1 oz	3.86	3.88	Prepreg 370HR 3313(59) 18Gx24
3	0.60	0.5 oz	3.96	6.00	Core 370HR 6mils 1080/3313 0.5 oz / 1 oz 18.25Gx24.25
4	1.20	1 oz	3.68	5.59	Prepreg 370HR 1080(68)1080(68) 18Gx24
5	0.60	0.5 oz	3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
6	0.60	0.5 oz	3.90	3.98	Prepreg 370HR 2116(57) 18Gx24
7	1.20	1 oz	3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
8	1.20	1 oz	3.98	8.25	Prepreg 370HR 2116(53)2116(53) 18Gx24
9	0.60	0.5 oz	3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
10	0.60	0.5 oz	3.90	3.98	Prepreg 370HR 2116(57) 18Gx24
11	1.20	1 oz	3.96	8.00	Core 370HR 8mils 2x3313 0.5 oz / 1 oz 18.25Gx24.25
12	0.60	0.5 oz	3.68	5.59	Prepreg 370HR 1080(68)1080(68) 18Gx24
13	1.20	1 oz	3.96	6.00	Core 370HR 6mils 1080/3313 0.5 oz / 1 oz 18.25Gx24.25
14	2.00	0.5 oz	3.86	3.88	Prepreg 370HR 3313(59) 18Gx24 Foil, 0.5 oz

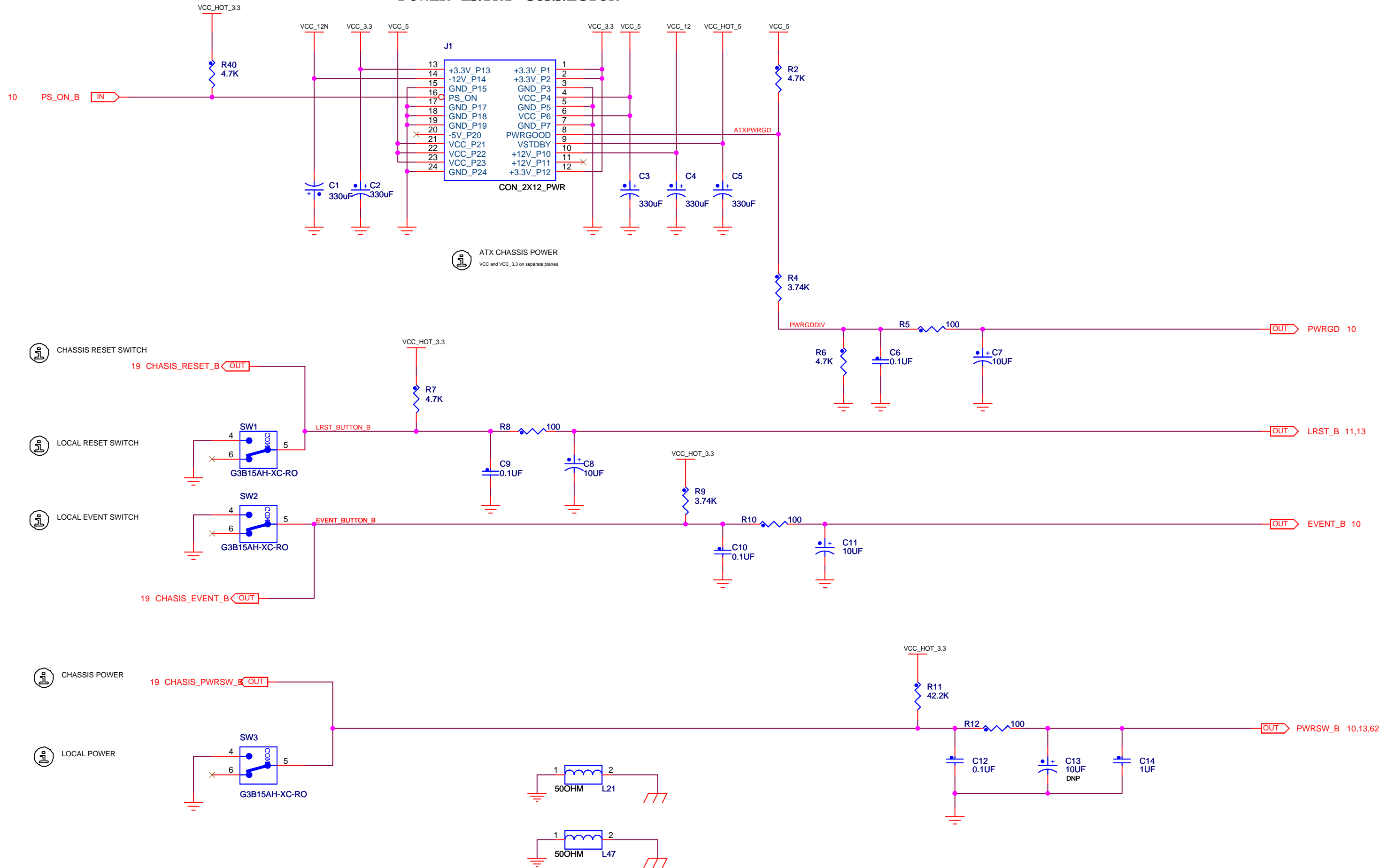
Layers	Drill Type	Via Fill	Thickness	Description
89.53			89.53	Thickness over Laminate
93.53	PTH	--	93.53	Thickness over Copper
94.93			94.93	Thickness over Soldermask



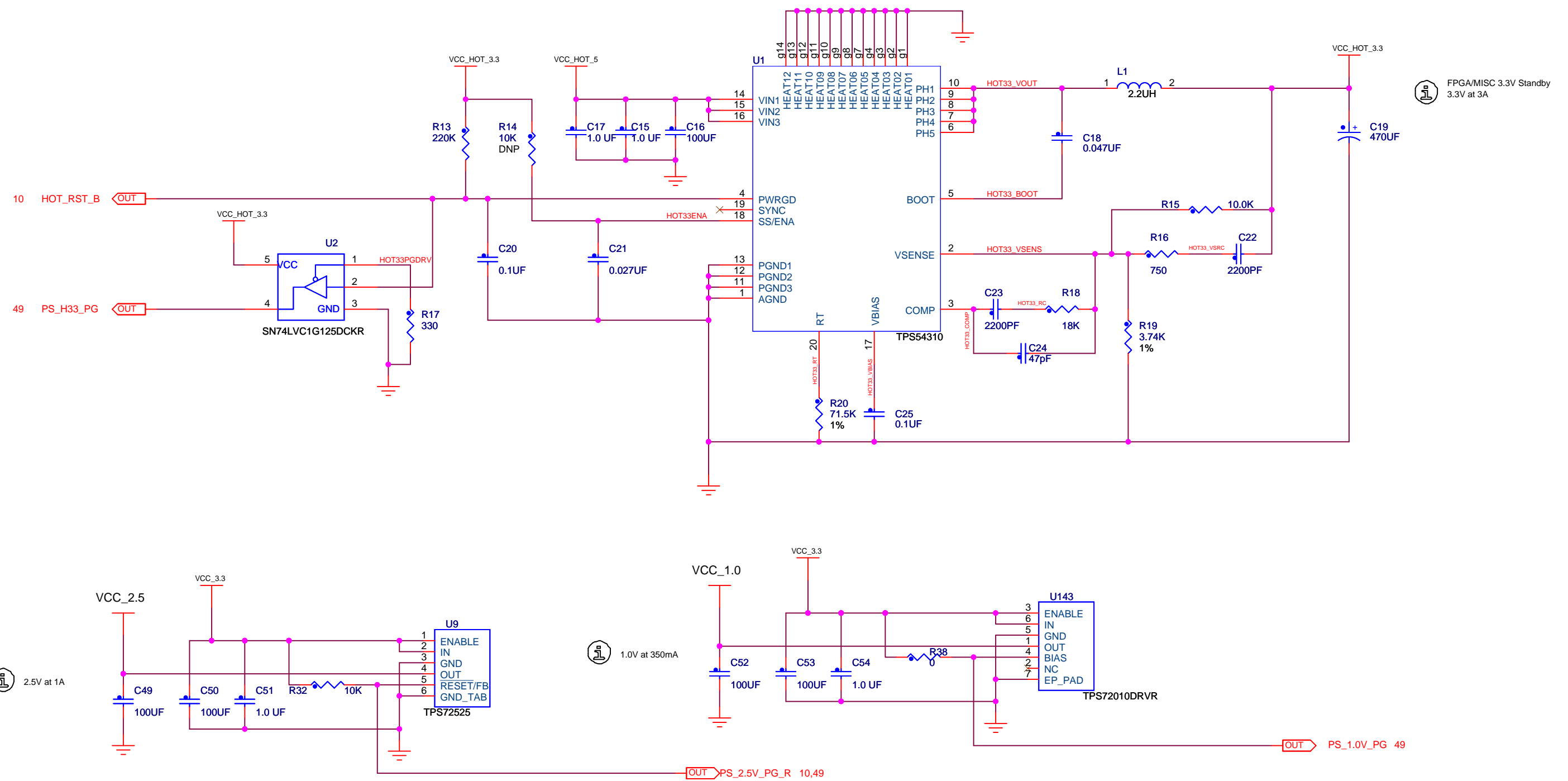
Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Single Ended	Yes	50.00	+/-5	5.75	0.00	(2)	5.75	50.49	
1	Edge Coupled Differential	Yes	100.00	+/-10	4.50	12.00	(2)	4.50	100.13	
3	Edge Coupled Differential	--	100.00	+/-10	4.50	10.00	(2, 4)	4.50	98.45	
3	Edge Coupled Differential	--	90.00	+/-9	5.25	10.00	(2, 4)	5.25	89.70	
3	Edge Coupled Differential	--	92.00	+/-9.2	5.00	10.00	(2, 4)	5.00	92.48	
3	Single Ended	--	50.00	+/-5	5.50	0.00	(2, 4)	5.50	49.71	
3	Edge Coupled Differential	--	120.00	+/-12	3.50	14.00	(2, 4)	3.50	118.99	
5	Edge Coupled Differential	--	120.00	+/-12	4.25	12.00	(4, 7)	4.25	119.31	
5	Edge Coupled Differential	--	100.00	+/-10	5.00	10.00	(4, 7)	5.00	101.95	
5	Edge Coupled Differential	--	90.00	+/-9	6.00	10.00	(4, 7)	6.00	90.59	
5	Edge Coupled Differential	--	92.00	+/-9.2	5.75	10.00	(4, 7)	5.75	93.30	
5	Single Ended	--	50.00	+/-5	9.00	0.00	(4, 7)	9.00	50.16	
6	Edge Coupled Differential	--	120.00	+/-12	4.25	12.00	(4, 7)	4.25	119.31	
6	Edge Coupled Differential	--	100.00	+/-10	5.00	10.00	(4, 7)	5.00	101.95	
6	Edge Coupled Differential	--	90.00	+/-9	6.00	10.00	(4, 7)	6.00	90.59	
6	Edge Coupled Differential	--	92.00	+/-9.2	5.75	10.00	(4, 7)	5.75	93.30	
6	Single Ended	--	50.00	+/-5	9.00	0.00	(4, 7)	9.00	50.16	
9	Edge Coupled Differential	--	120.00	+/-12	4.25	12.00	(8, 11)	4.25	119.31	
9	Edge Coupled Differential	--	100.00	+/-10	5.00	10.00	(8, 11)	5.00	101.95	
9	Edge Coupled Differential	--	90.00	+/-9	6.00	10.00	(8, 11)	6.00	90.59	
9	Edge Coupled Differential	--	92.00	+/-9.2	5.75	10.00	(8, 11)	5.75	93.30	
9	Single Ended	--	50.00	+/-5	9.00	0.00	(8, 11)	9.00	50.16	
10	Edge Coupled Differential	--	120.00	+/-12	4.25	12.00	(8, 11)	4.25	119.31	
10	Edge Coupled Differential	--	100.00	+/-10	5.00	10.00	(8, 11)	5.00	101.95	
10	Edge Coupled Differential	--	90.00	+/-9	6.00	10.00	(8, 11)	6.00	90.59	
10	Edge Coupled Differential	--	92.00	+/-9.2	5.75	10.00	(8, 11)	5.75	93.30	
10	Single Ended	--	50.00	+/-5	9.00	0.00	(8, 11)	9.00	50.16	
12	Edge Coupled Differential	--	100.00	+/-10	4.50	10.00	(11, 13)	4.50	98.45	
12	Edge Coupled Differential	--	90.00	+/-9	5.25	10.00	(11, 13)	5.25	89.70	
12	Edge Coupled Differential	--	92.00	+/-9.2	5.00	10.00	(11, 13)	5.00	92.48	
12	Single Ended	--	50.00	+/-5	5.50	0.00	(11, 13)	5.50	49.71	
12	Edge Coupled Differential	--	120.00	+/-12	3.50	14.00	(11, 13)	3.50	118.99	
14	Single Ended	Yes	50.00	+/-5	5.75	0.00	(13)	5.75	50.49	
14	Edge Coupled Differential	Yes	100.00	+/-10	4.50	12.00	(13)	4.50	100.13	

* Edge Coupled Pitch is measured from the center line of one differential trace to the center line of the other.

POWER ENTRY CONNECTOR



5V to 3.3V Step Down Regulator



FPGA/MISC 3.3V Standby
3.3V at 3A

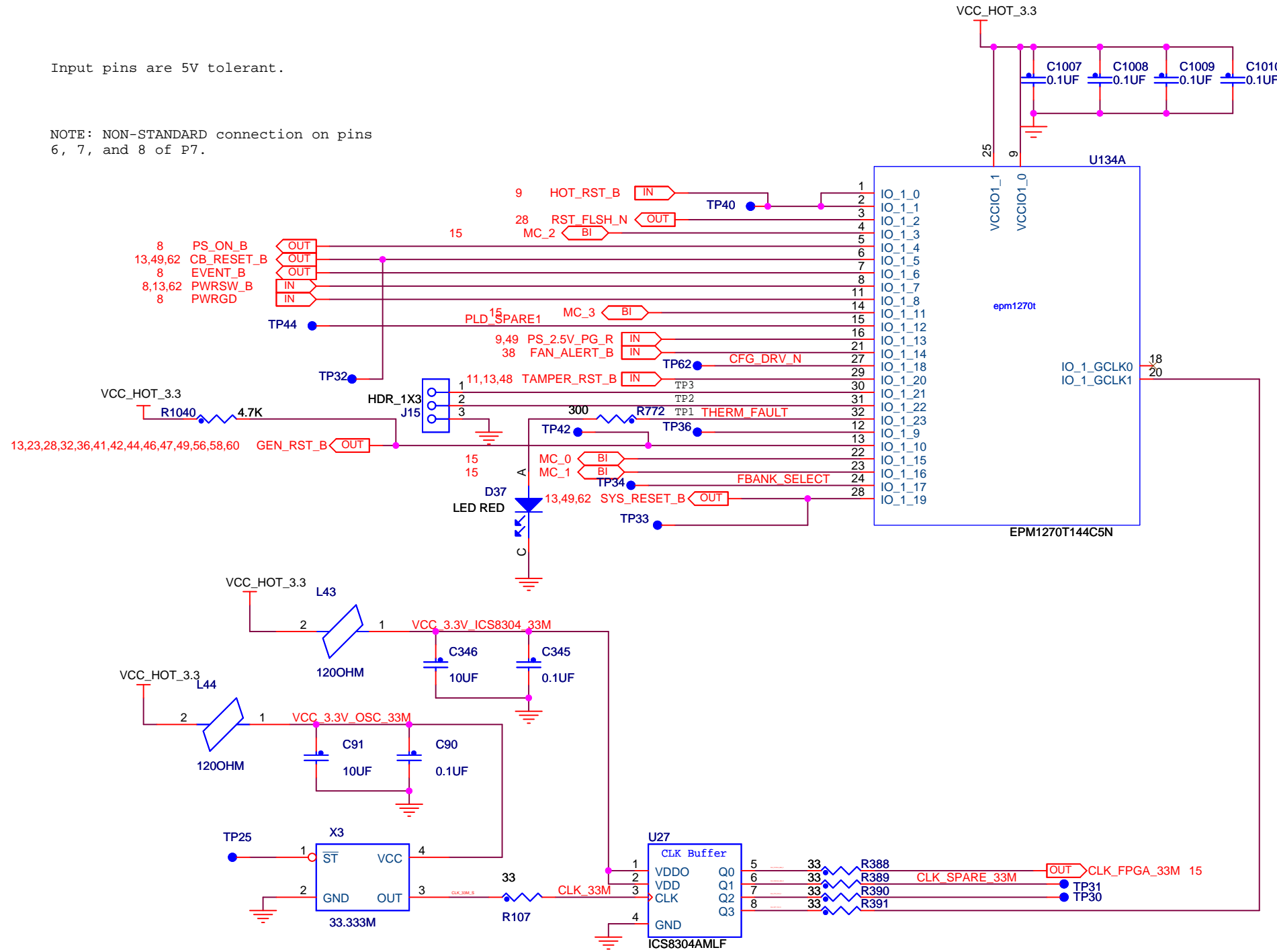
2.5V at 1A

1.0V at 350mA

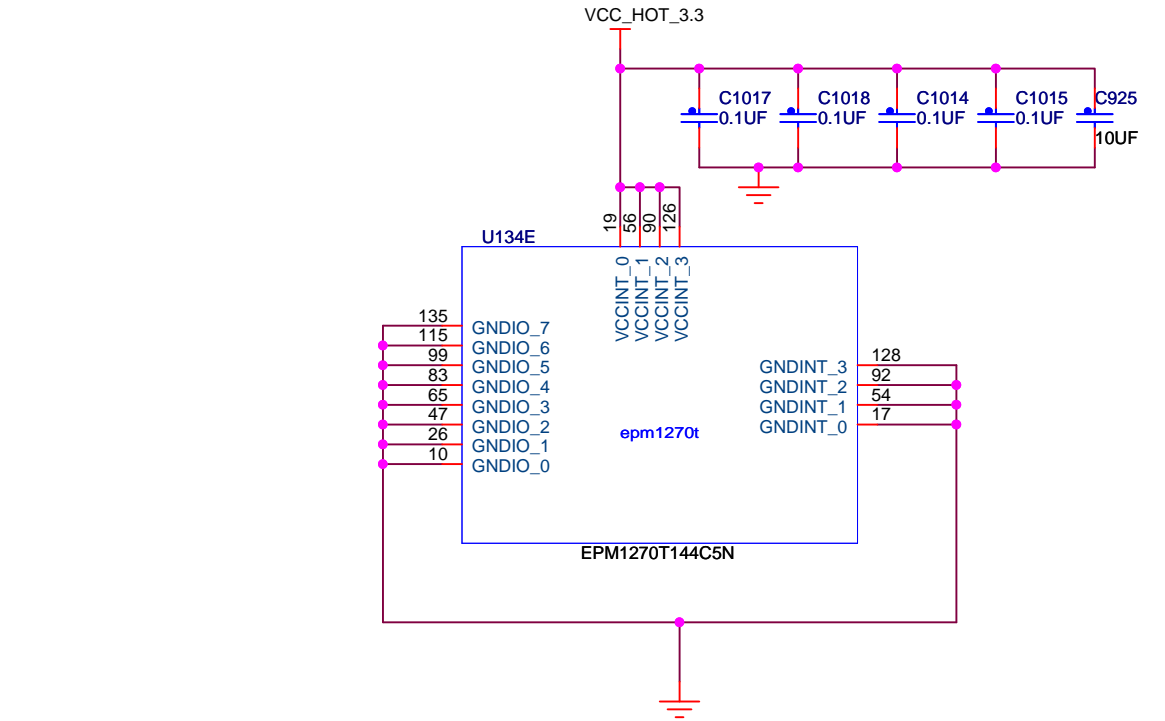
CPLD Interface

Input pins are 5V tolerant.

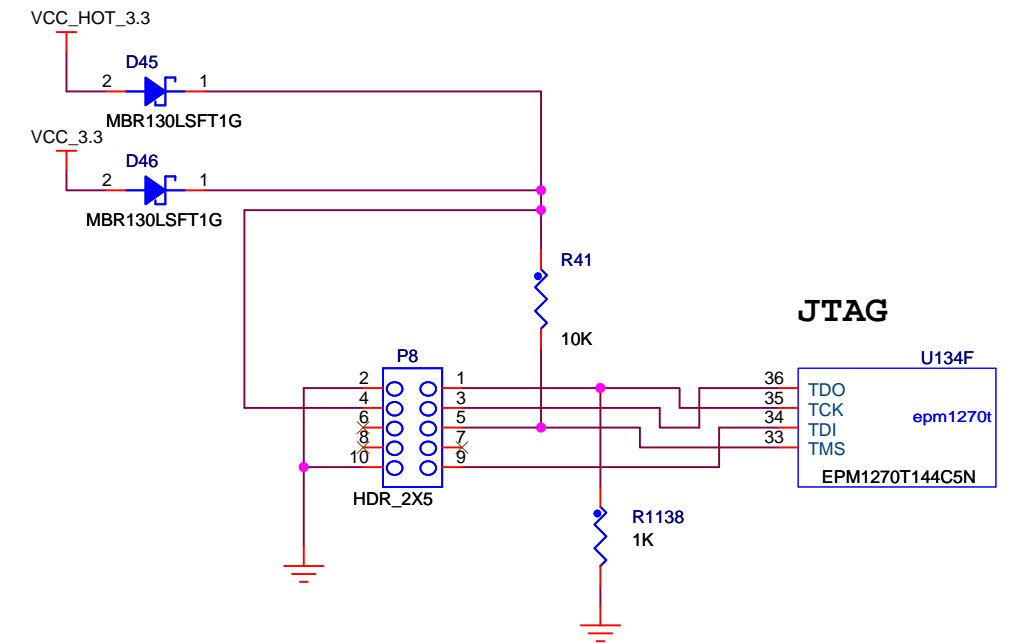
NOTE: NON-STANDARD connection on pins 6, 7, and 8 of P7.



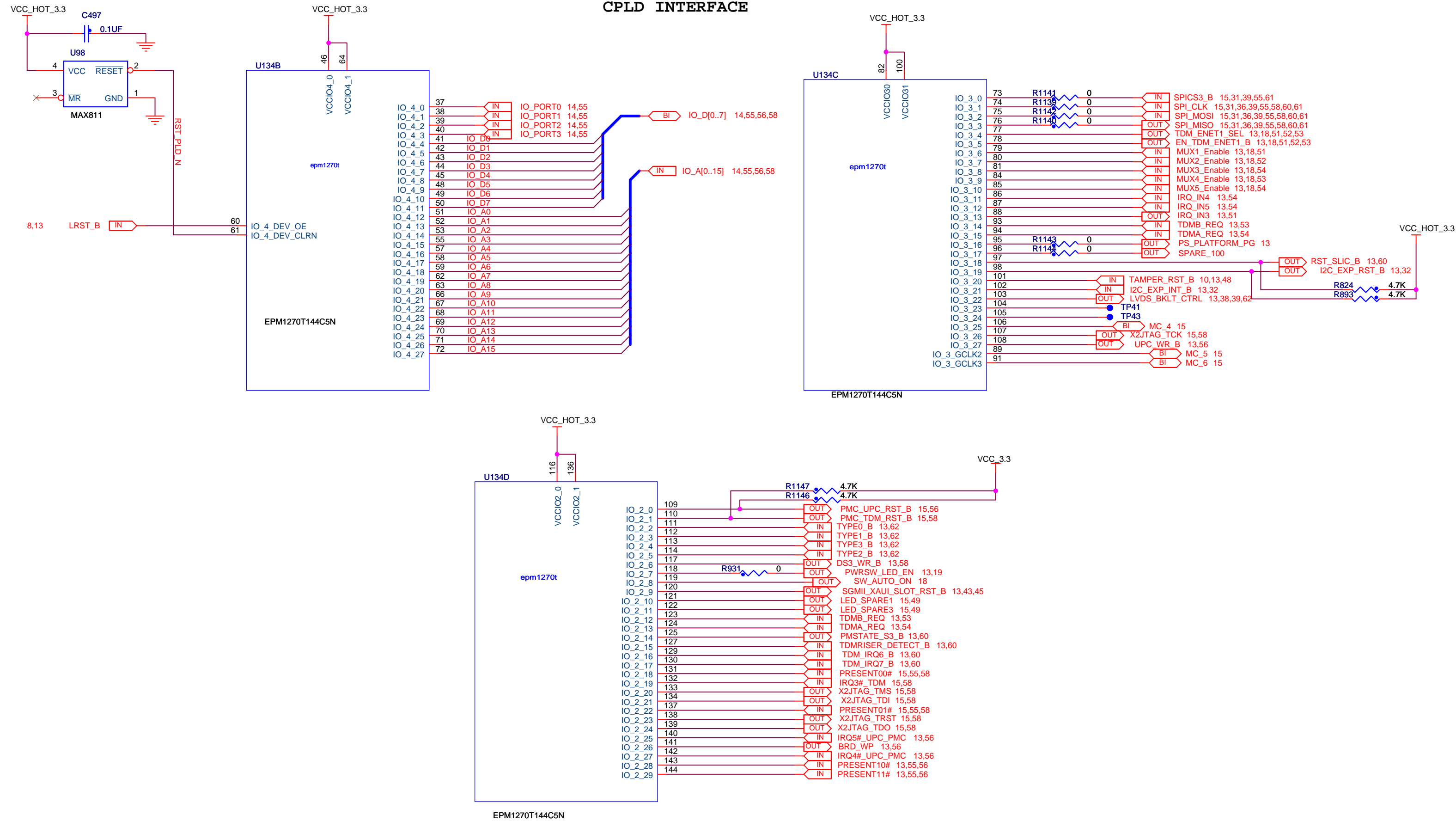
CPLD POWER



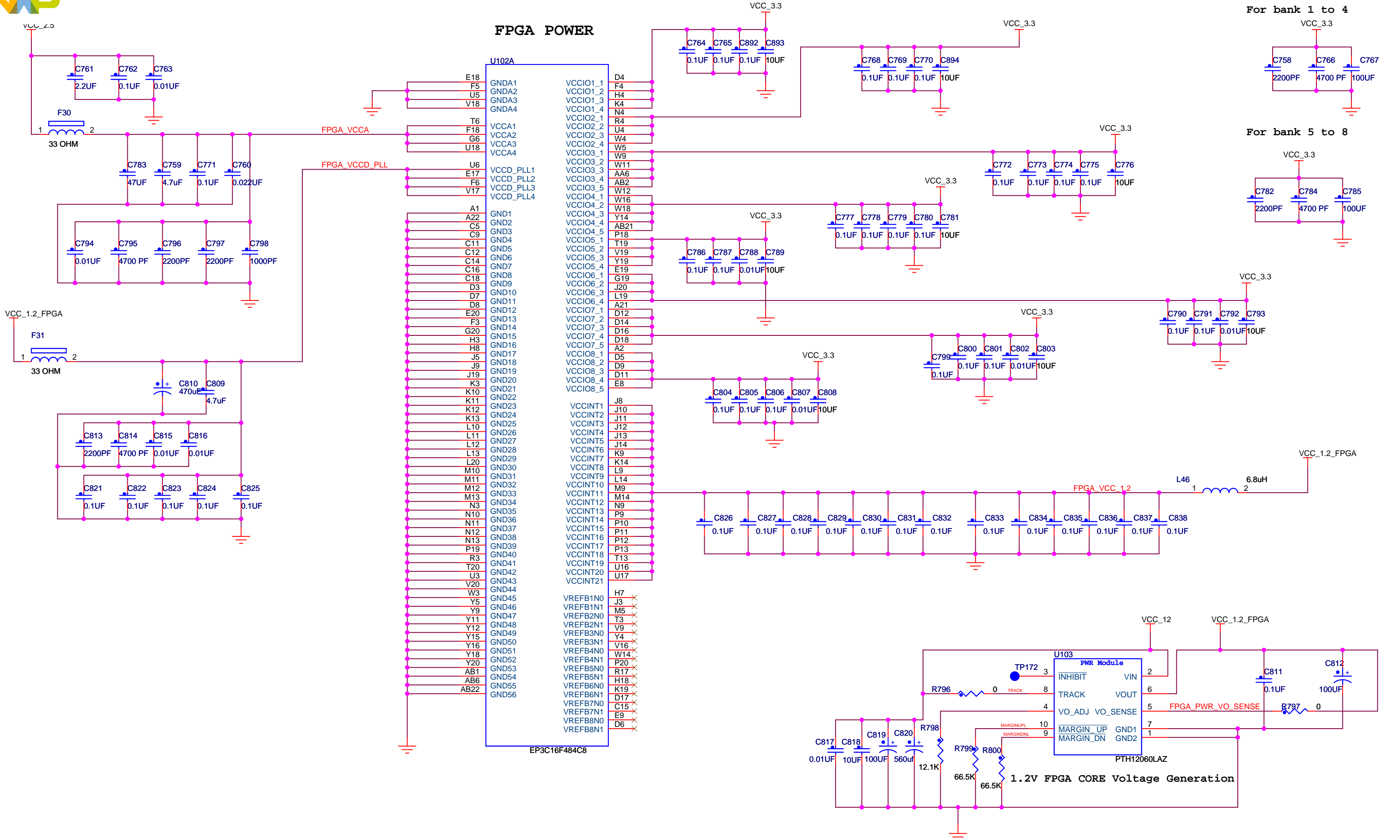
CLOCK Generation for CPLD



CPLD INTERFACE



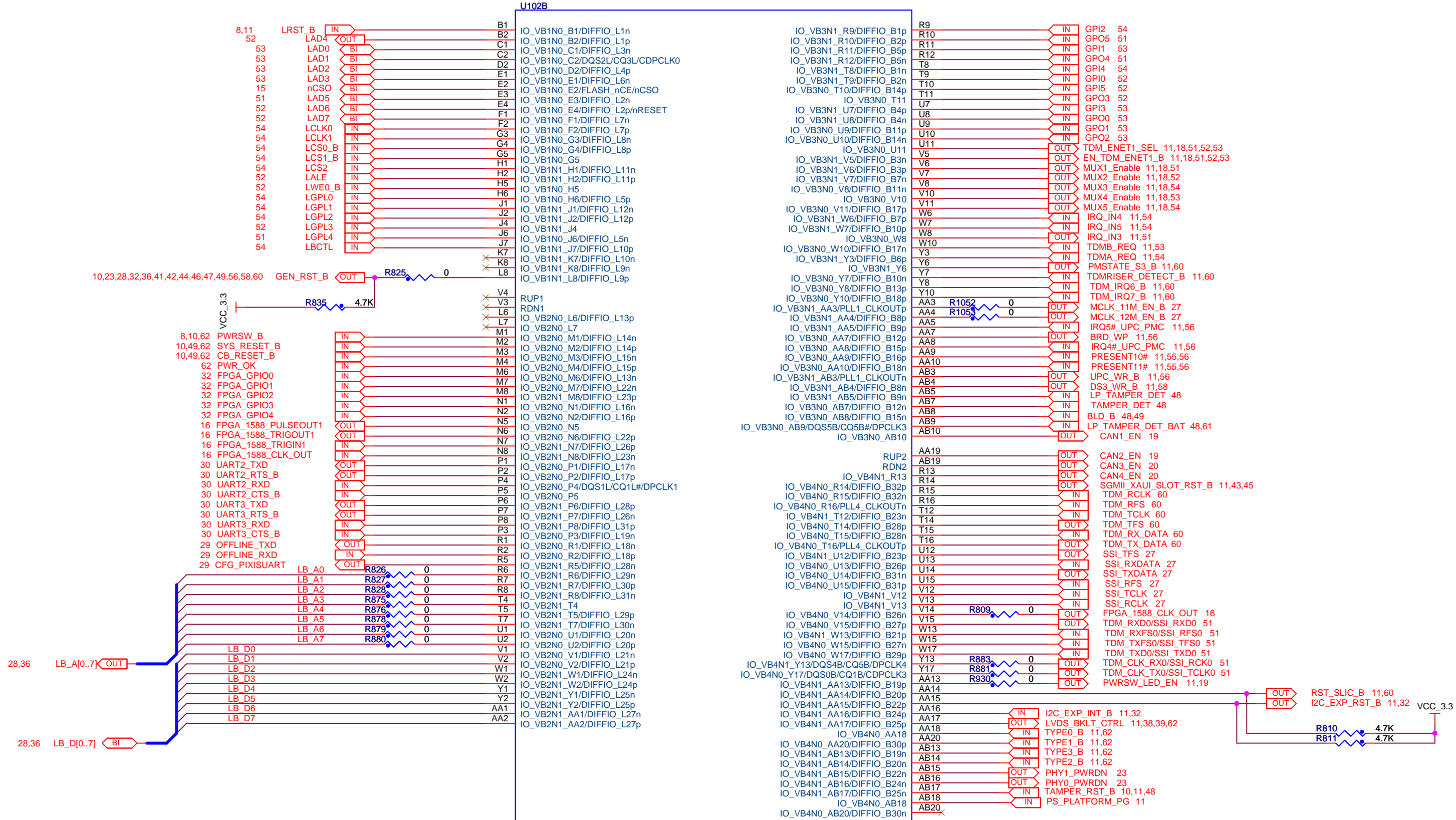
FPGA POWER



For bank 1 to 4

For bank 5 to 8

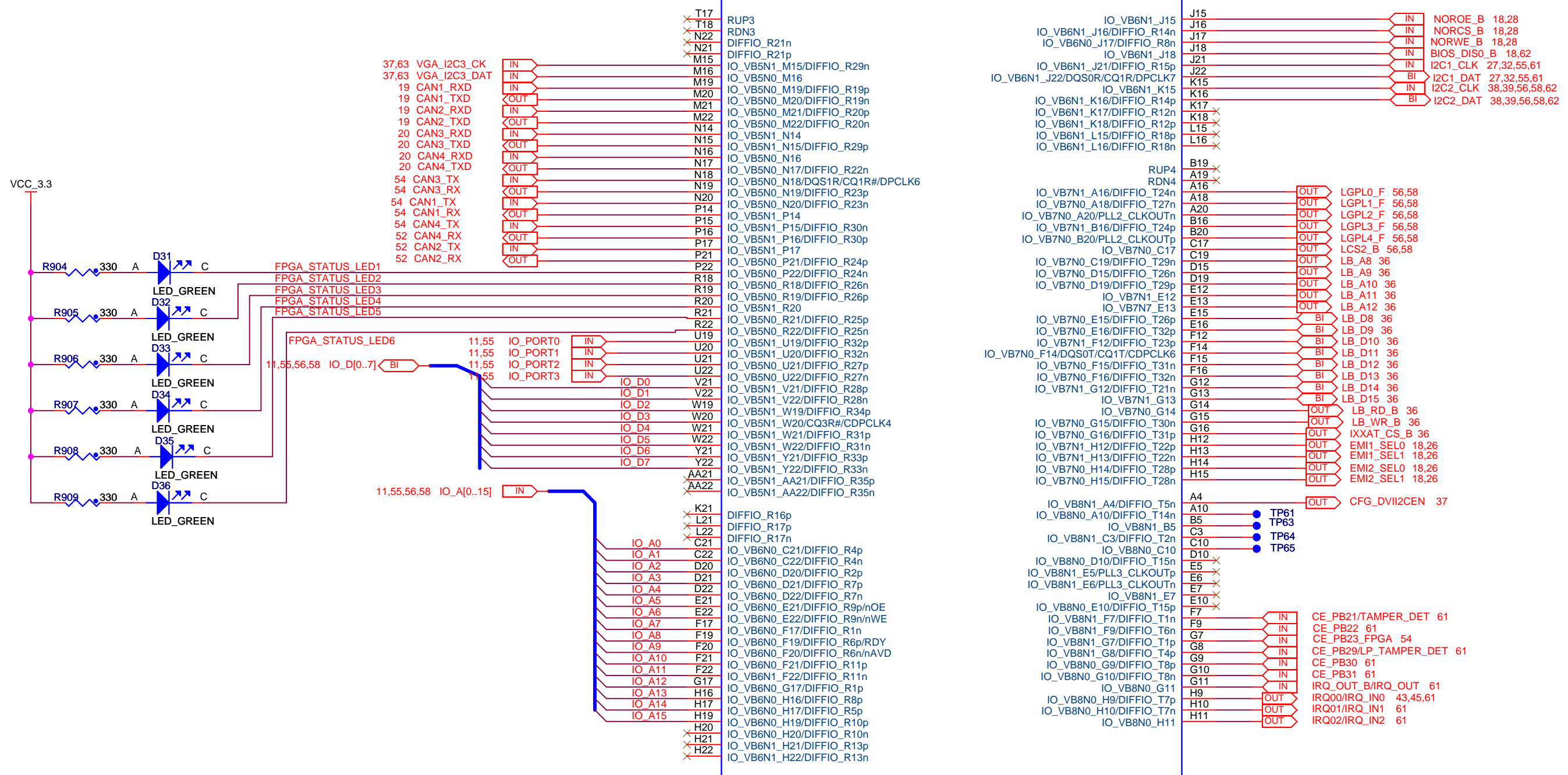
FPGA INTERFACE



EP3C16F484C8

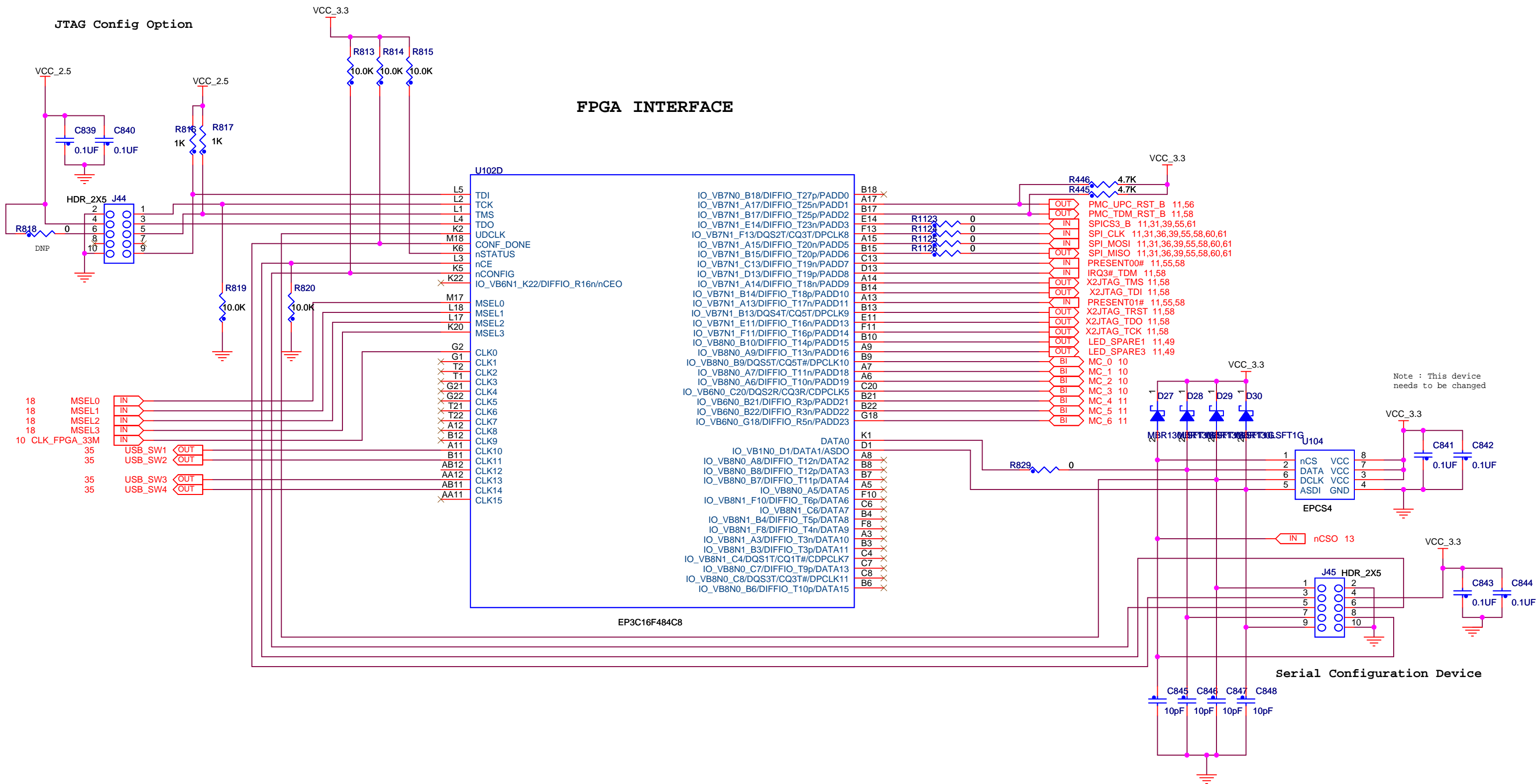
FPGA INTERFACE

U102C



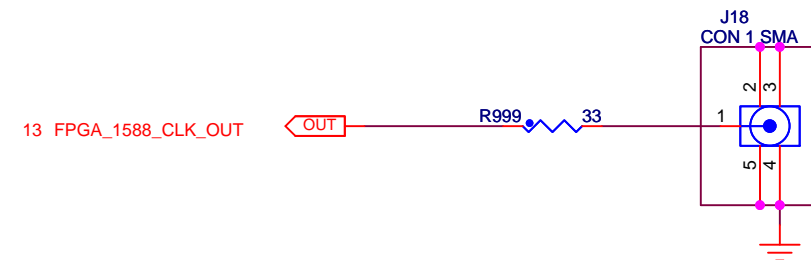
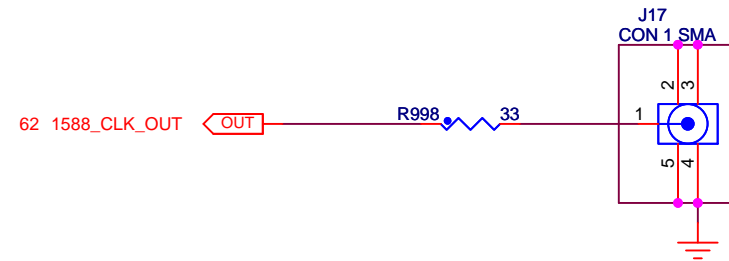
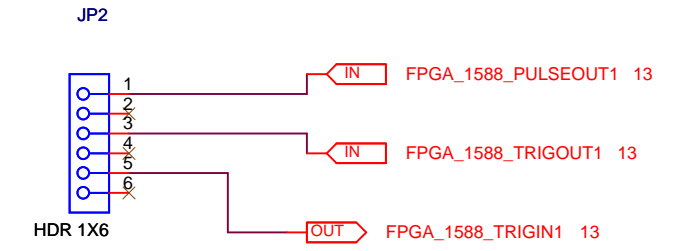
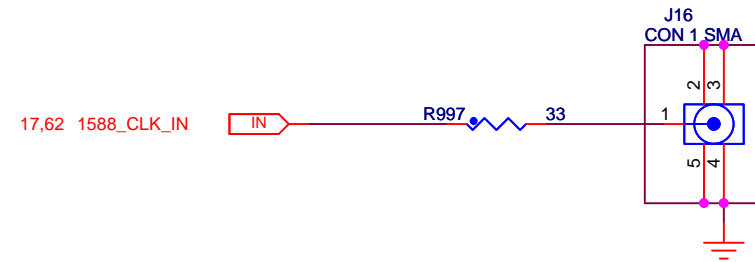
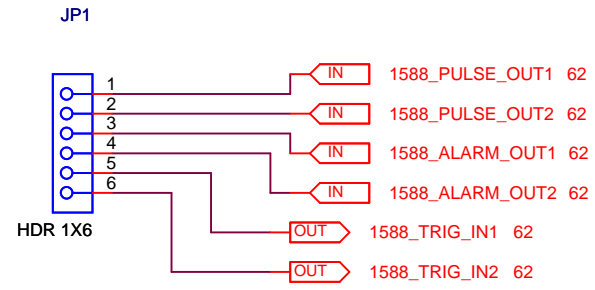
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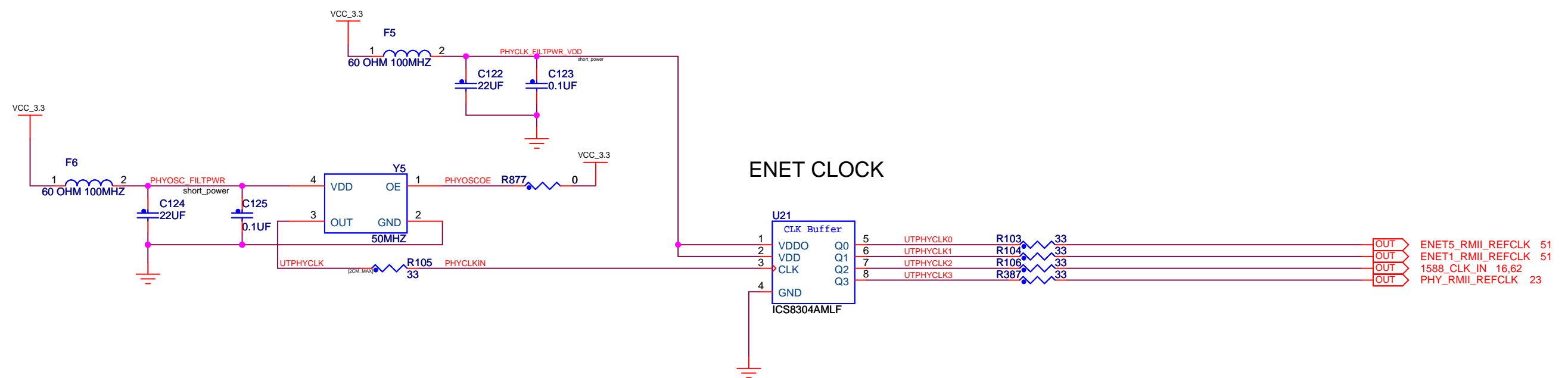
FPGA INTERFACE



Note : This device needs to be changed

1588 INTERFACE

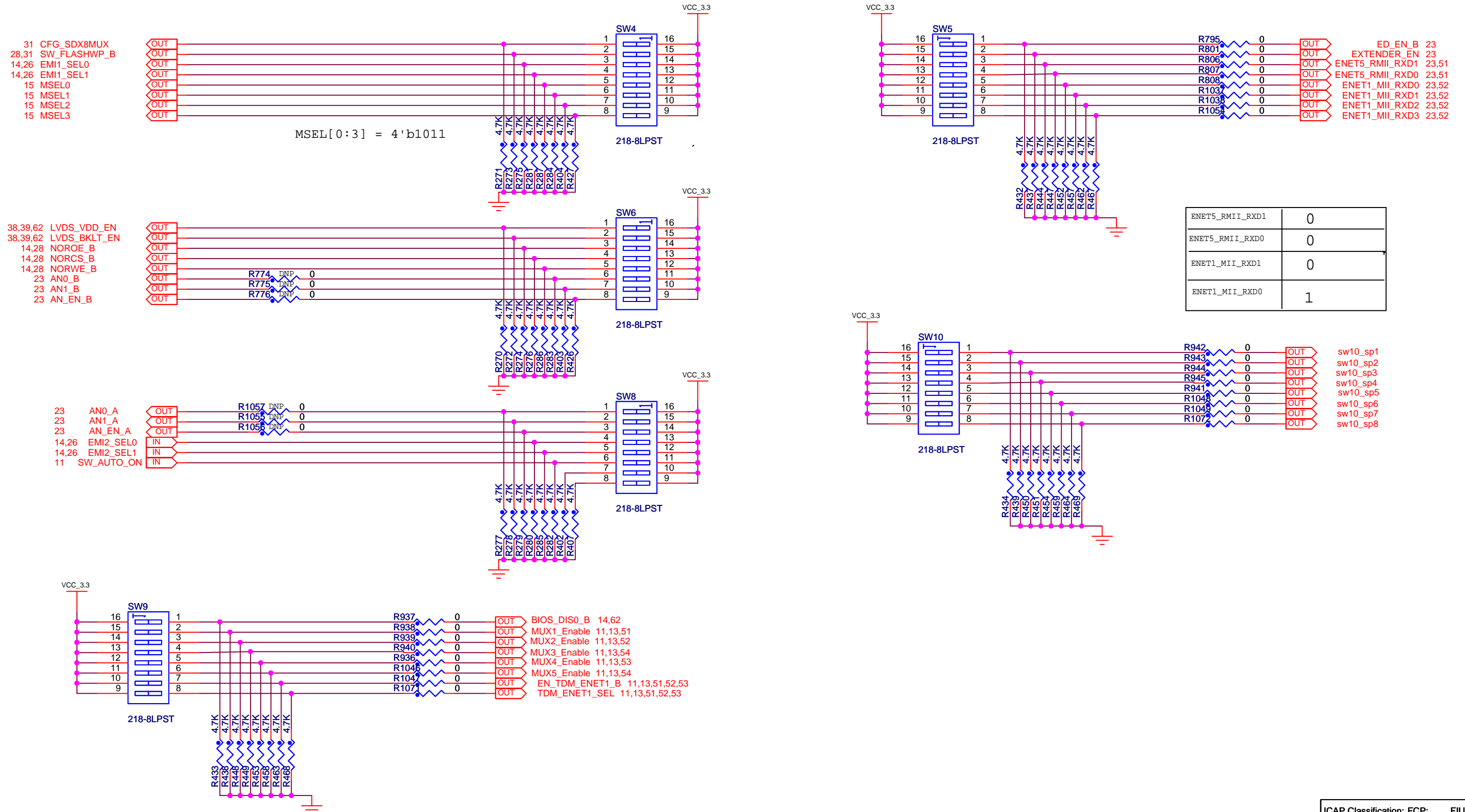




ENET CLOCK

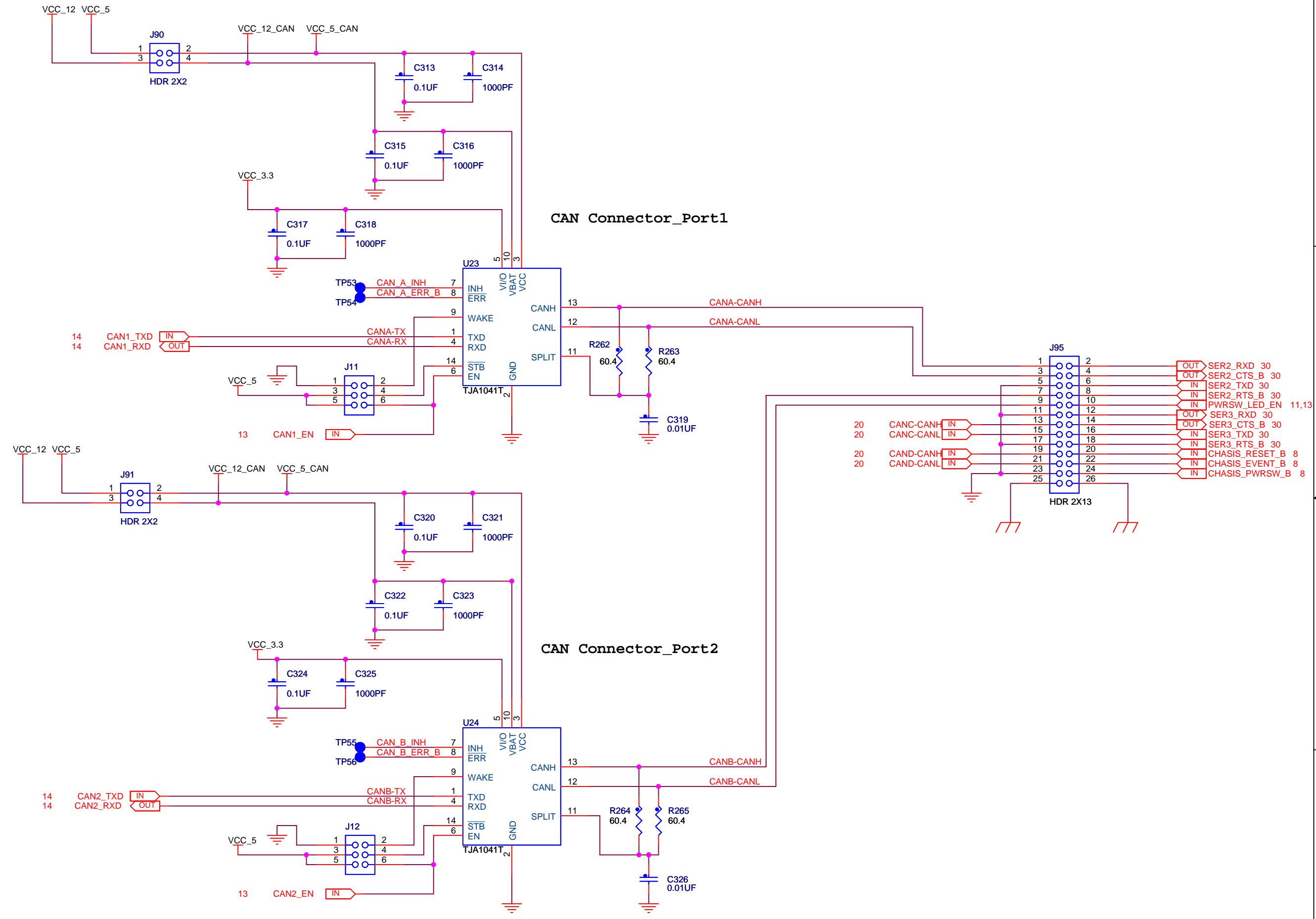
U21
CLK Buffer
VDDO Q0
VDD Q1
CLK Q2
Q3
GND
ICS8304AMLF

CONFIGURATION SWITCHES



CANA

CANB

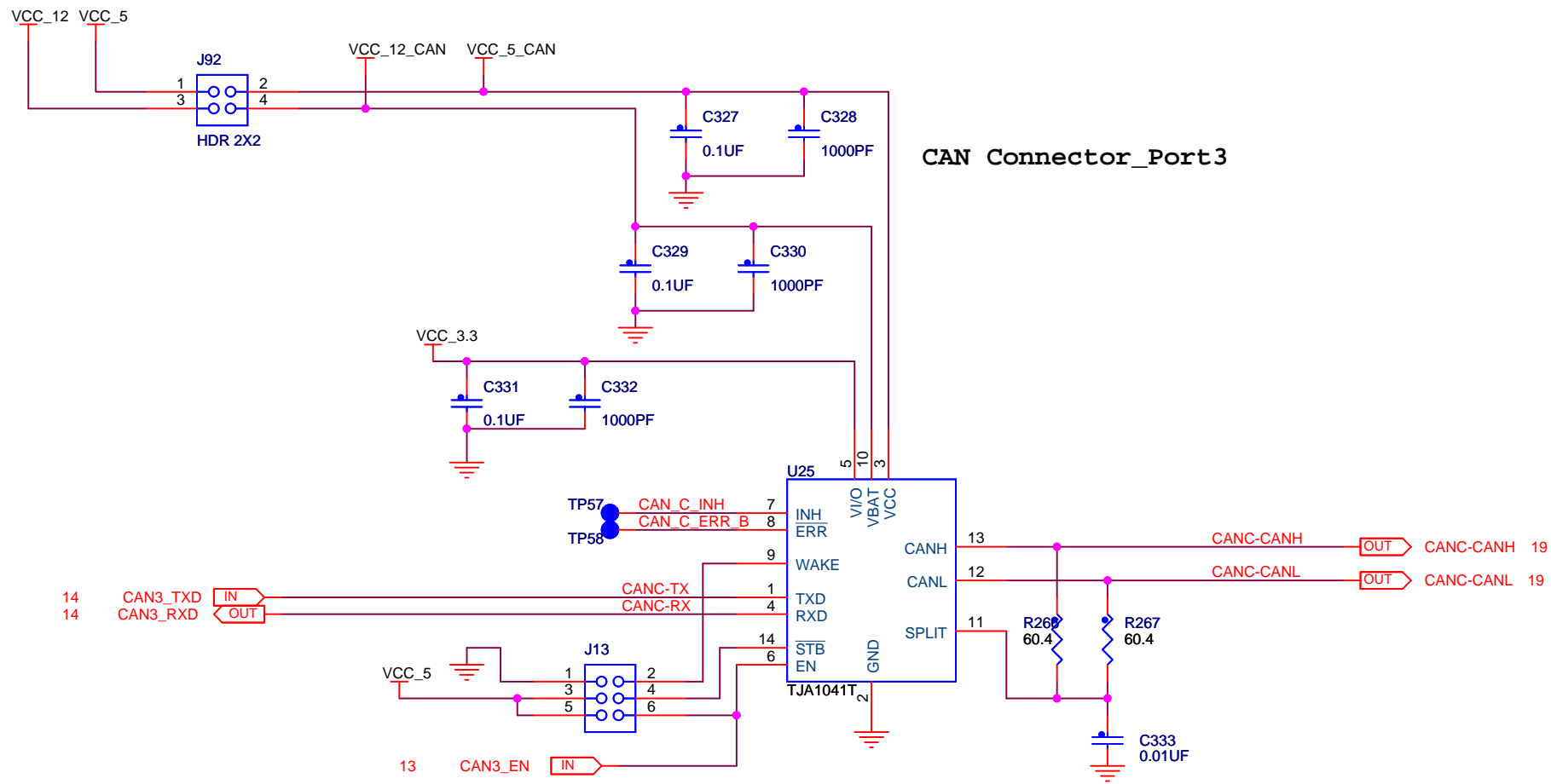


CAN Connector_Port1

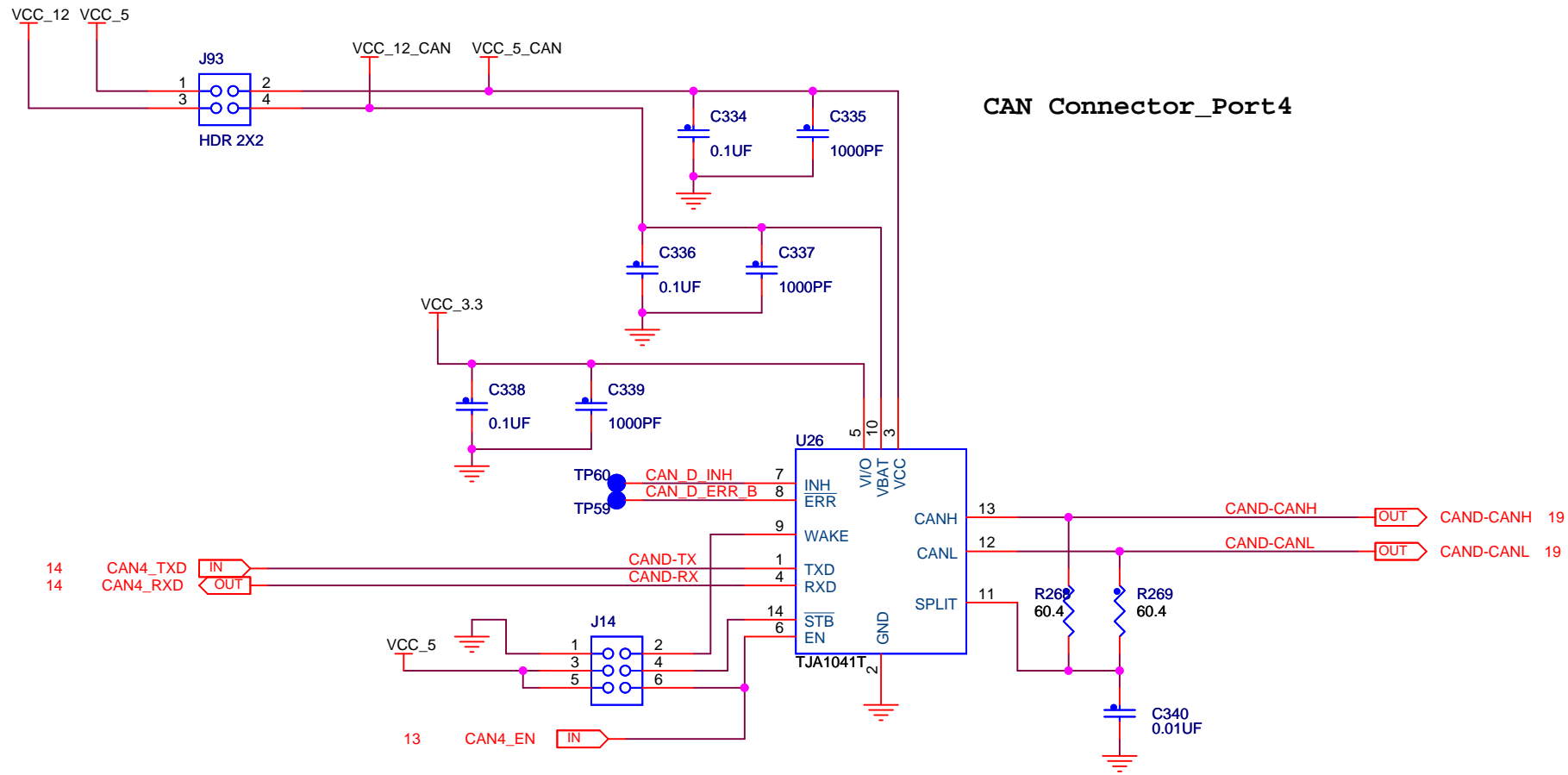
CAN Connector_Port2



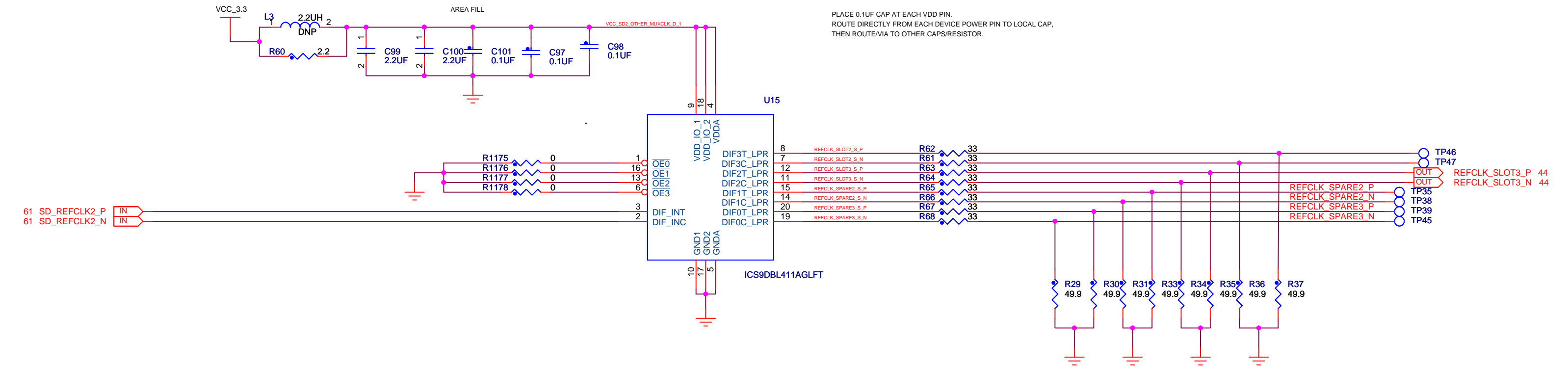
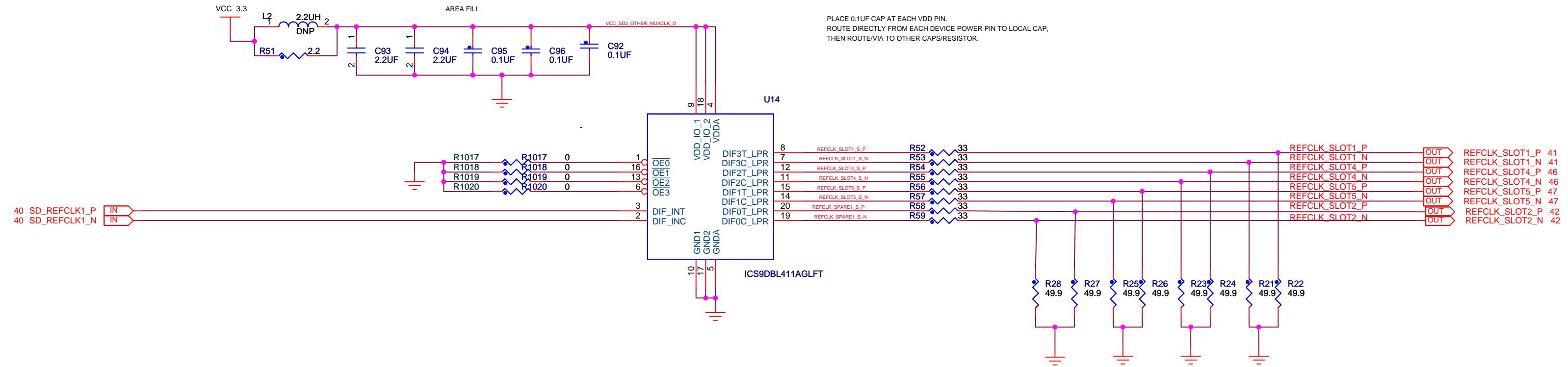
CANC



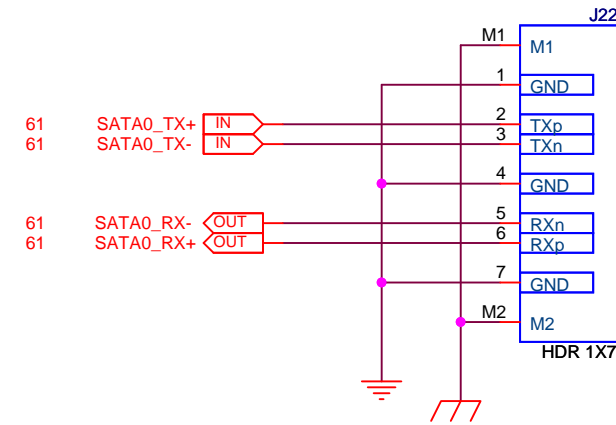
CAND



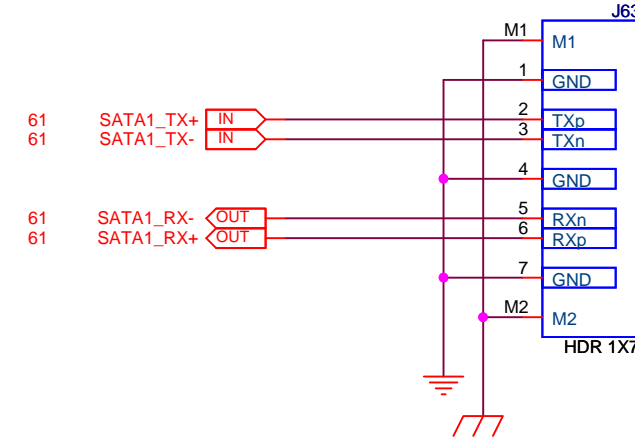
SERDES REFCLK BUFFER



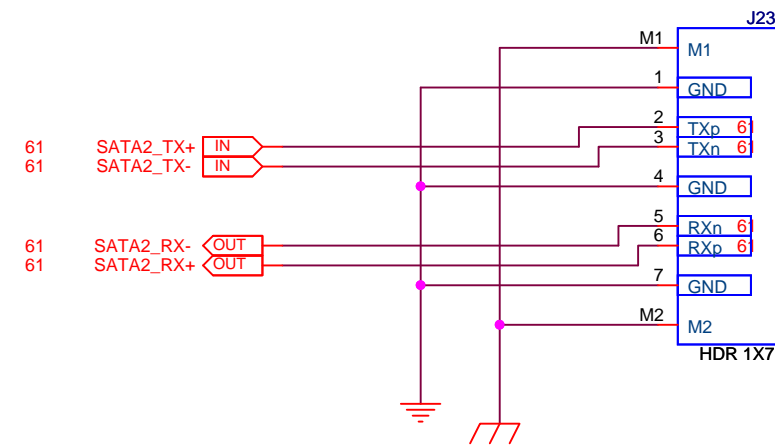
SATA Connector Port 0



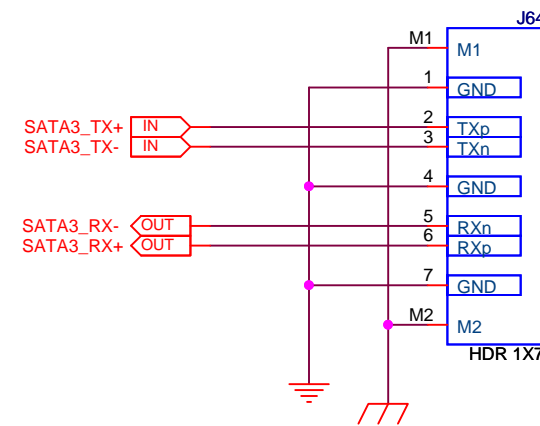
SATA Connector Port 1



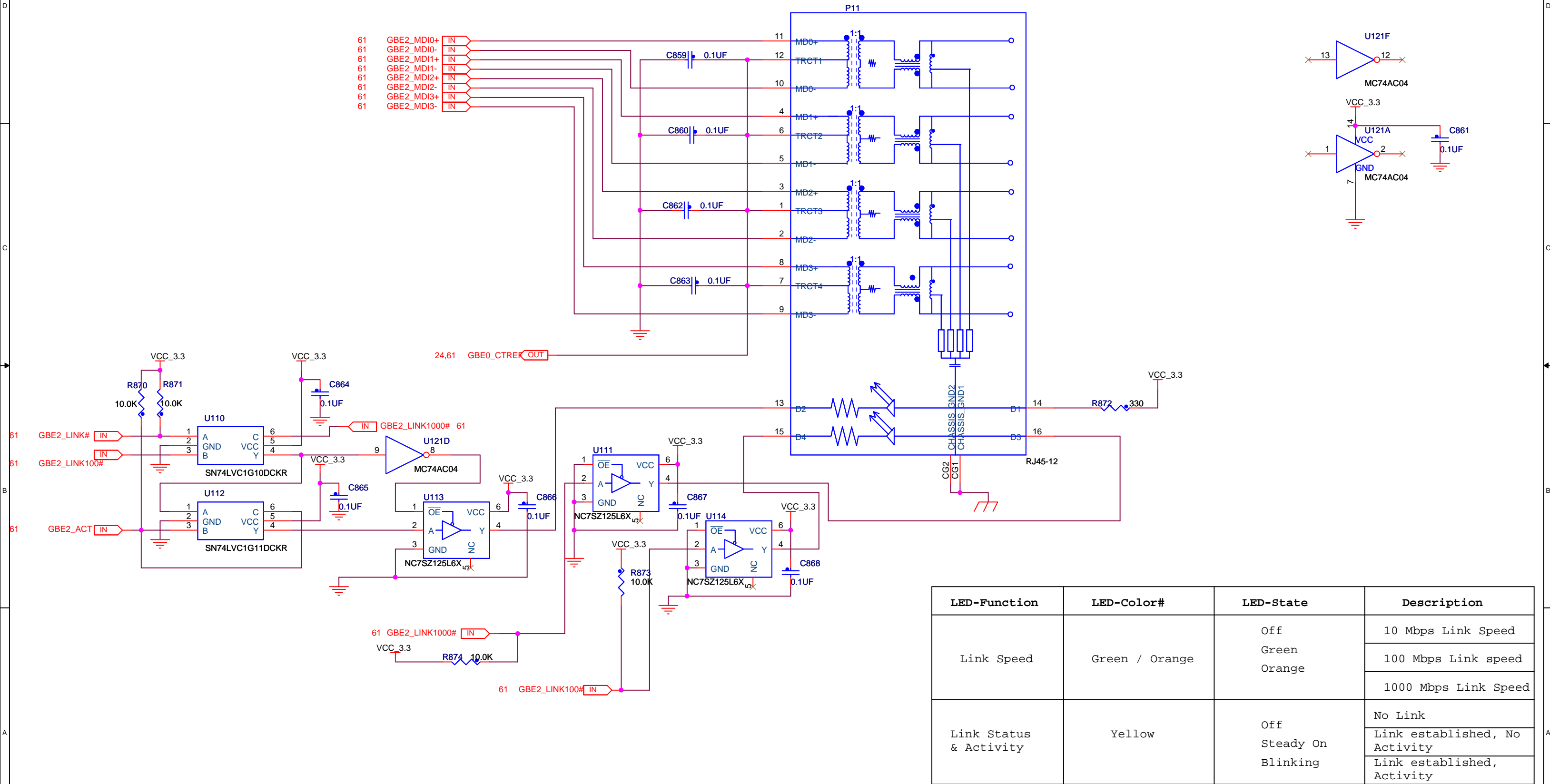
SATA Connector Port 2



SATA Connector Port 3

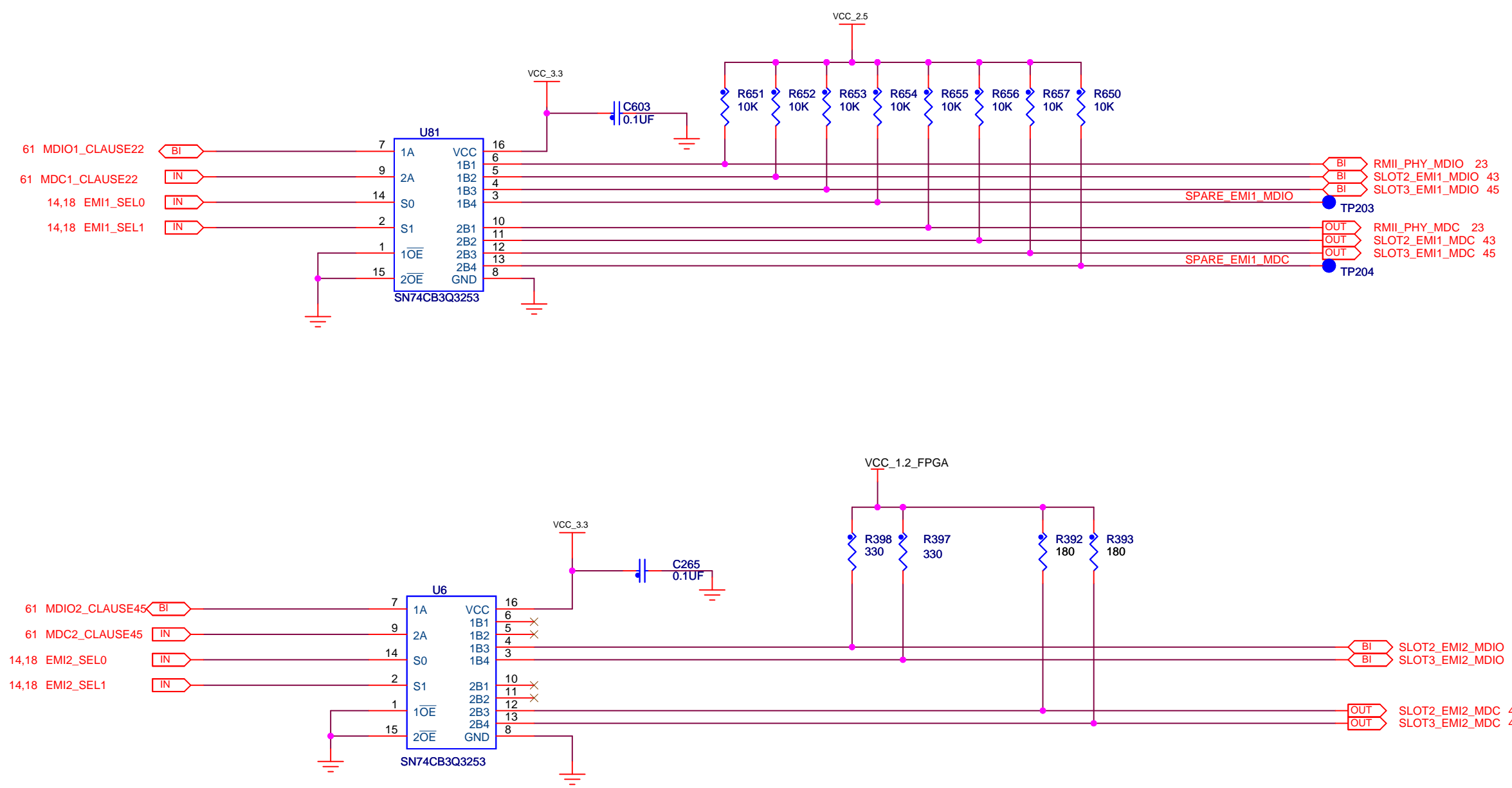


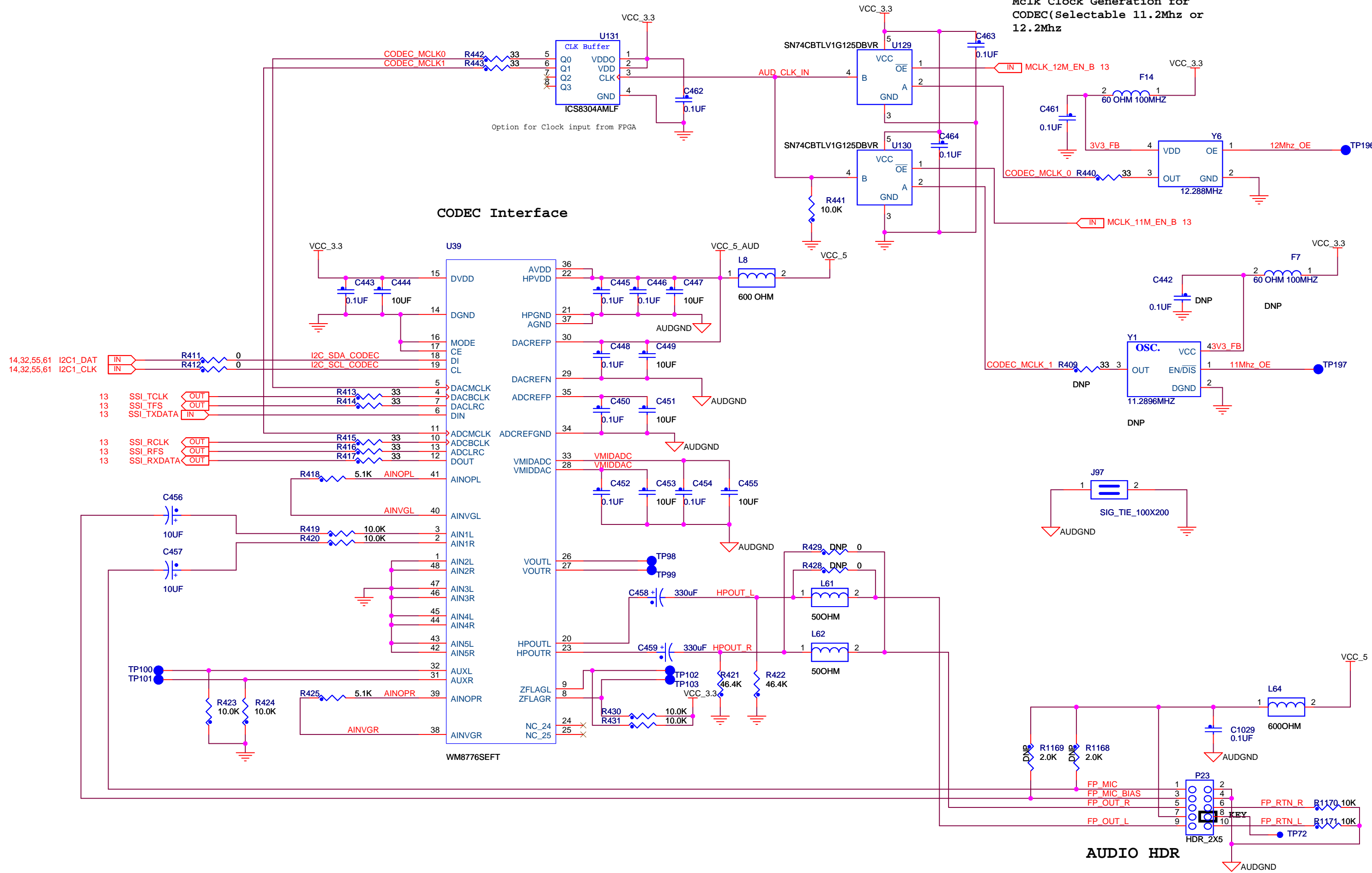
GIGA BIT ETHERNET PORT 3



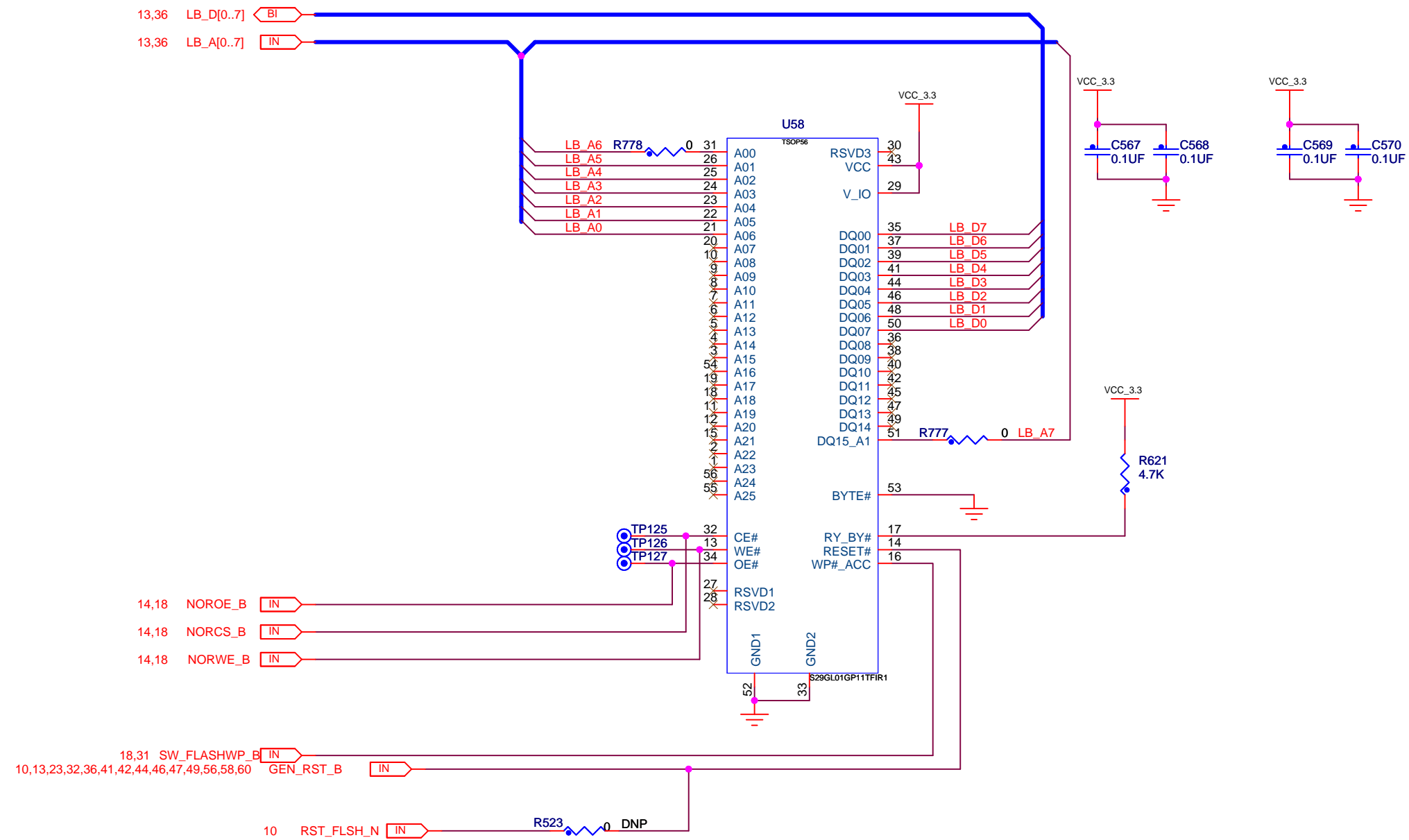
LED-Function	LED-Color#	LED-State	Description
Link Speed	Green / Orange	Off	10 Mbps Link Speed
		Green	100 Mbps Link speed
		Orange	1000 Mbps Link Speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, No Activity
		Blinking	Link established, Activity

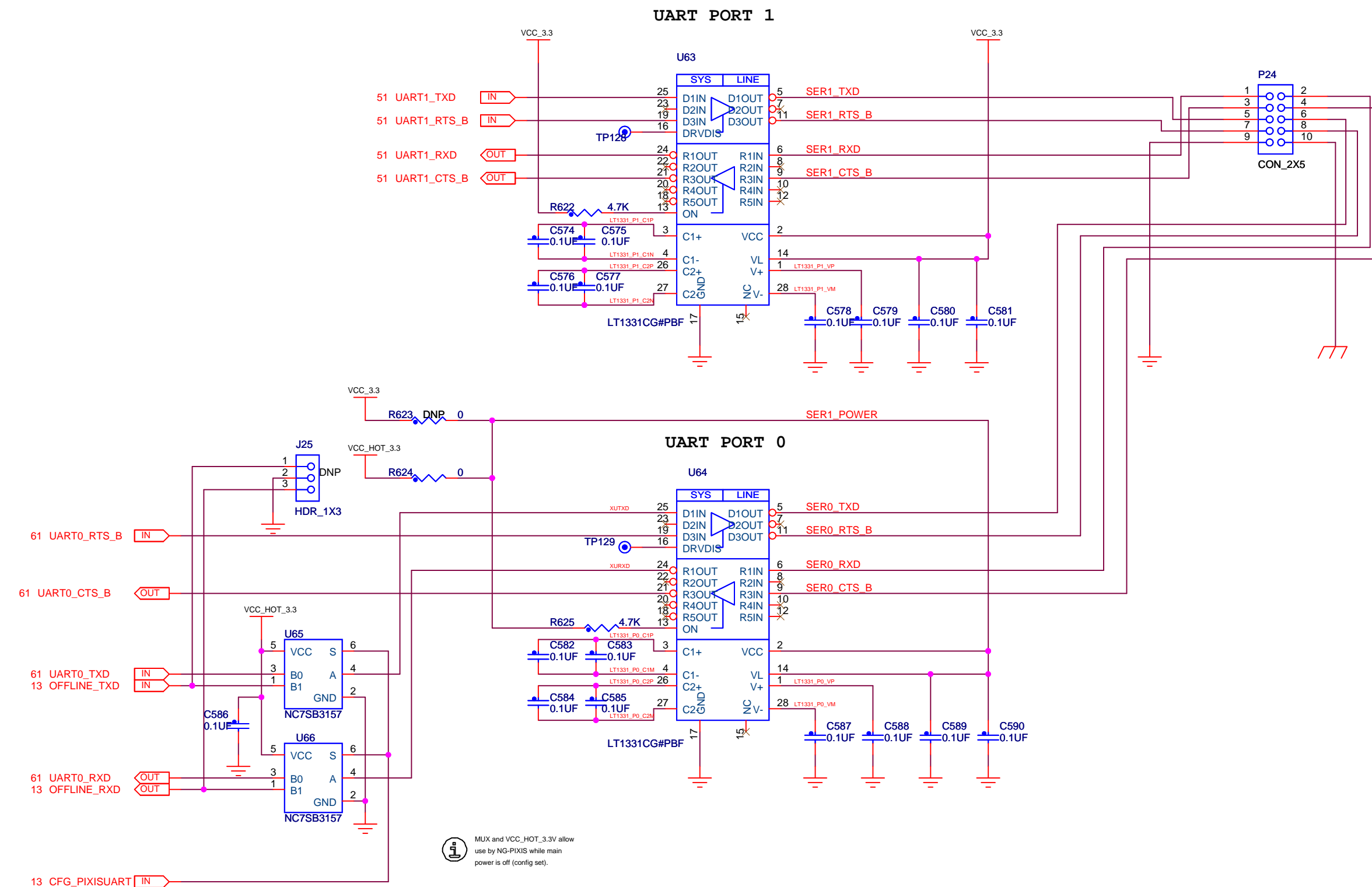
MANAGEMENT BUS MUXING



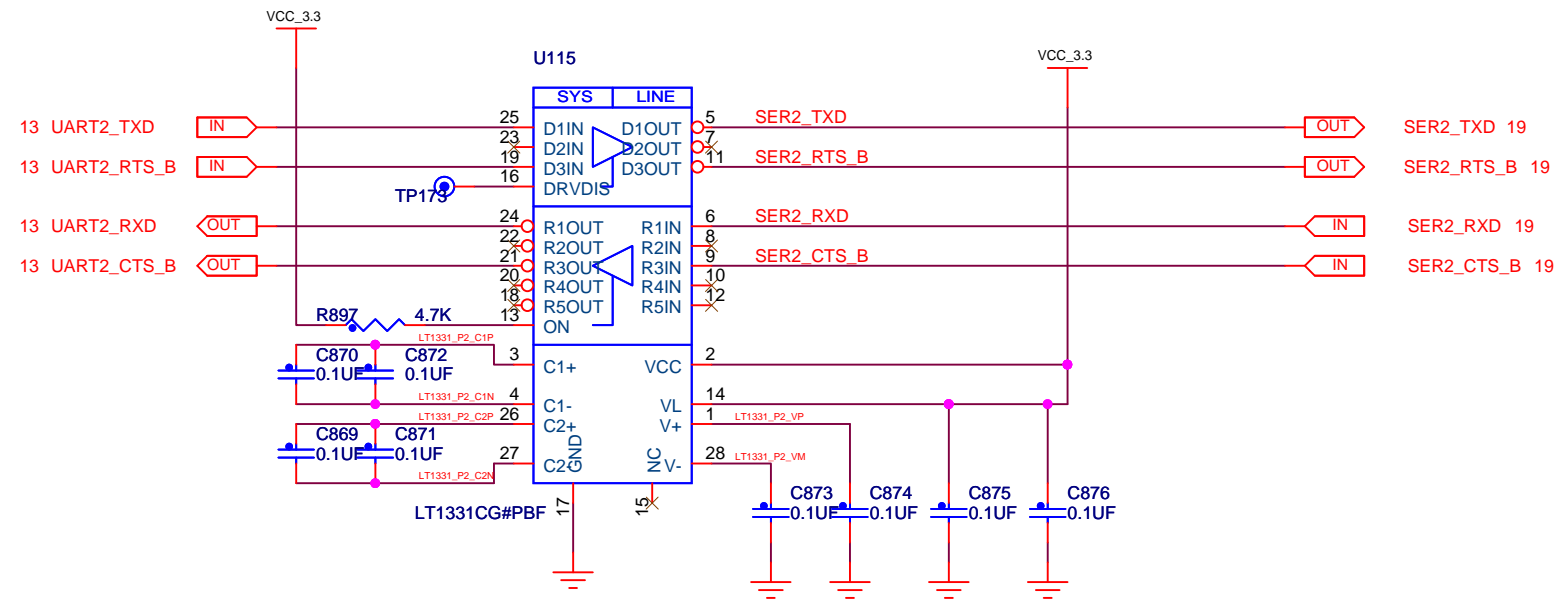


NOR FLASH

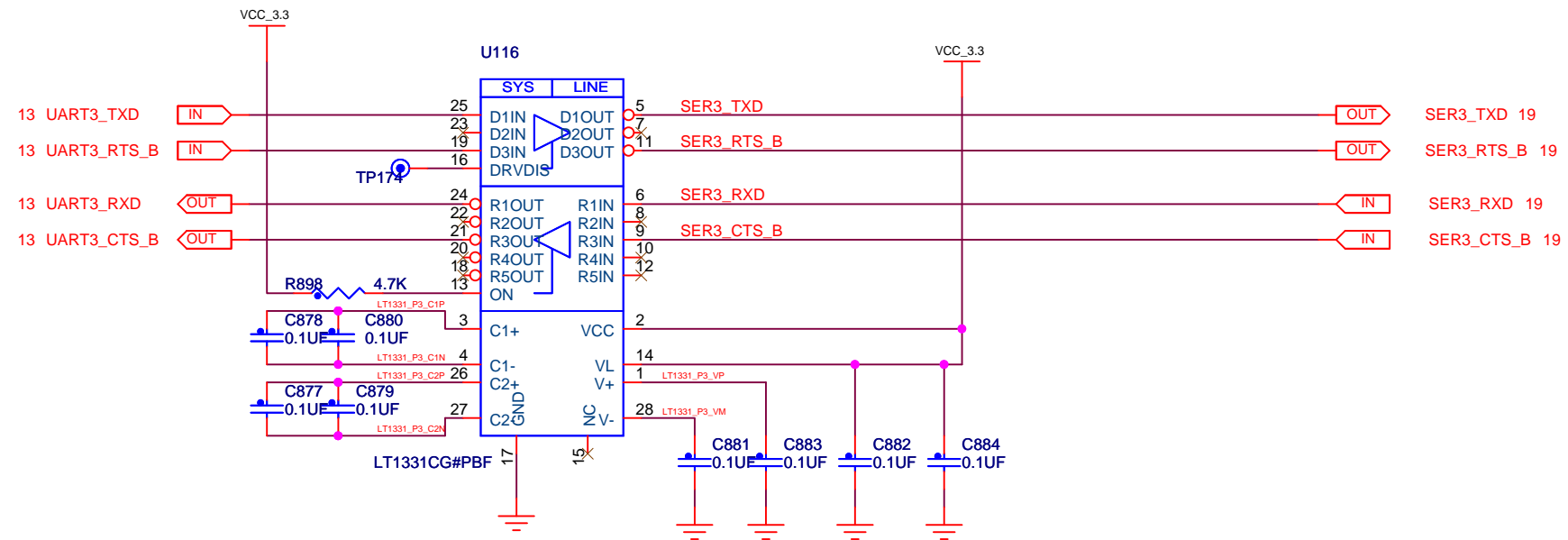




UART Port 2



UART Port 3



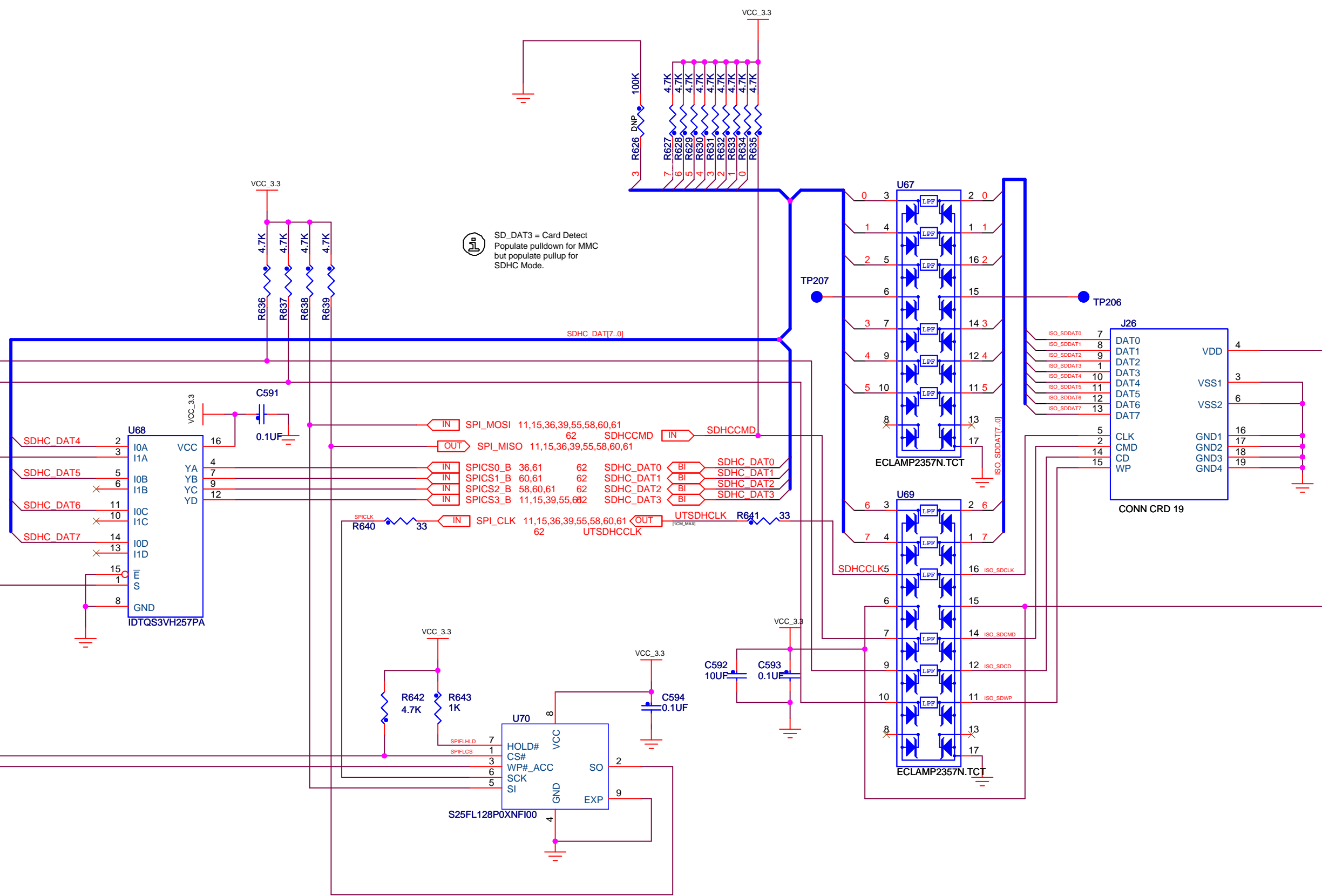
IIC3_SCL and IIC3_SDA P4080 = SDHC CD and WP, resp.

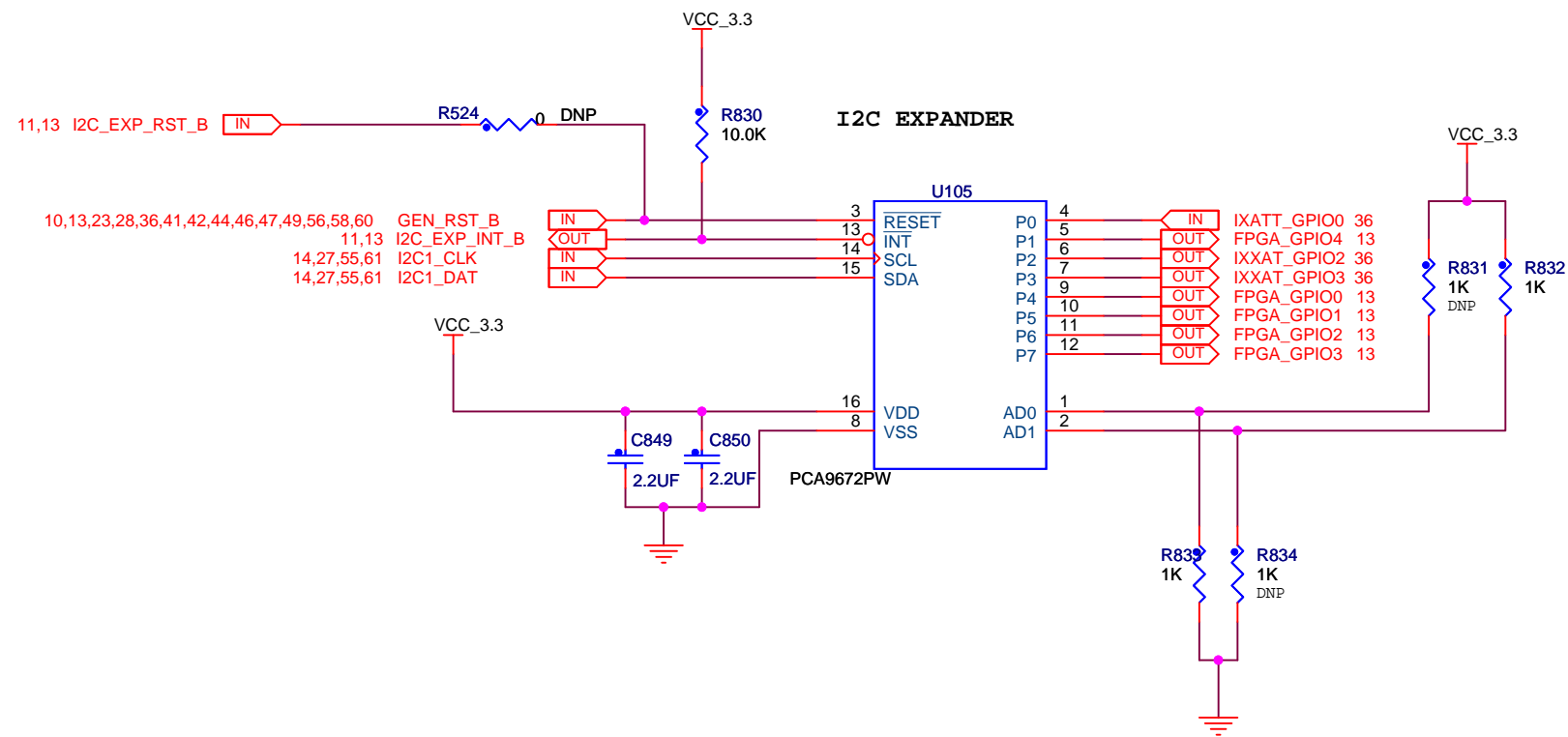
SD_DAT3 = Card Detect
Populate pulldown for MMC
but populate pullup for SDHC Mode.

62 SDHC_CD_B <OUT>
62 SDHC_WP_B <OUT>

18 CFG_SDx8MUX <IN>

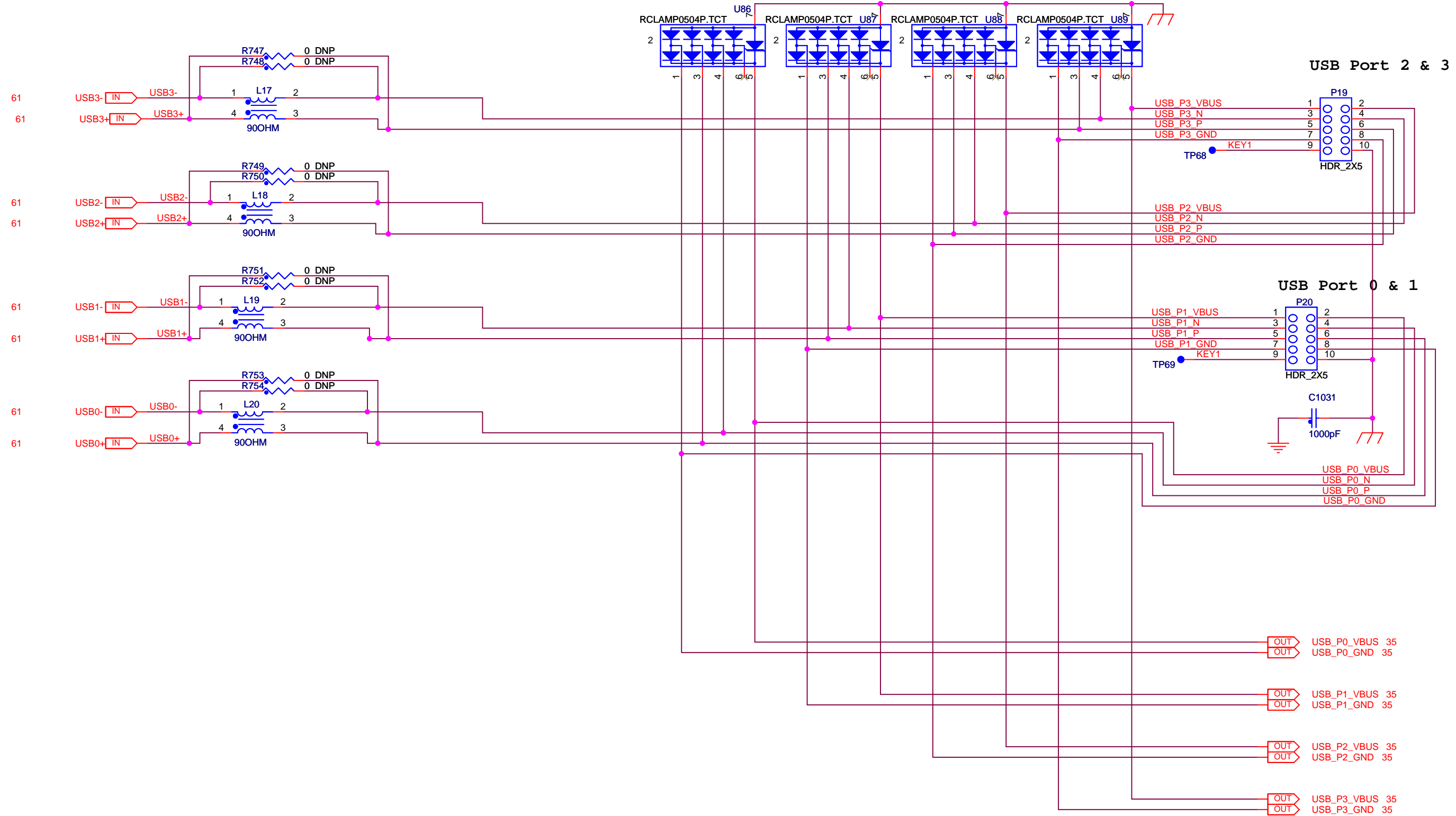
18,28 SW_FLASHWP_B <IN>



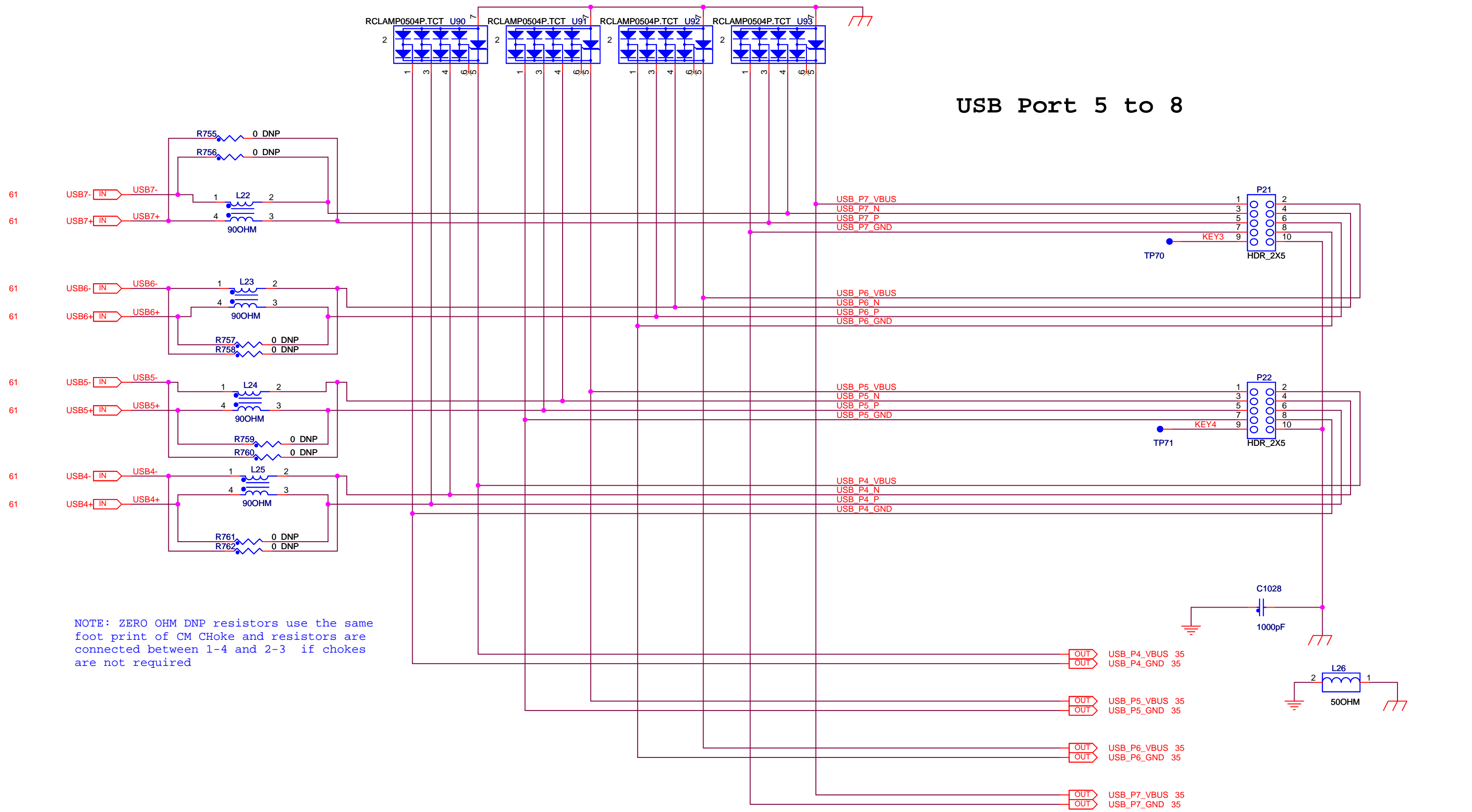


USB PORTS 1 to 4

NOTE: ZERO OHM DNP resistors use the same foot print of CM Choke and resistors are connected between 1-4 and 2-3 if chokes are not required



- OUT USB_P0_VBUS 35
- OUT USB_P0_GND 35
- OUT USB_P1_VBUS 35
- OUT USB_P1_GND 35
- OUT USB_P2_VBUS 35
- OUT USB_P2_GND 35
- OUT USB_P3_VBUS 35
- OUT USB_P3_GND 35

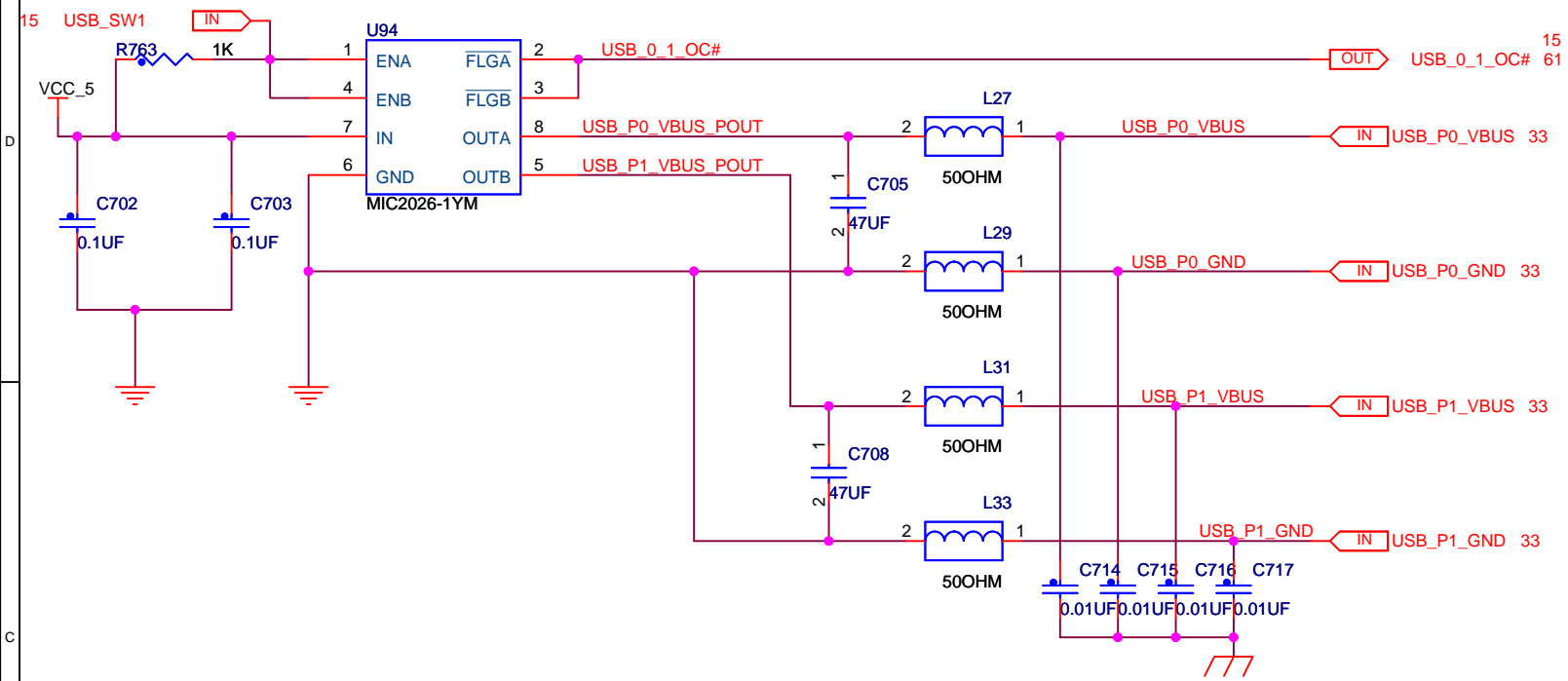


USB Port 5 to 8

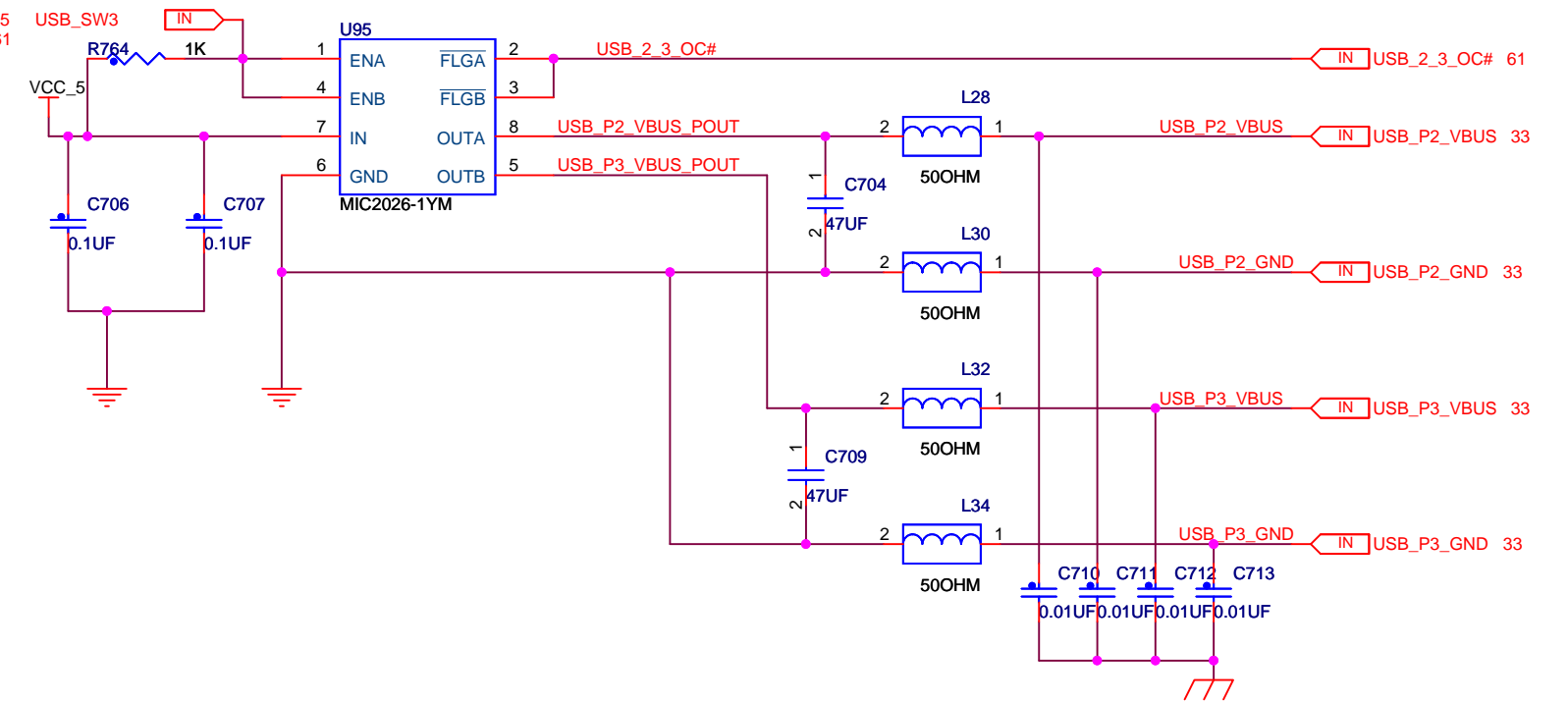
NOTE: ZERO OHM DNP resistors use the same foot print of CM Choke and resistors are connected between 1-4 and 2-3 if chokes are not required

- OUT USB_P4_VBUS 35
- OUT USB_P4_GND 35
- OUT USB_P5_VBUS 35
- OUT USB_P5_GND 35
- OUT USB_P6_VBUS 35
- OUT USB_P6_GND 35
- OUT USB_P7_VBUS 35
- OUT USB_P7_GND 35

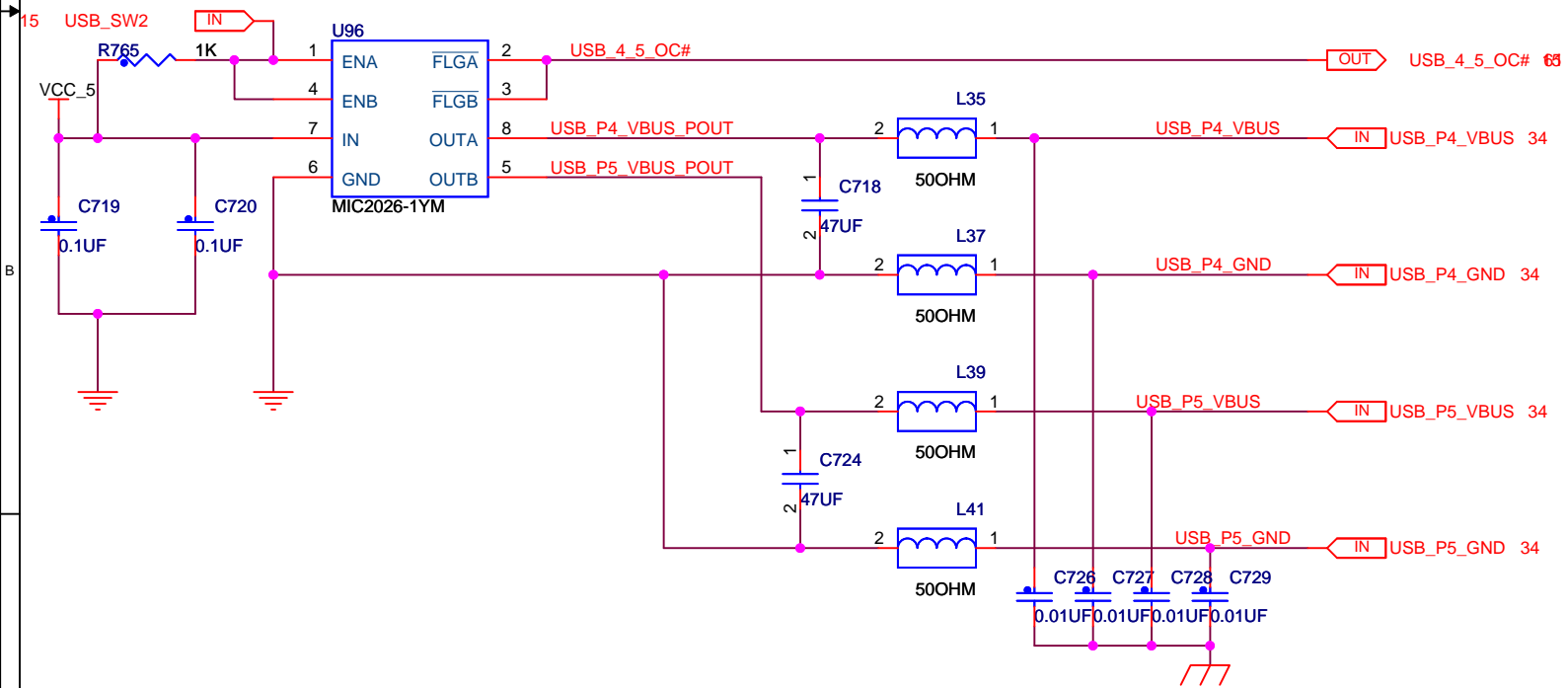
Power Switch for Port 0 & 1



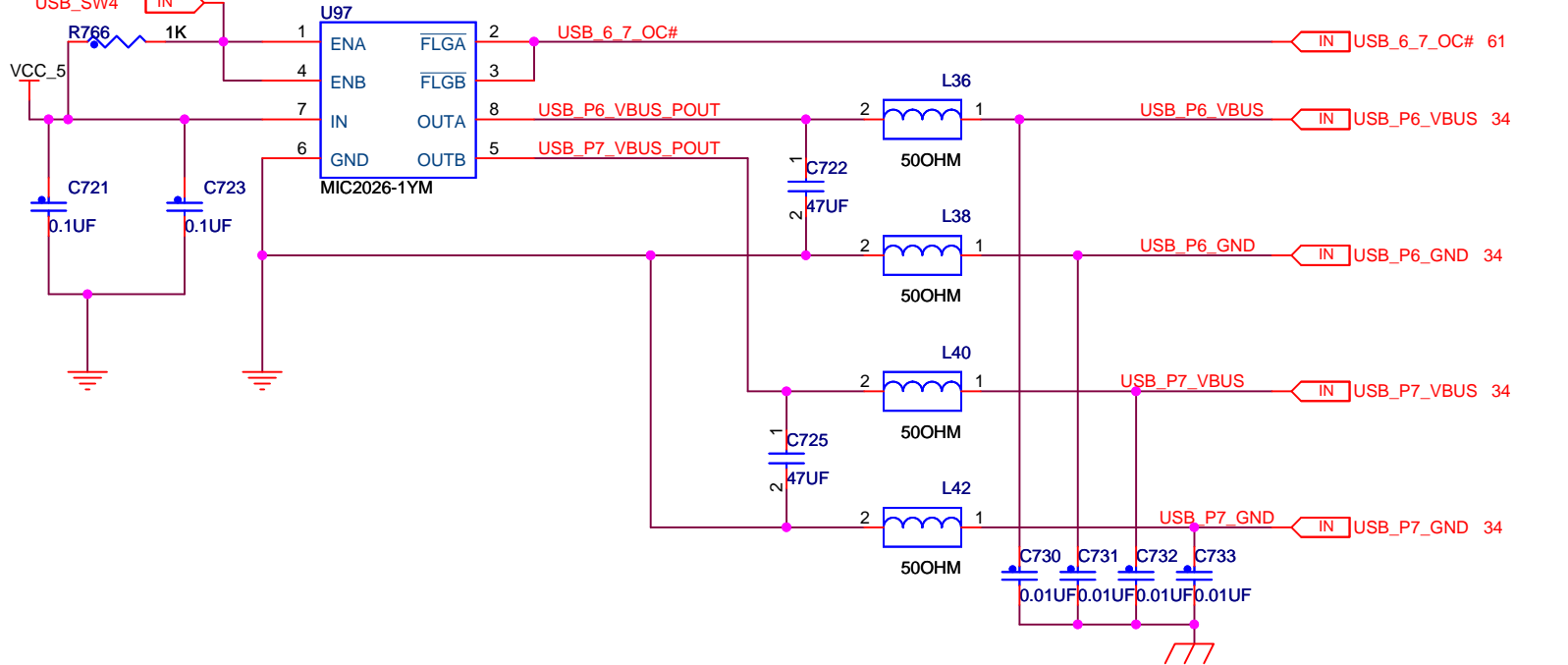
Power Switch for Port 2 & 3



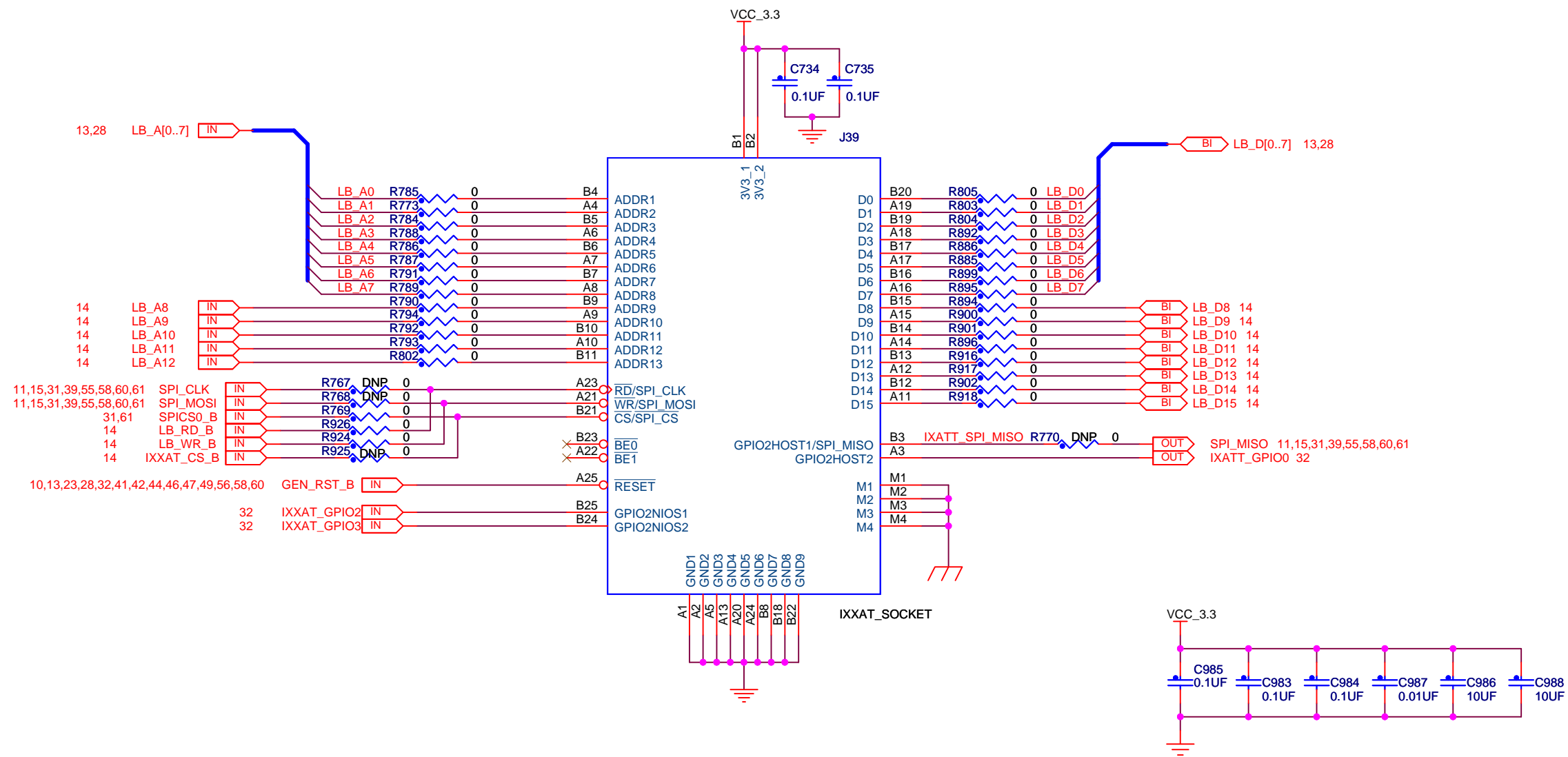
Power Switch for Port 4 & 5

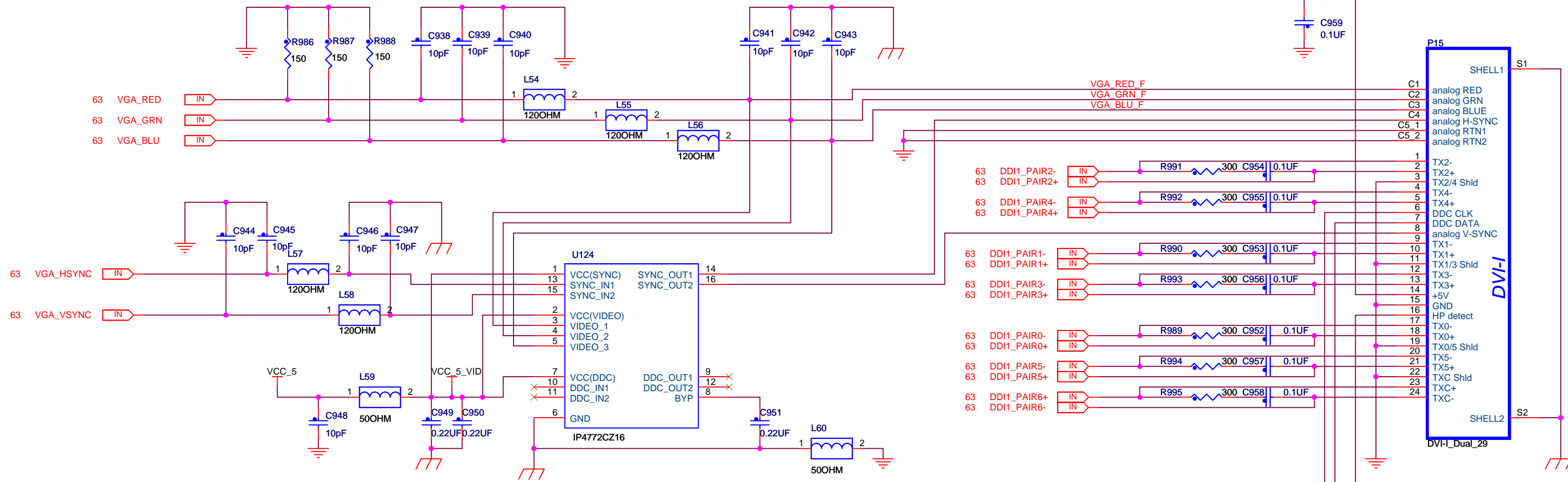


Power Switch for Port 6 & 7



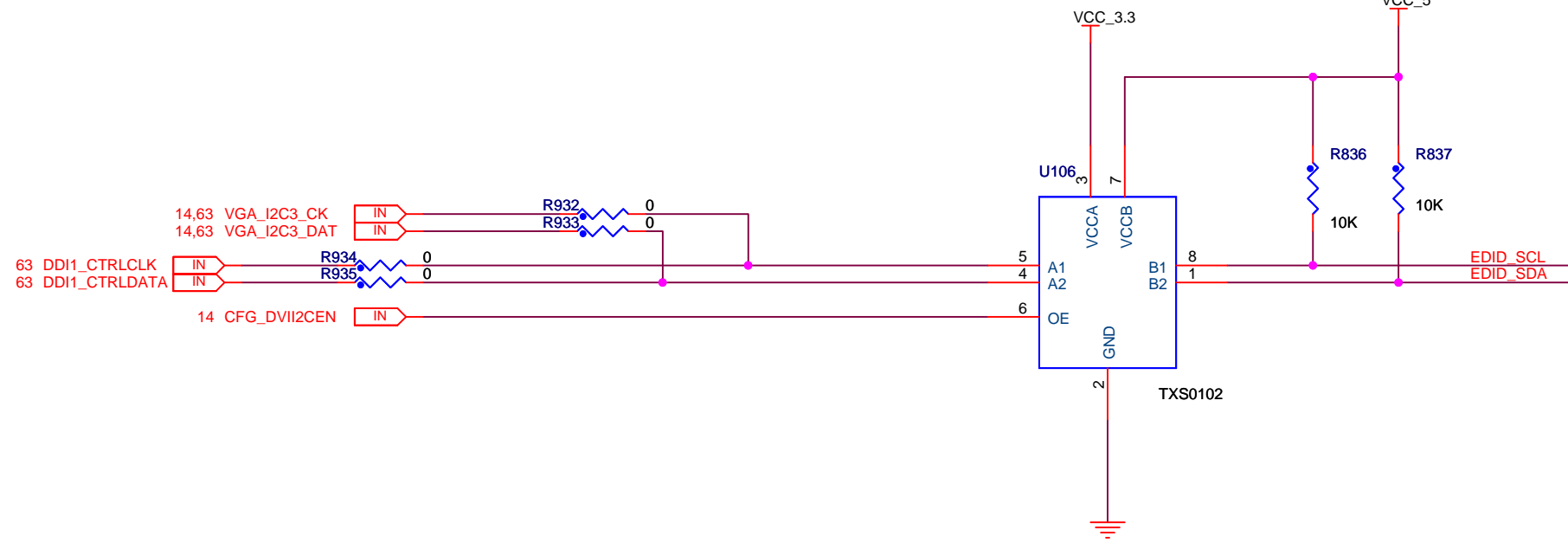
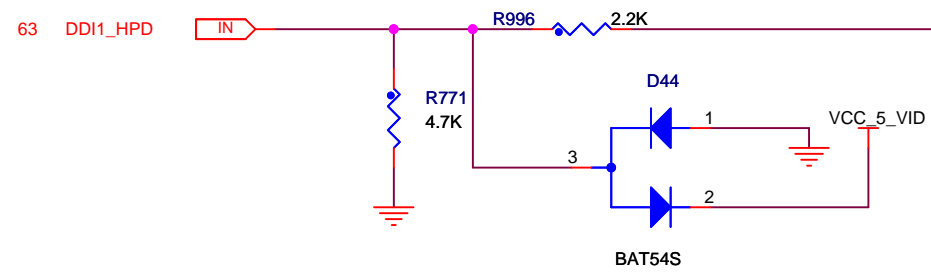
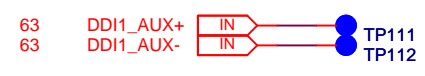
IEM Module

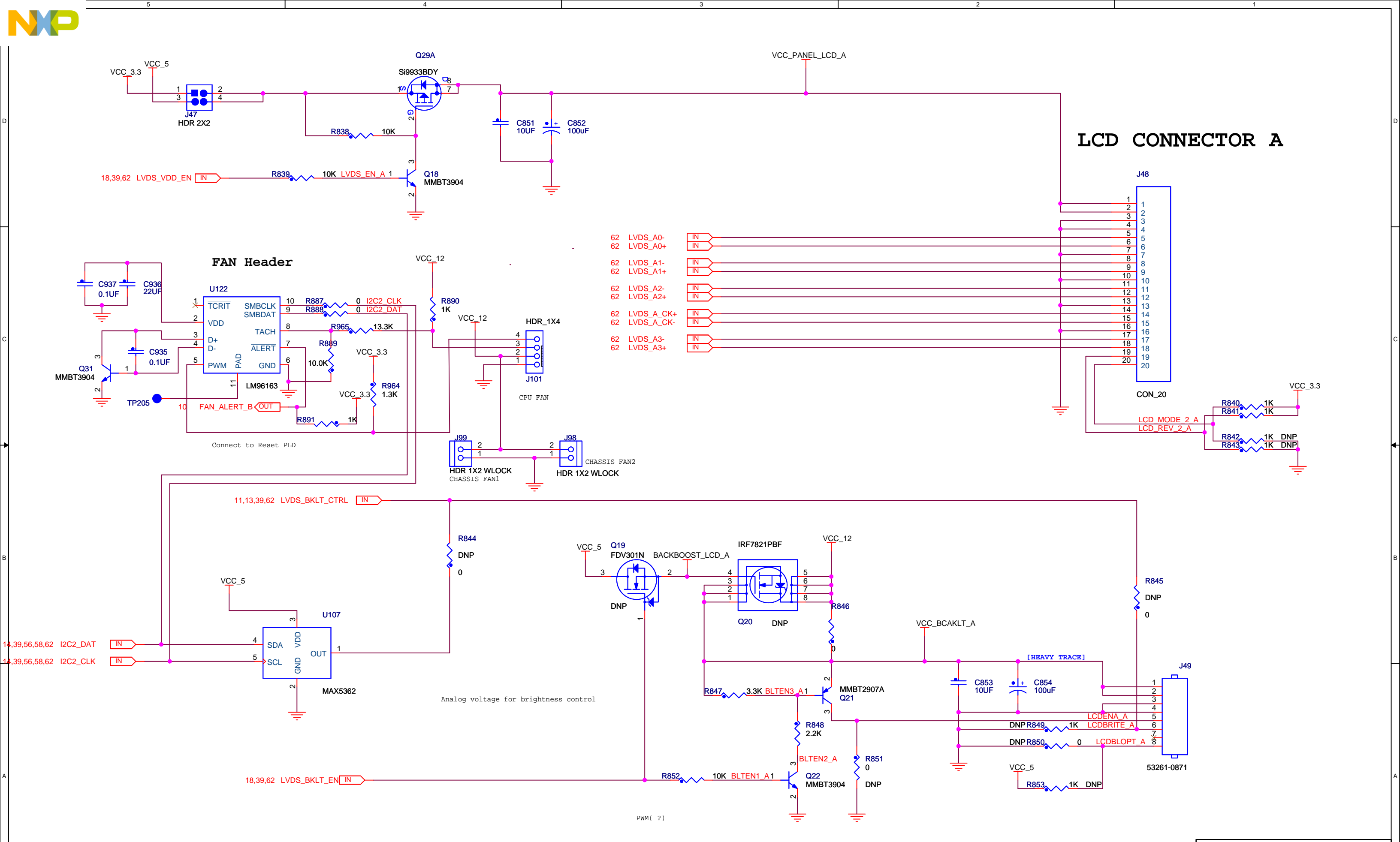


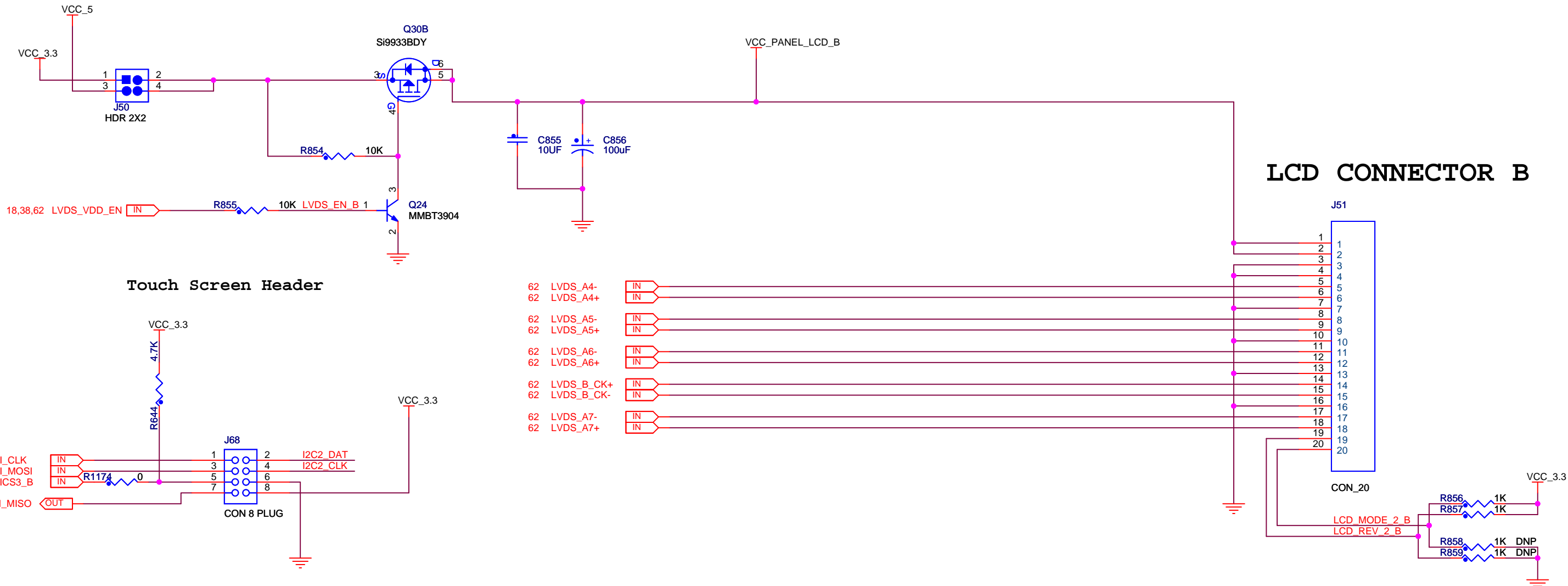


ESD Protection buffer

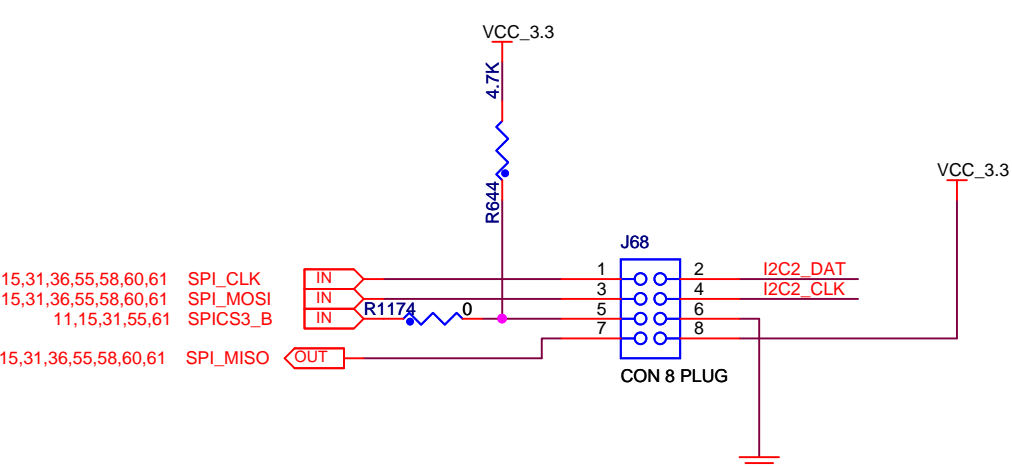
DVI_VGA Connector



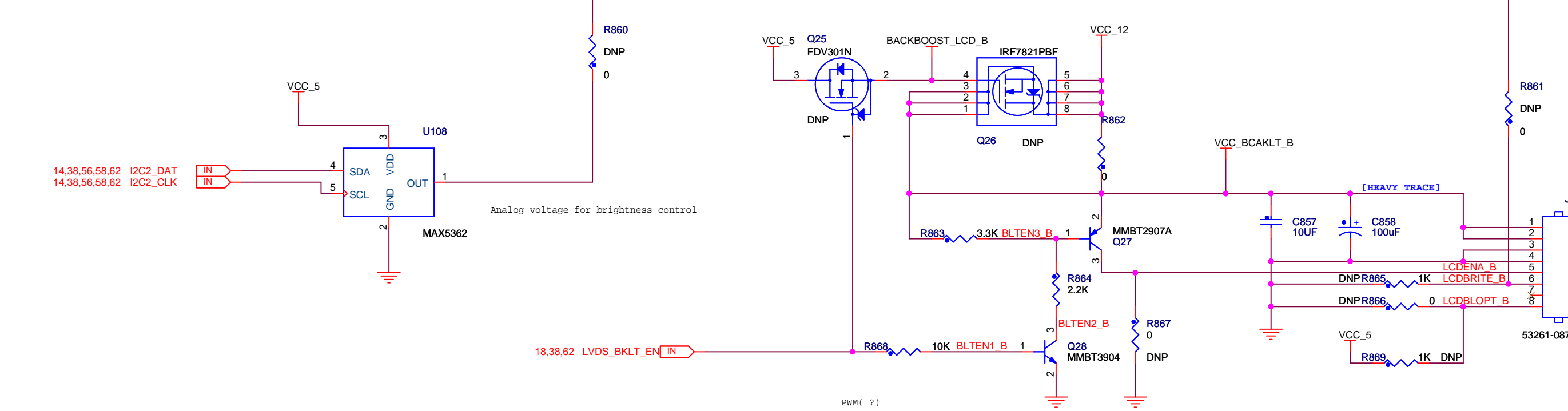




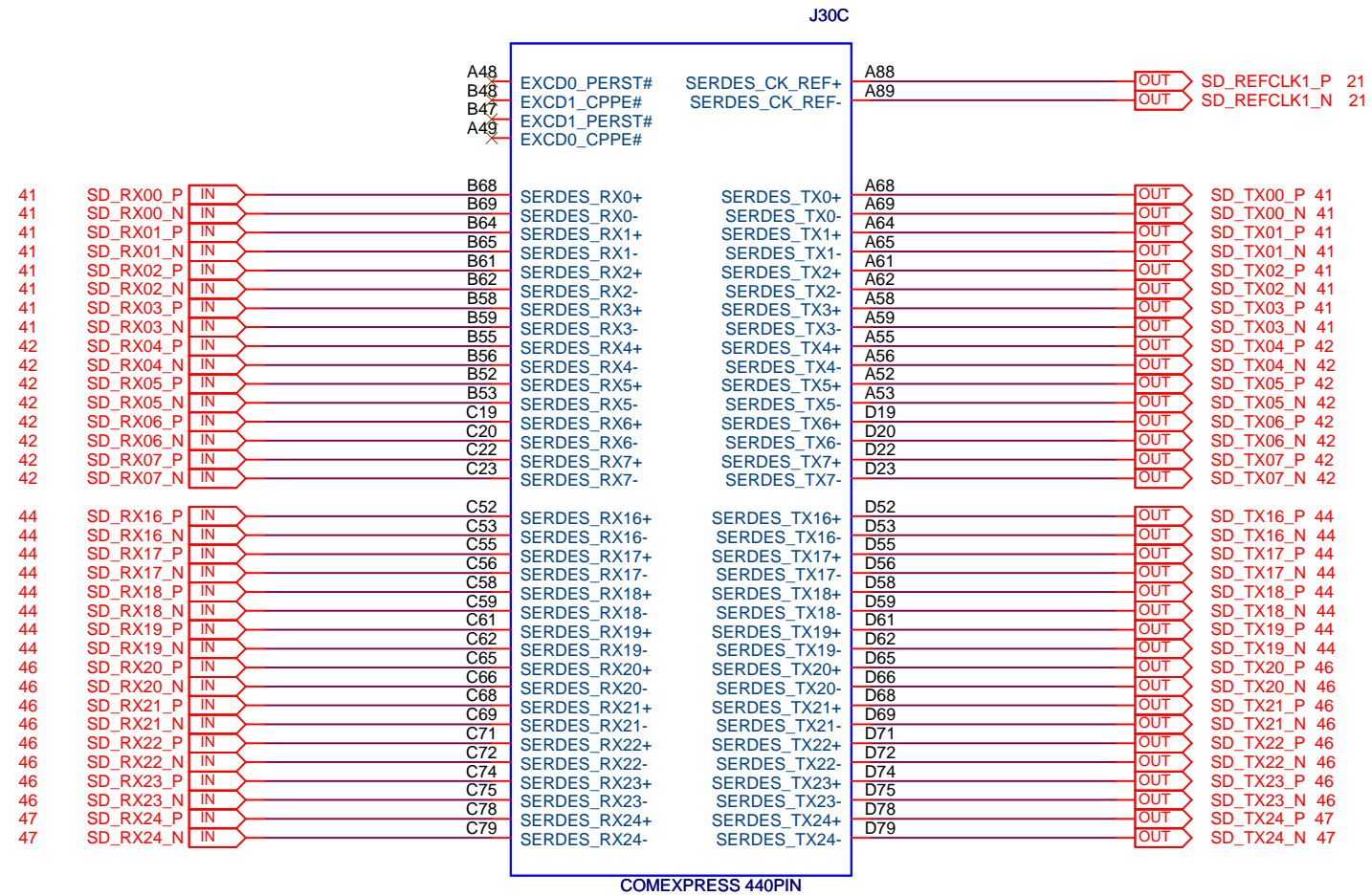
Touch Screen Header



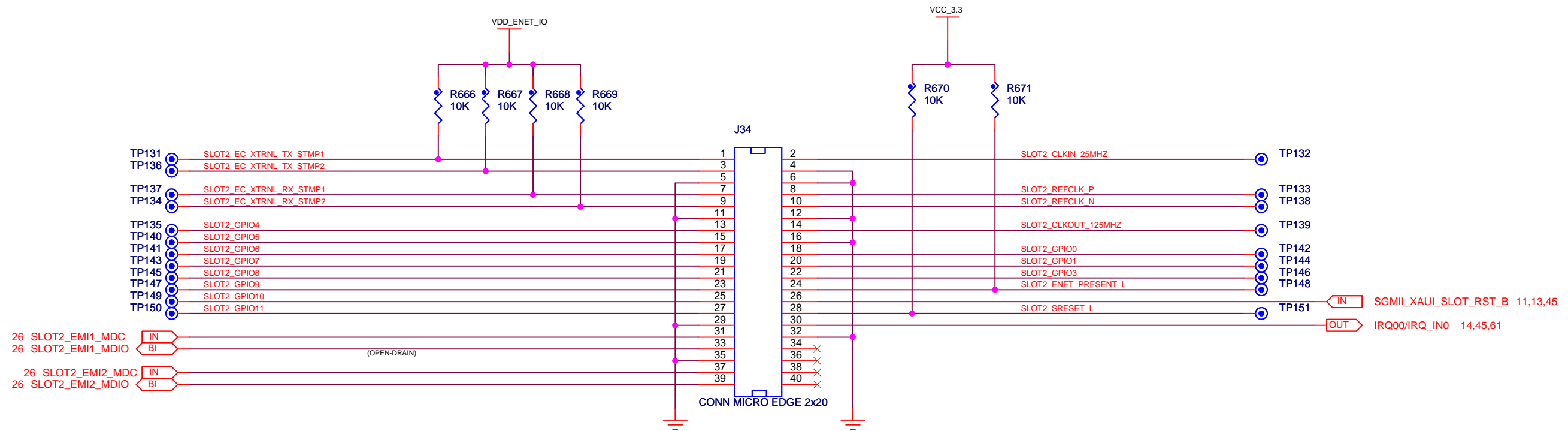
LVDS_BKLT_CTRL



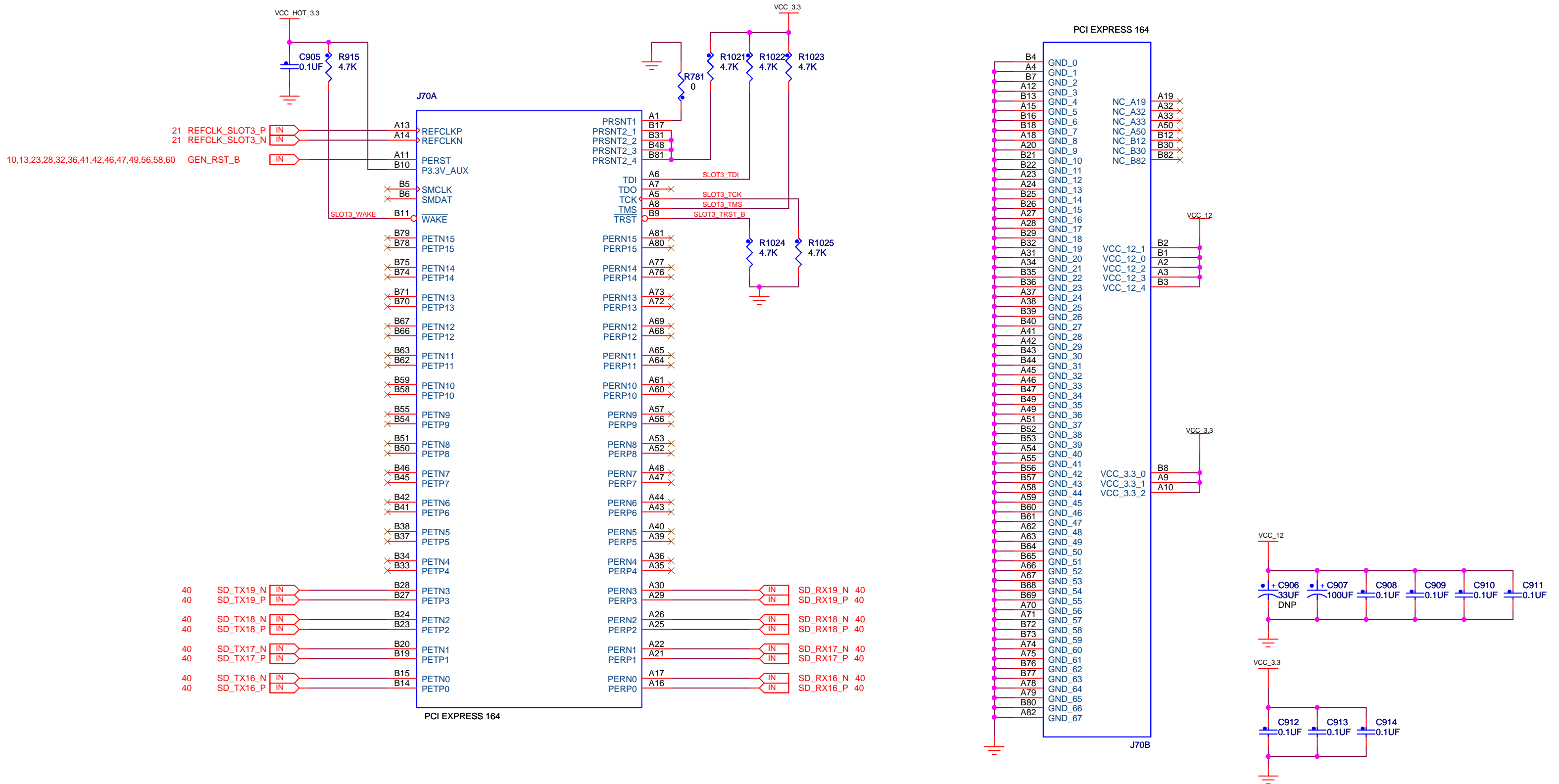
SERDES - COMe CONNECTOR



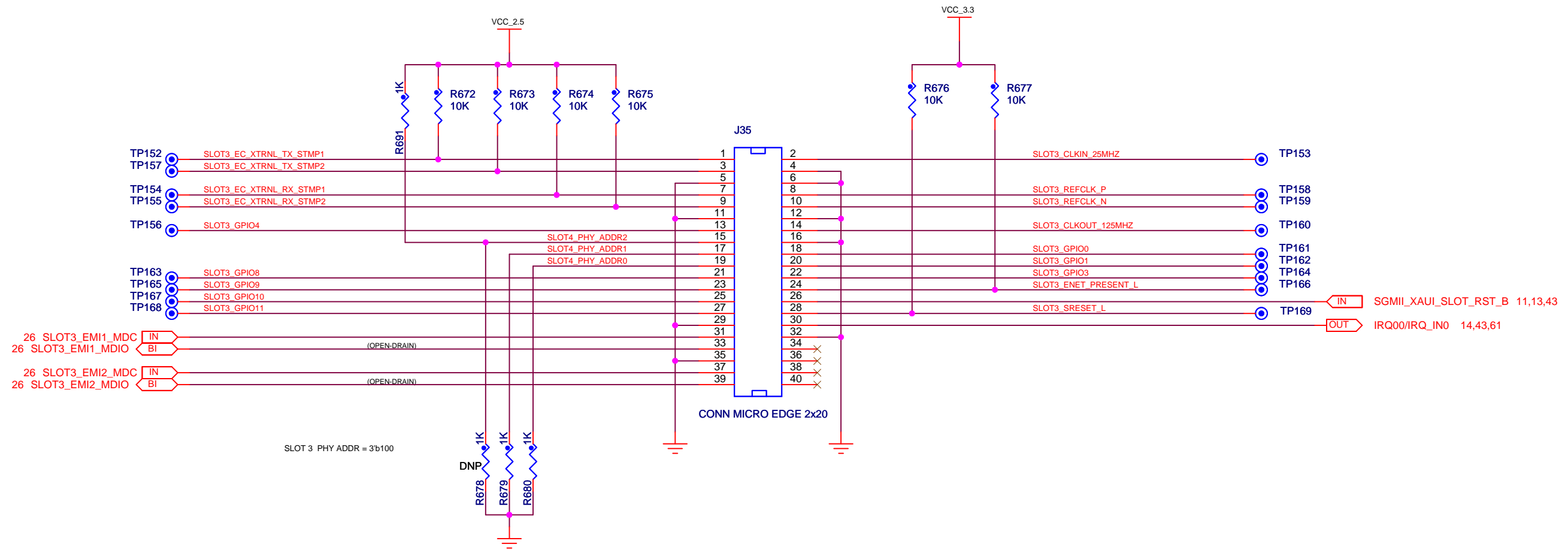
SLOT 2 (PEX/SGMII) SIDEBAND (PART 2 OF 2) CONNECTOR

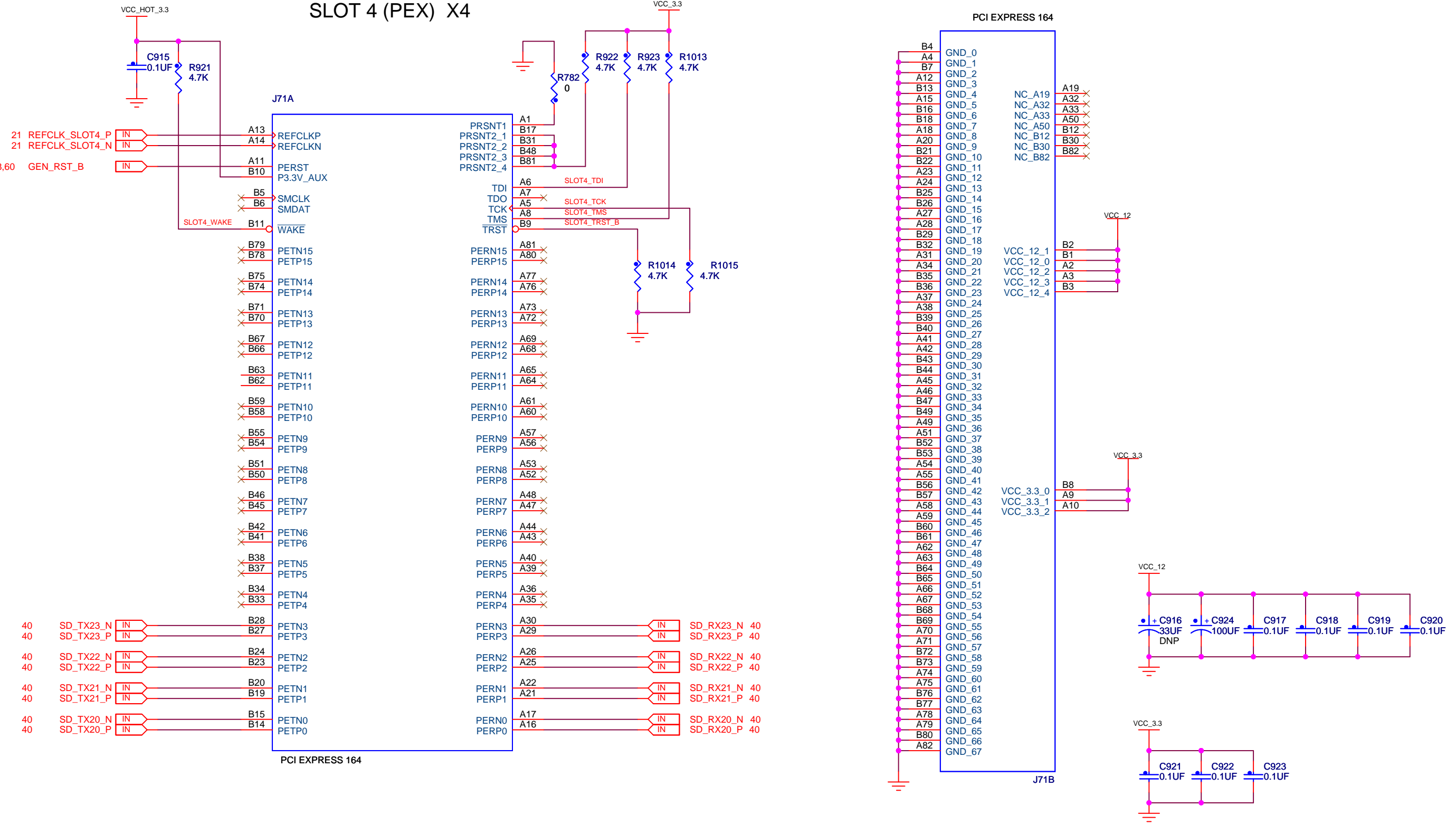


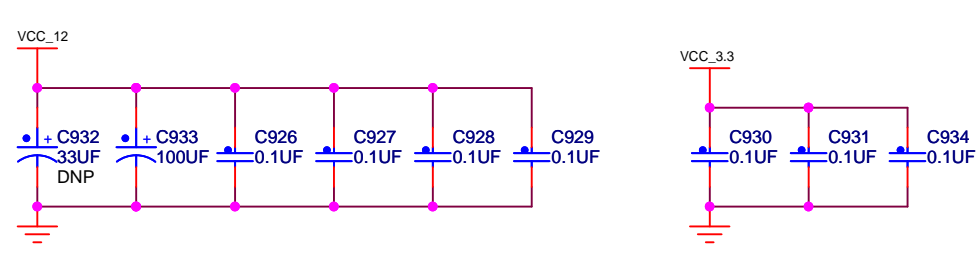
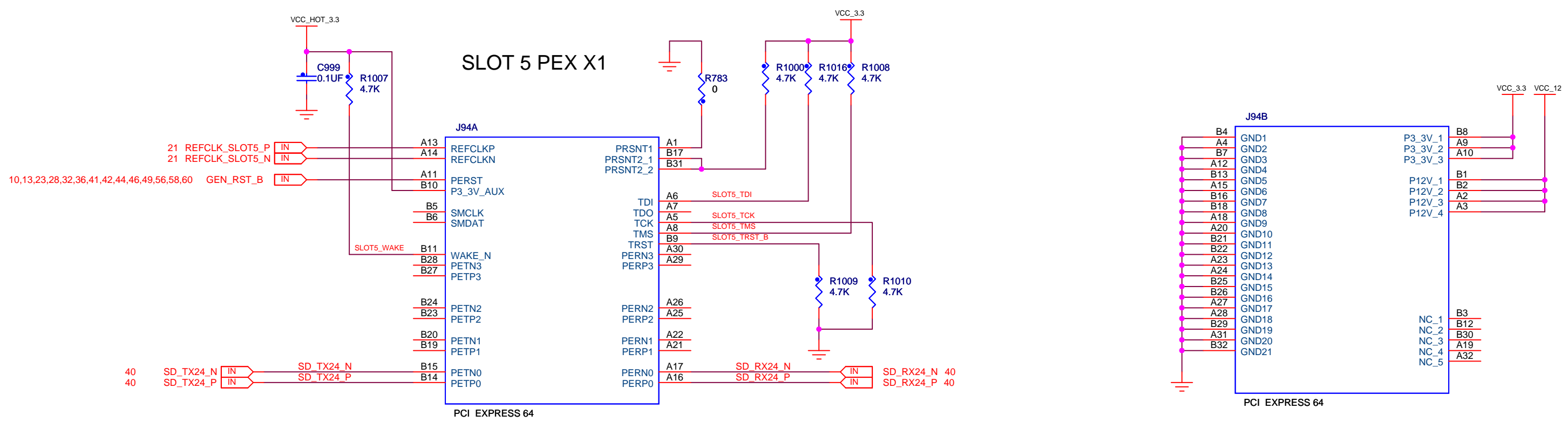
SLOT 3 (XAUI/SGMII) MAIN (PART 1 OF 2) CONNECTOR



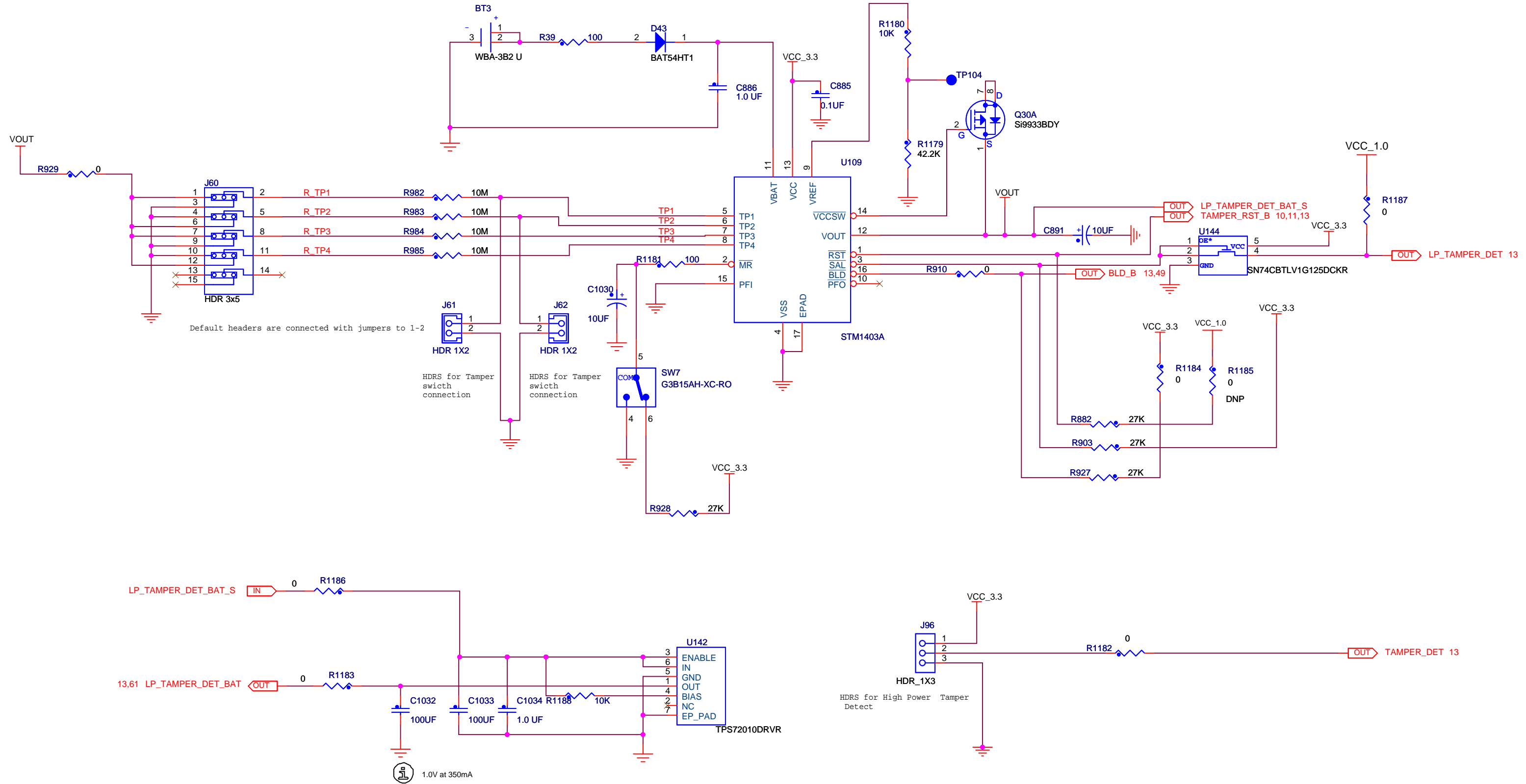
SLOT 3 (XAUI/SGMII/SRIO) SIDEBAND (PART 2 OF 2) CONNECTOR



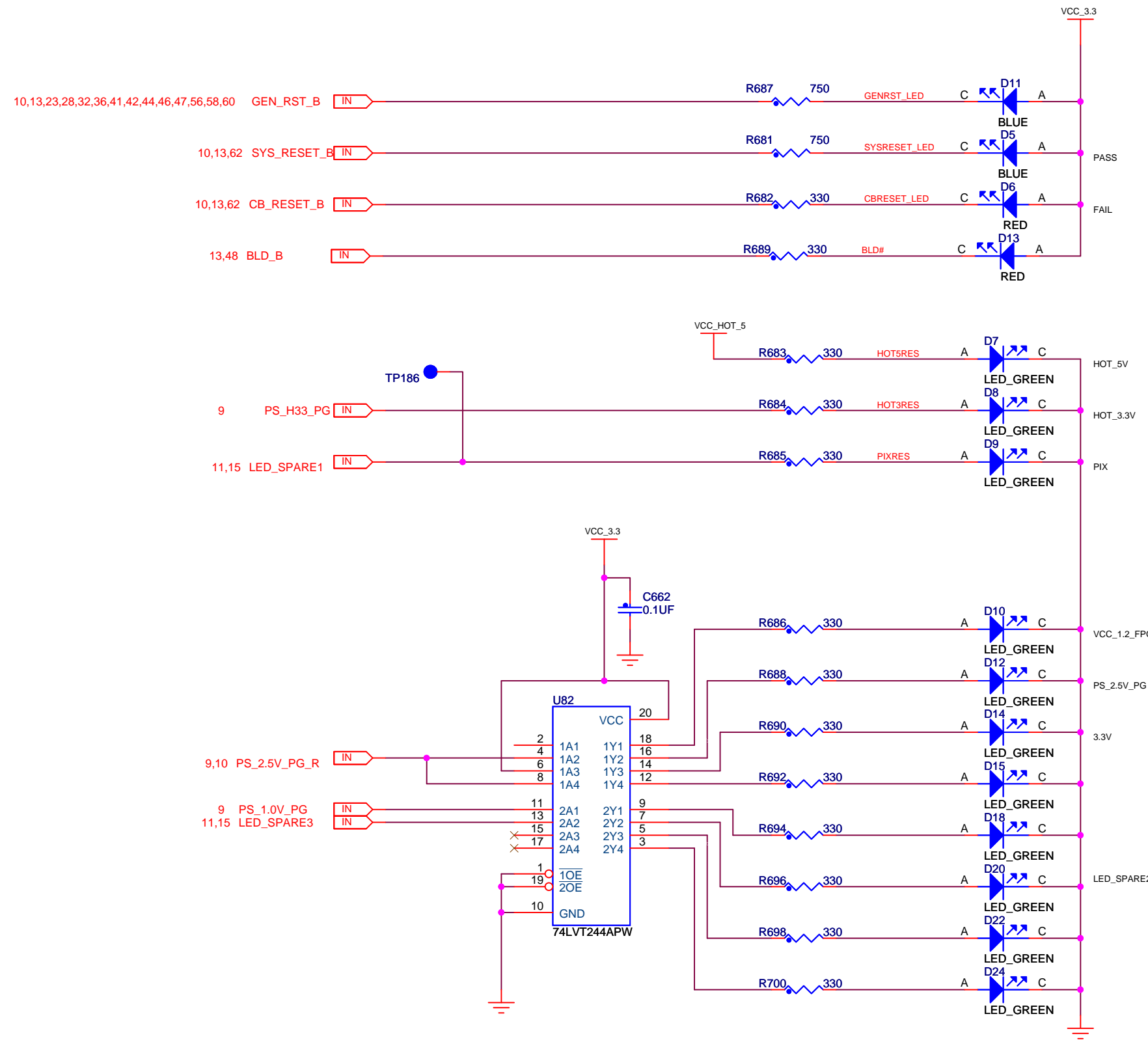




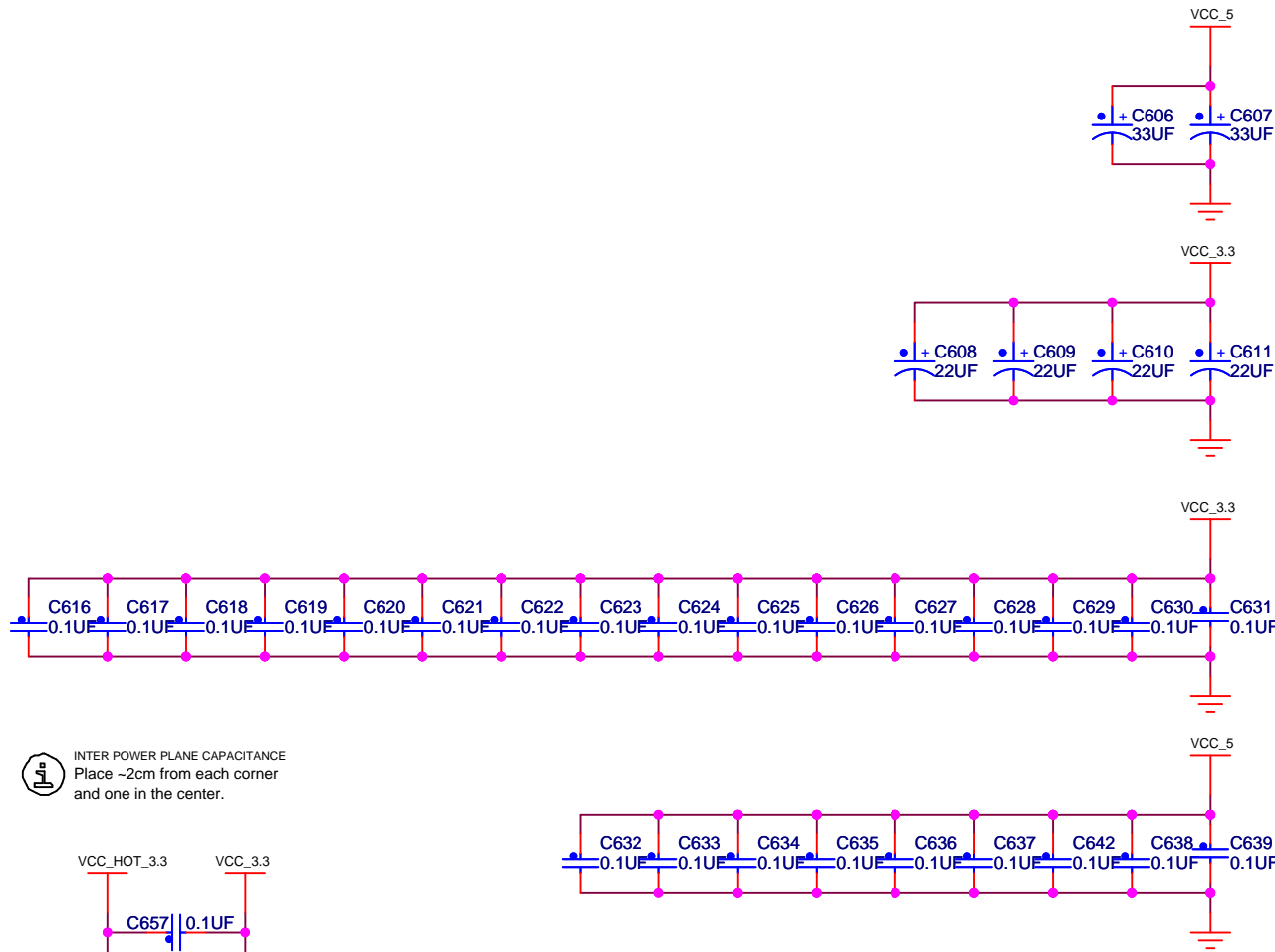
TAMPER DETECT INTERFACE



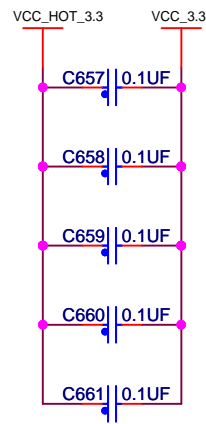
DEBUG LED INDICATION



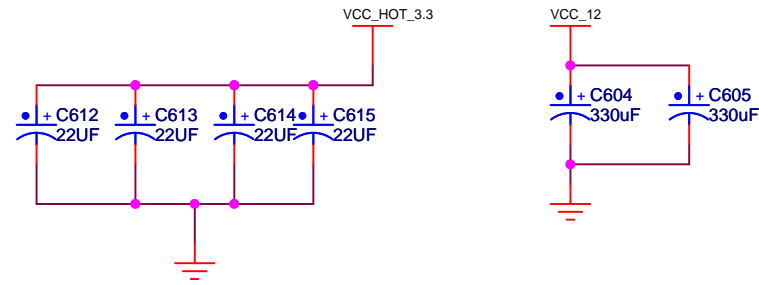
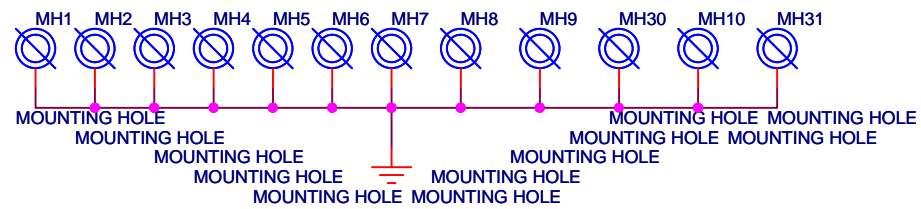
DECOUPLING CAPACITORS



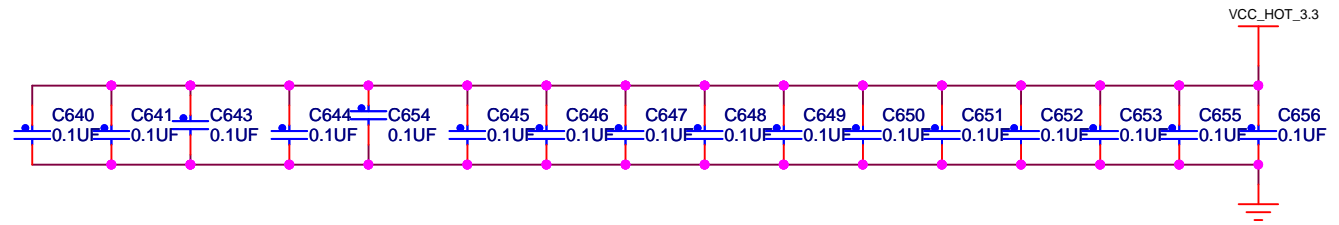
INTER POWER PLANE CAPACITANCE
Place ~2cm from each corner and one in the center.



CHASSIS MOUNTING HOLES
ATX Chassis: 10 holes.

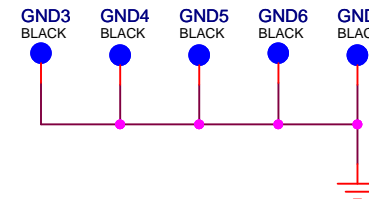


GLOBAL HF CAPACITANCE
Place in a grid ~5cm everywhere.

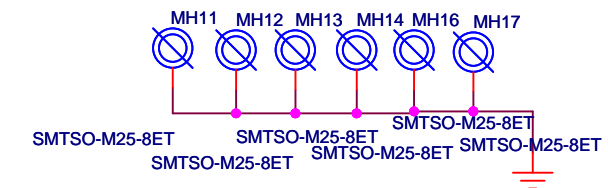


ATX Chassis: 11standoffs holes.

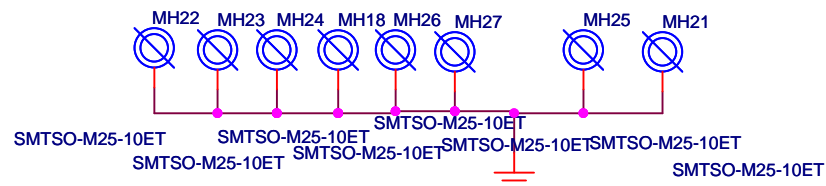
GROUND TEST POINTS
Place in each corner and center



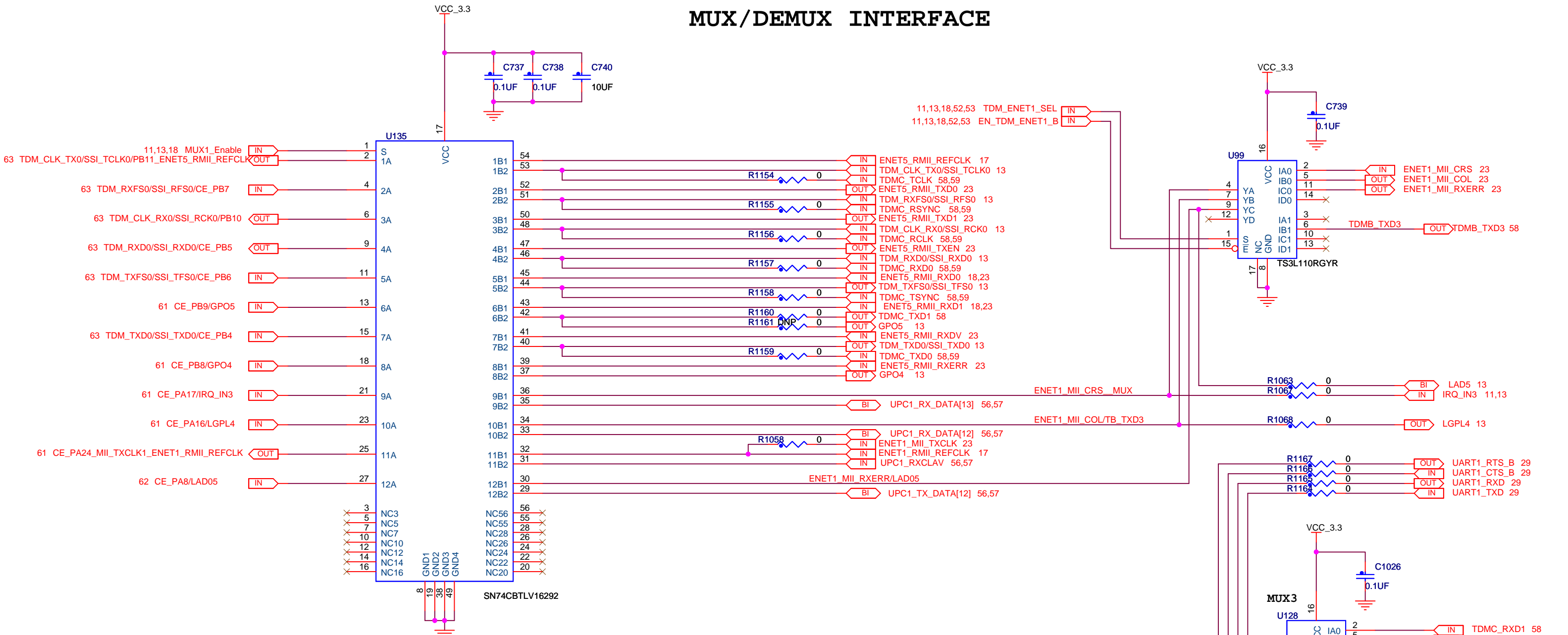
11 STANDOFFS MOUNTING HOLES FOR COMe MODULES



8 STANDOFFS MOUNTING HOLES FOR PMC CARDS 0 & 1



MUX/DEMUX INTERFACE



Note : After Demux

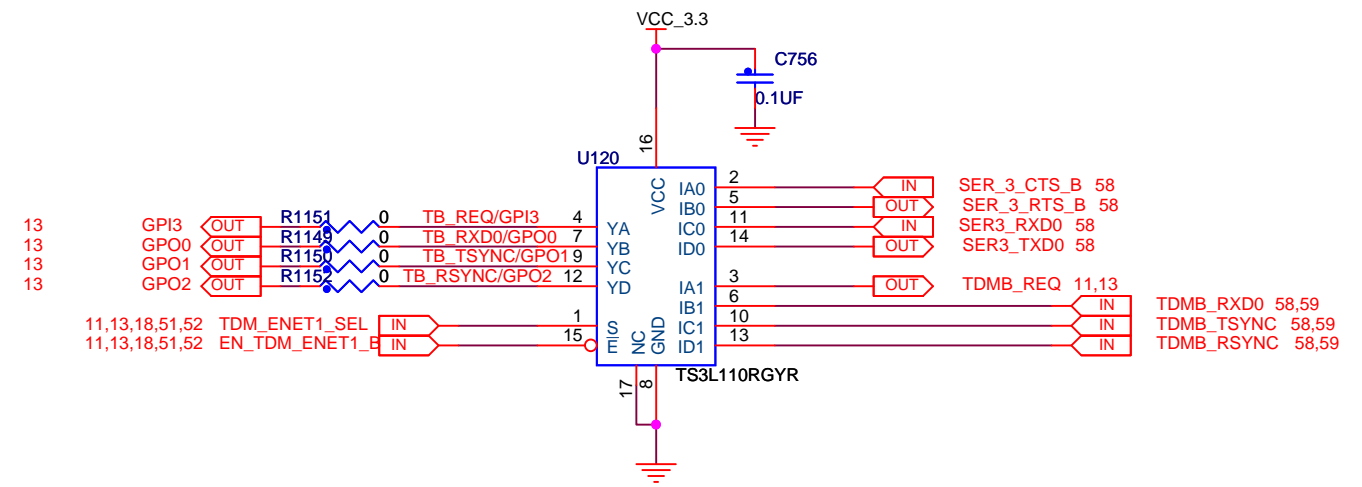
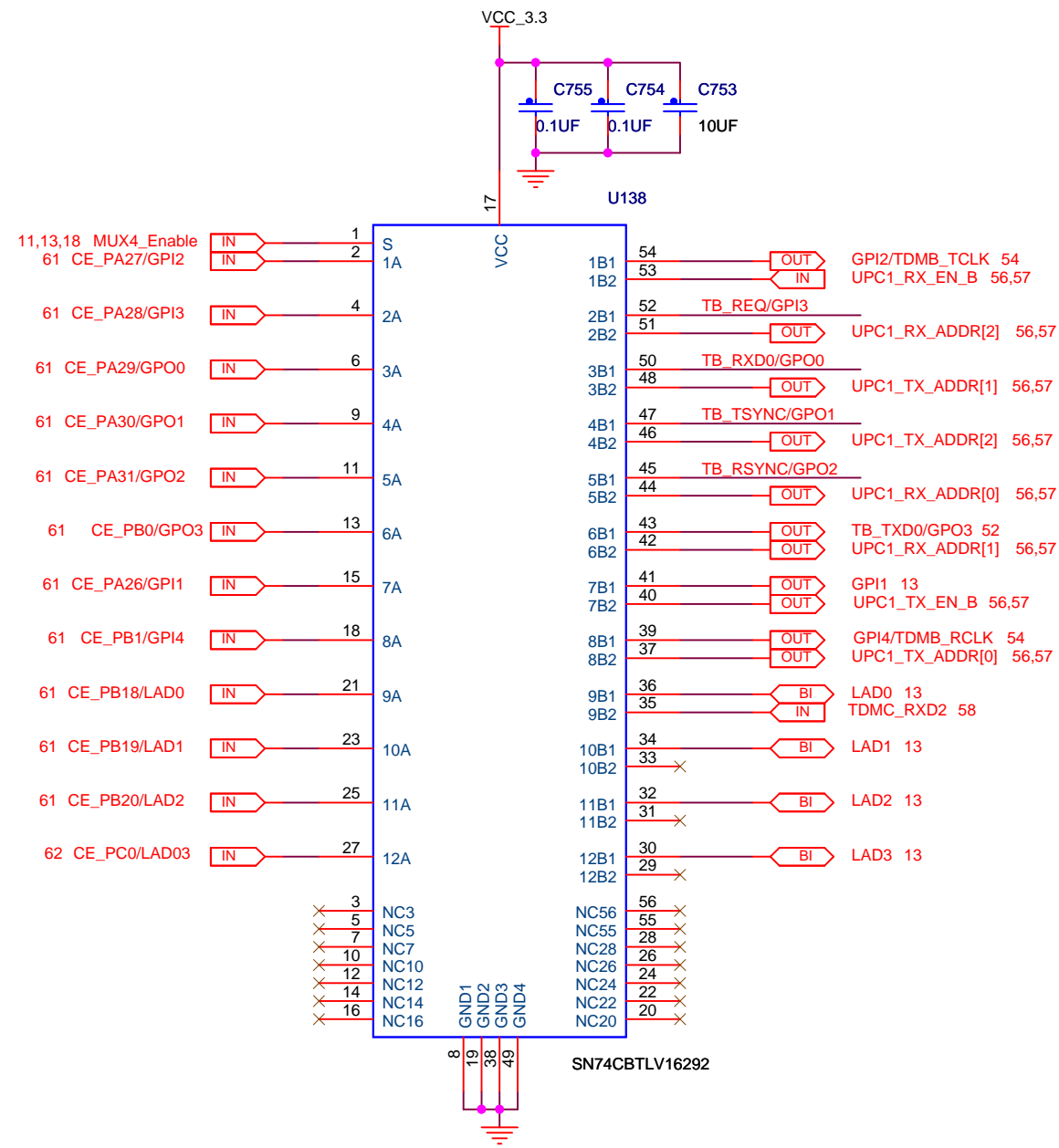
- TDMB - Interfaced to PMC HDLC
- TDMC - Interfaced to TDM RISER, PMC HDLC
- TDMD - Interfaced to PMC HDLC
- TDM/SSI - Interfaced to FPGA
- Local bus, GPIO, INTR - Interfaced to FPGA
- UART1 - Interfaced to Transceiver
- UTOPIA - Interfaced to PMC connector
- Ethernet1, 5 - Interfaced to PHY

After Mux

All Signals - Interfaced to COMe connector

	MUX1_Enable		TDM ENET1_SEL		EN TDM ENET1_B	
	Low	High	Low	High	Low	High
ENET5_RMII	*					
ENET1_RMII	*		*		*	
TDMB(NIBBLE)	*			*	*	
TDMC(Nibble)		*	*		*	
TDMD(Serial)				*	*	
UTOPIA		*				
GPIO		*				
LBC	*					
INTR	*					

MUX/DEMUX INTERFACE



Note : After Demux

- SER3 - Interfaced to PMC HDLC
- Local bus, GPIO - Interfaced to FPGA
- UTOPIA - Interfaced to PMC connector
- TDMB - Interfaced to PMC HDLC
- TDMC - Interfaced to PMC HDLC

After Mux

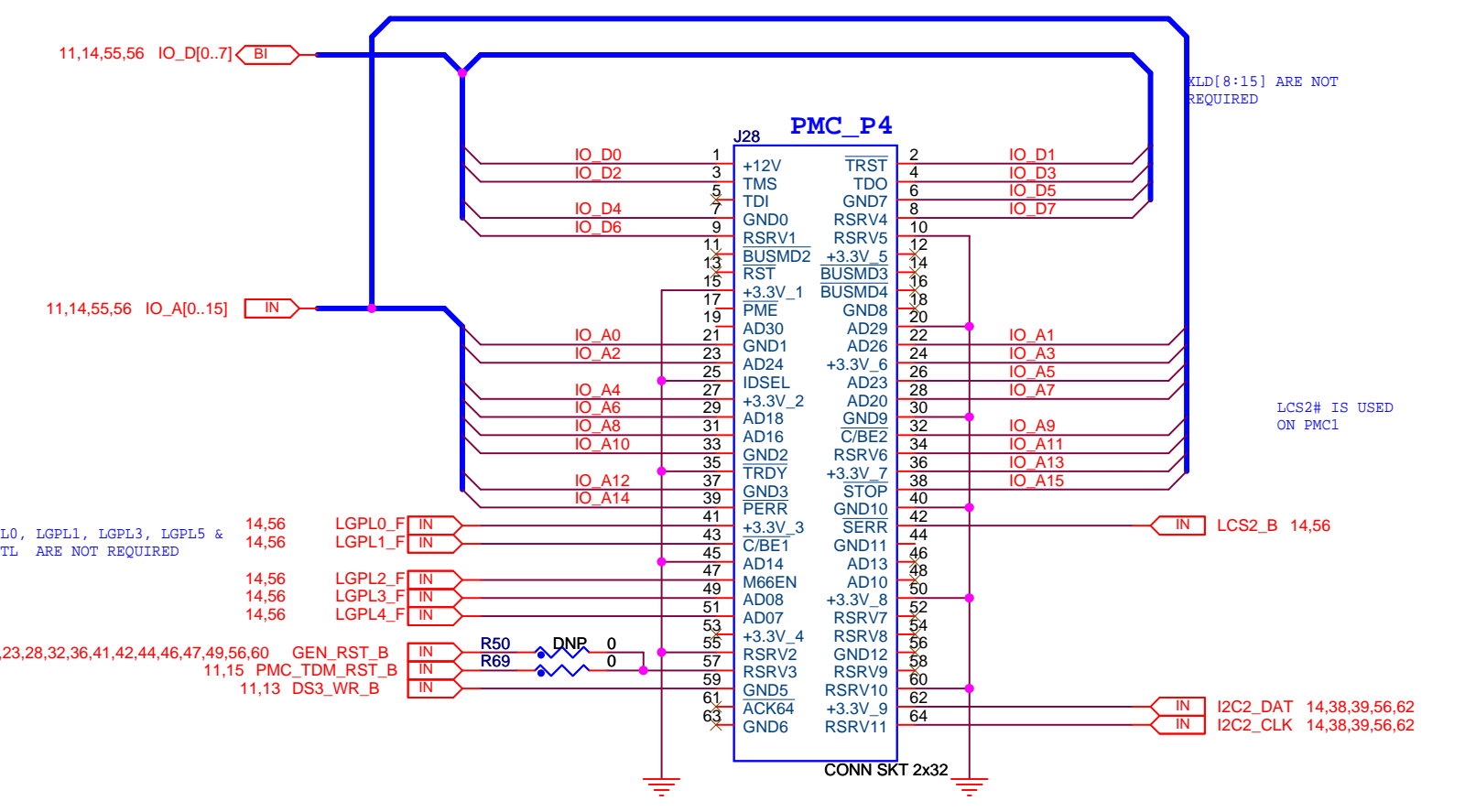
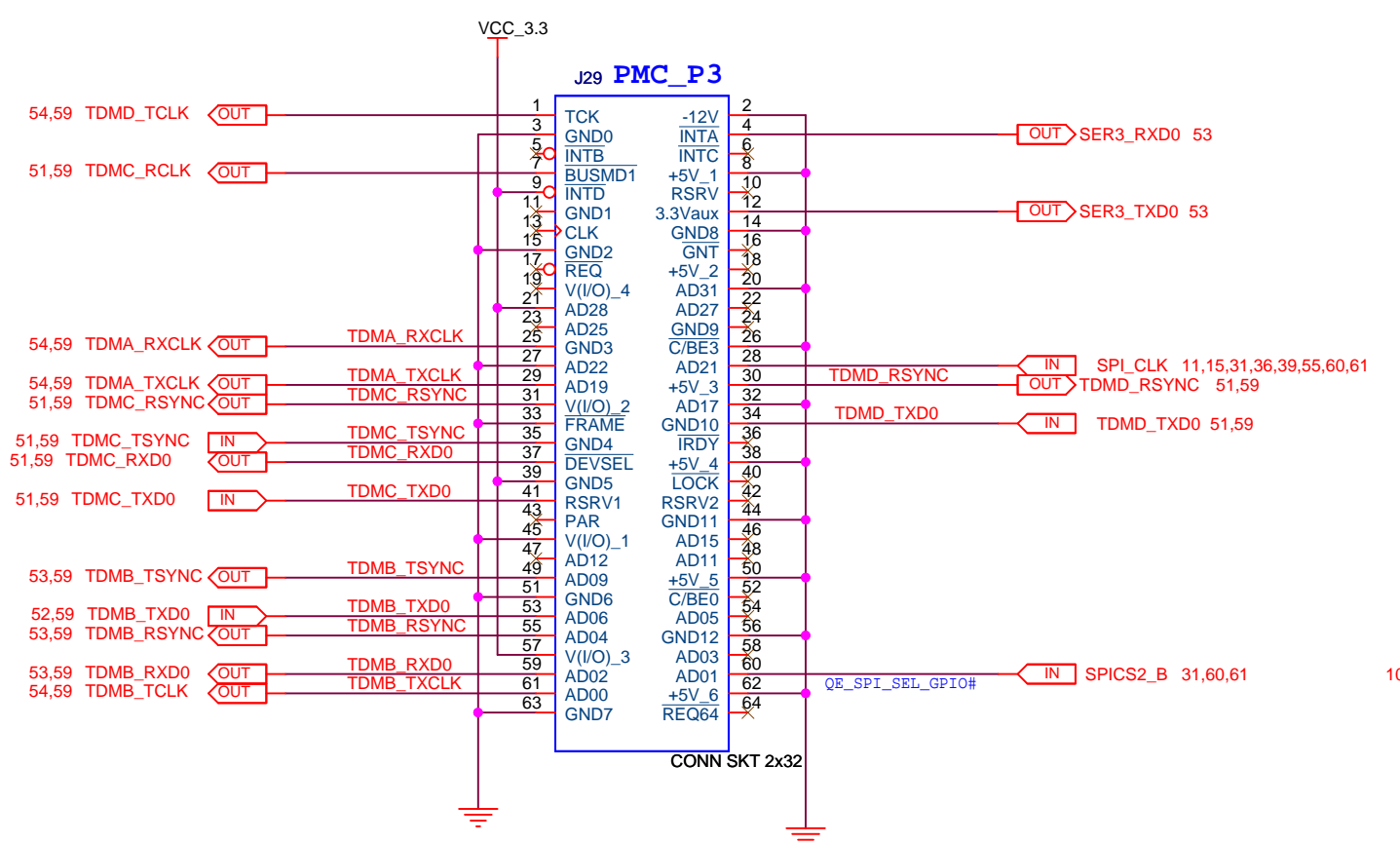
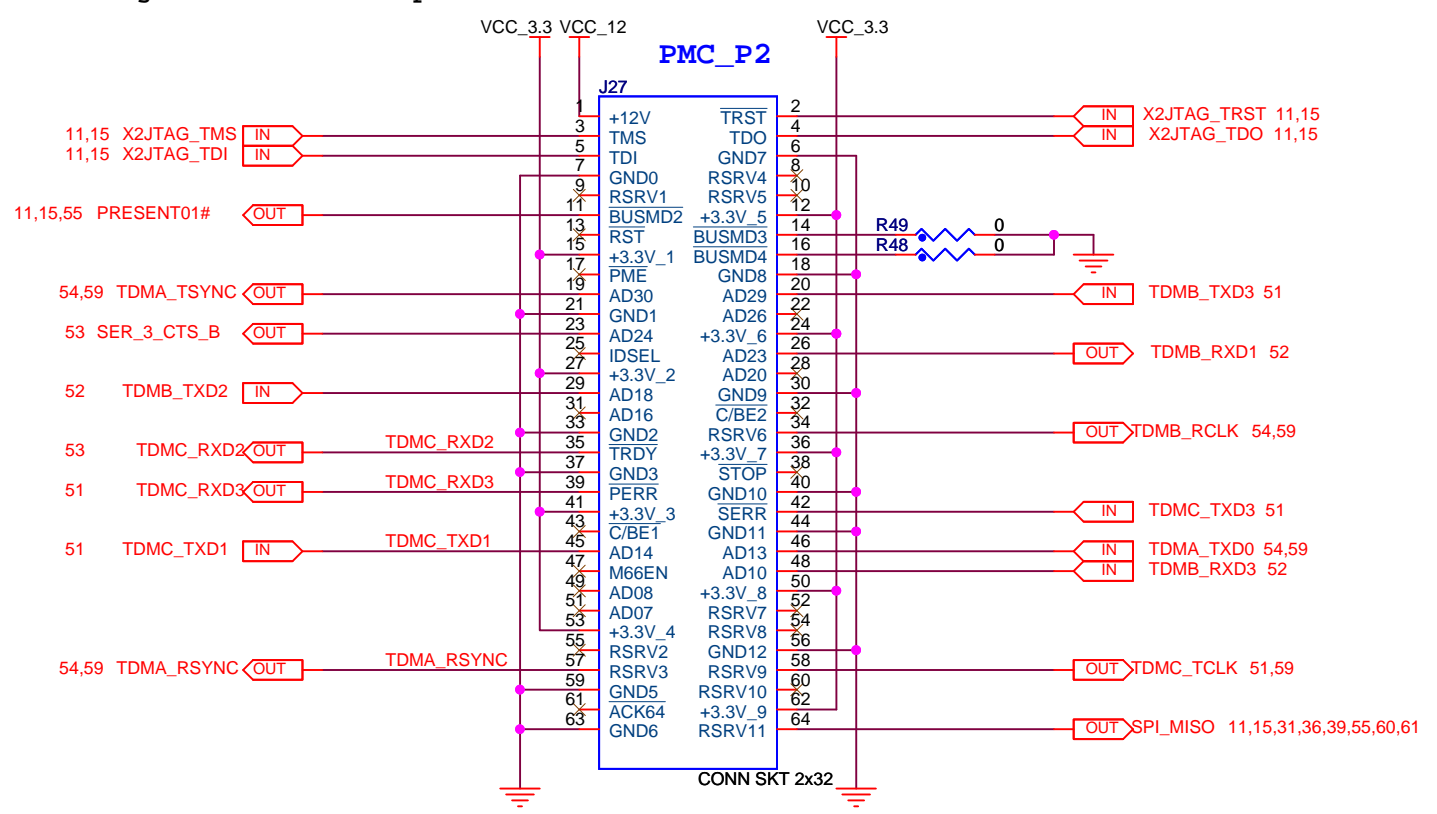
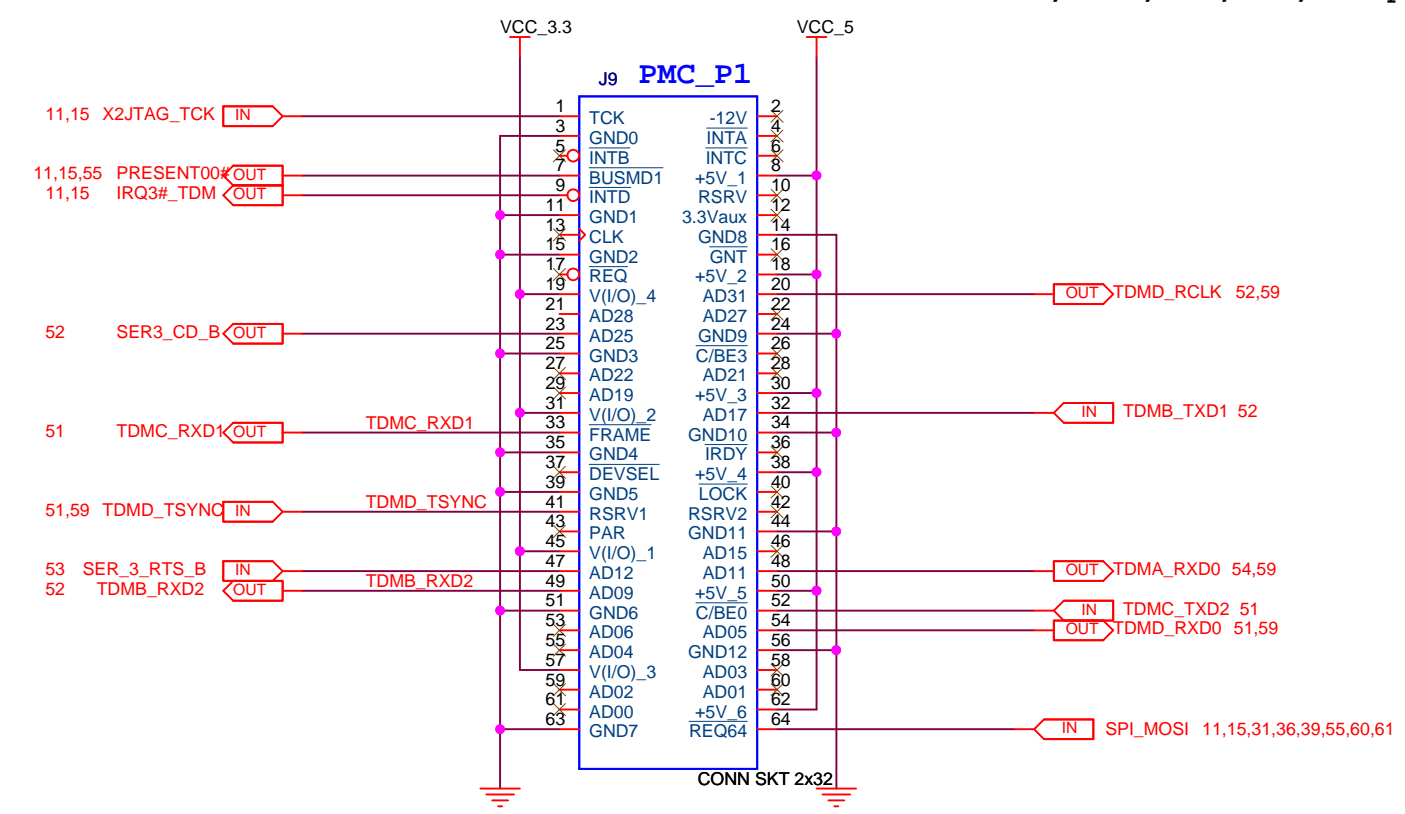
All Signals - Interfaced to COME connector

	MUX3_Enable		TDM_ENET1_SEL		EN_TDM_ENET1_B	
	Low	High	Low	High	Low	High
SER3	*		*		*	
TDMB (NIBBLE)	*			*	*	
UTOPIA		*				
GPIO/INTR	*			*	*	
LBC	*					
TDMC		*				

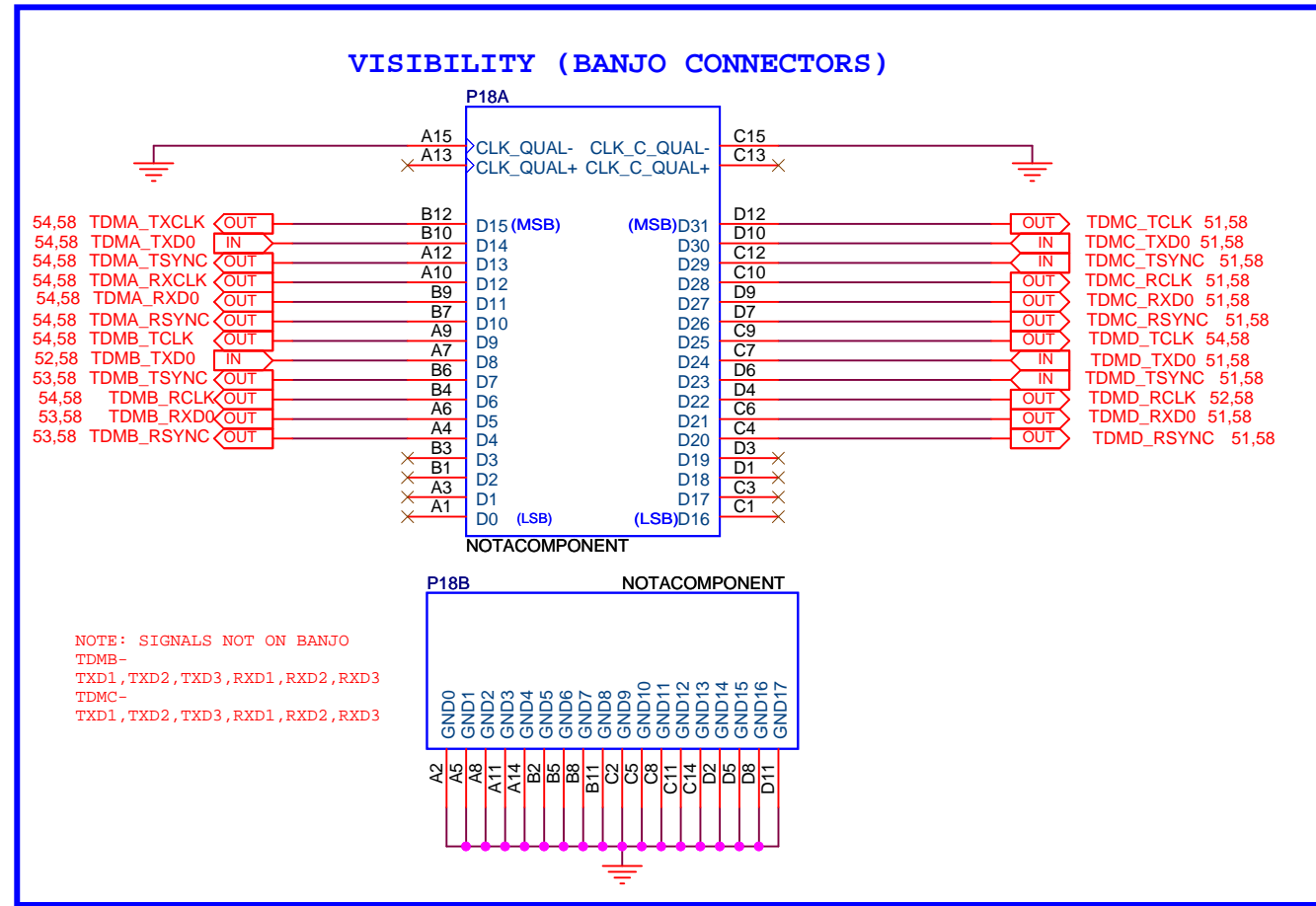


Note :TDMA, TDMB,TDMC,TDMD,SER3 ports brought from the Multiplexer

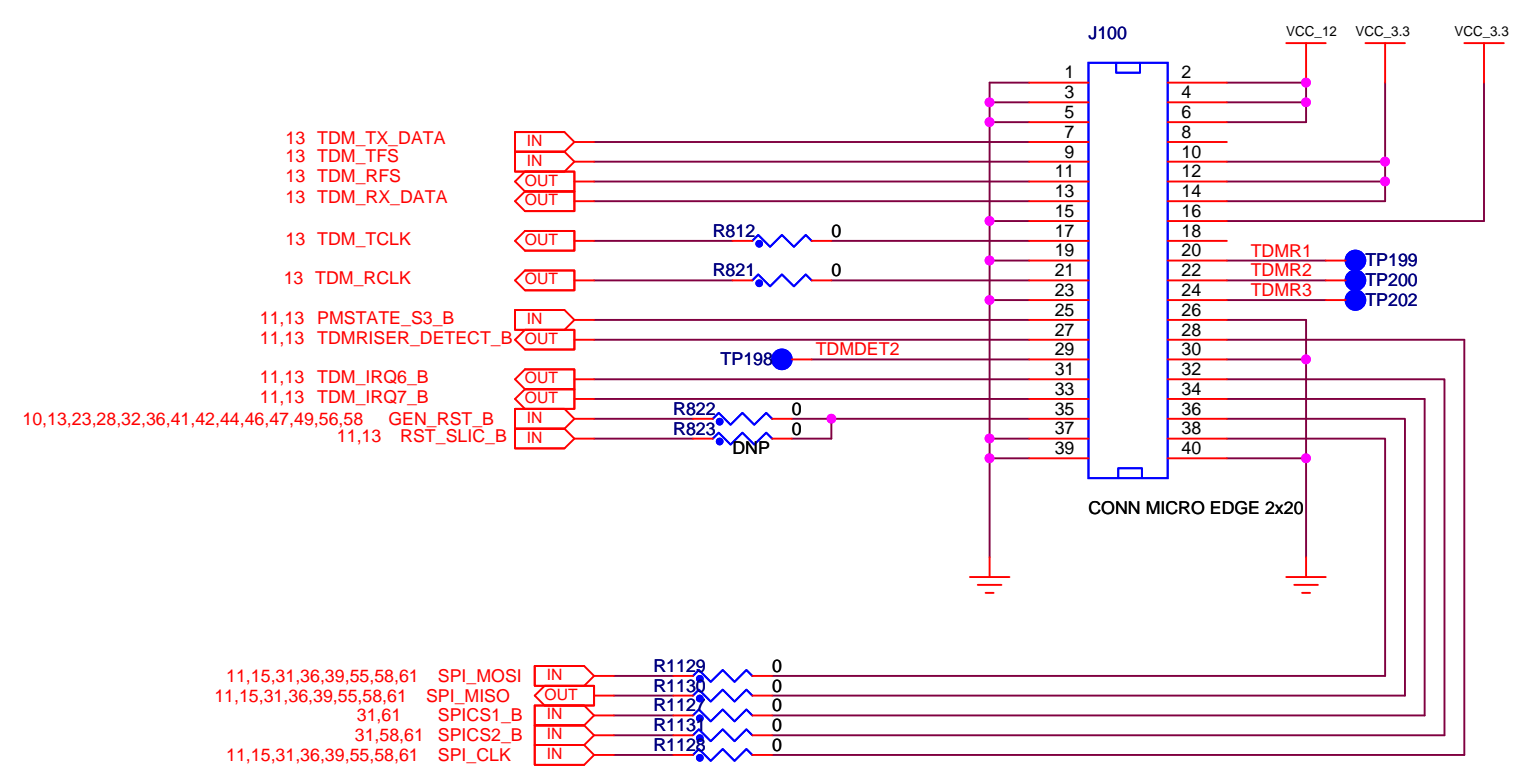
*-Nibble mode



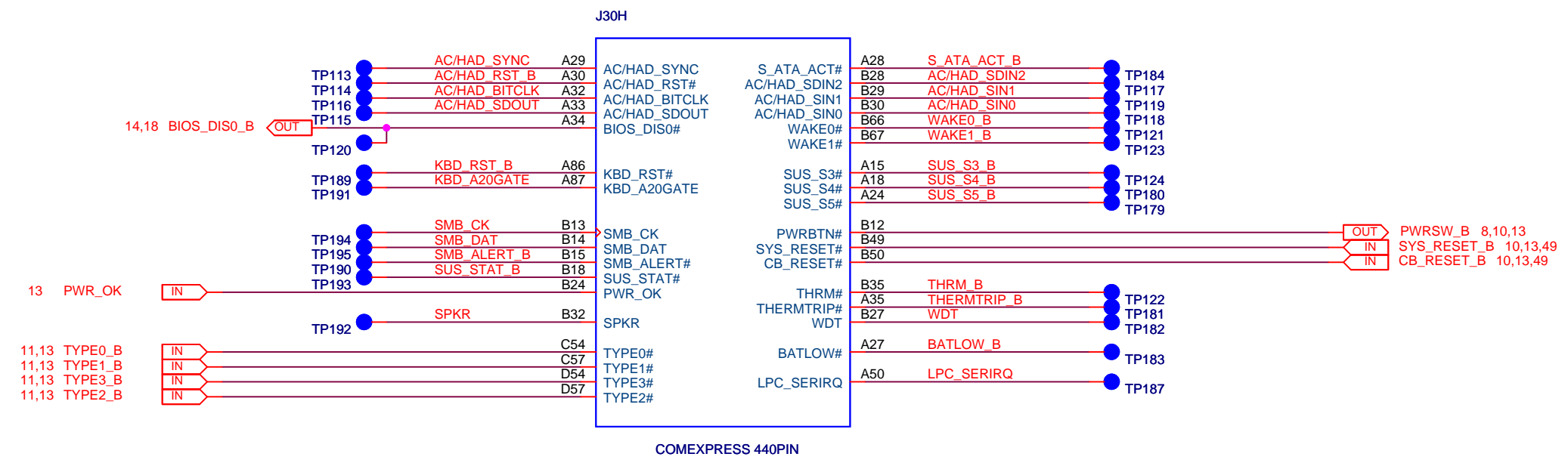
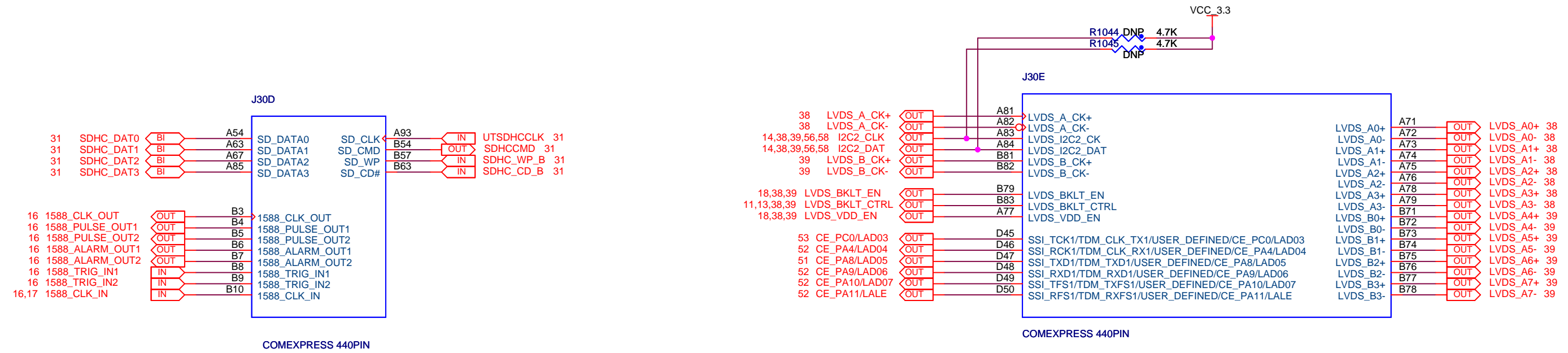
VISIBILITY (BANJO CONNECTORS)



TDM RISER CARD CONNECTIVITY



COM EXPRESS CONNECTOR



COM EXPRESS CONNECTOR

