

MPC5553 Microcontroller Product Brief

The MPC5553 is a member of the next generation of microcontrollers that follows the MPC5xx family and is based on the PowerPC™ Book E architecture. Book E enhances the PowerPC architecture's fit in embedded applications and is 100% user mode compatible (with floating point library) with the classic PowerPC instruction set. This document provides an overview of the MPC5553 microcontroller features, including the major functional components.

The MPC5553 device's on-chip modules include the following:

- Single issue, 32-bit PowerPC Book E-compliant e200z6 CPU core complex
- 32-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 212 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- External bus interface (EBI) with error correction status module (ECSM)
- System integration unit (SIU)

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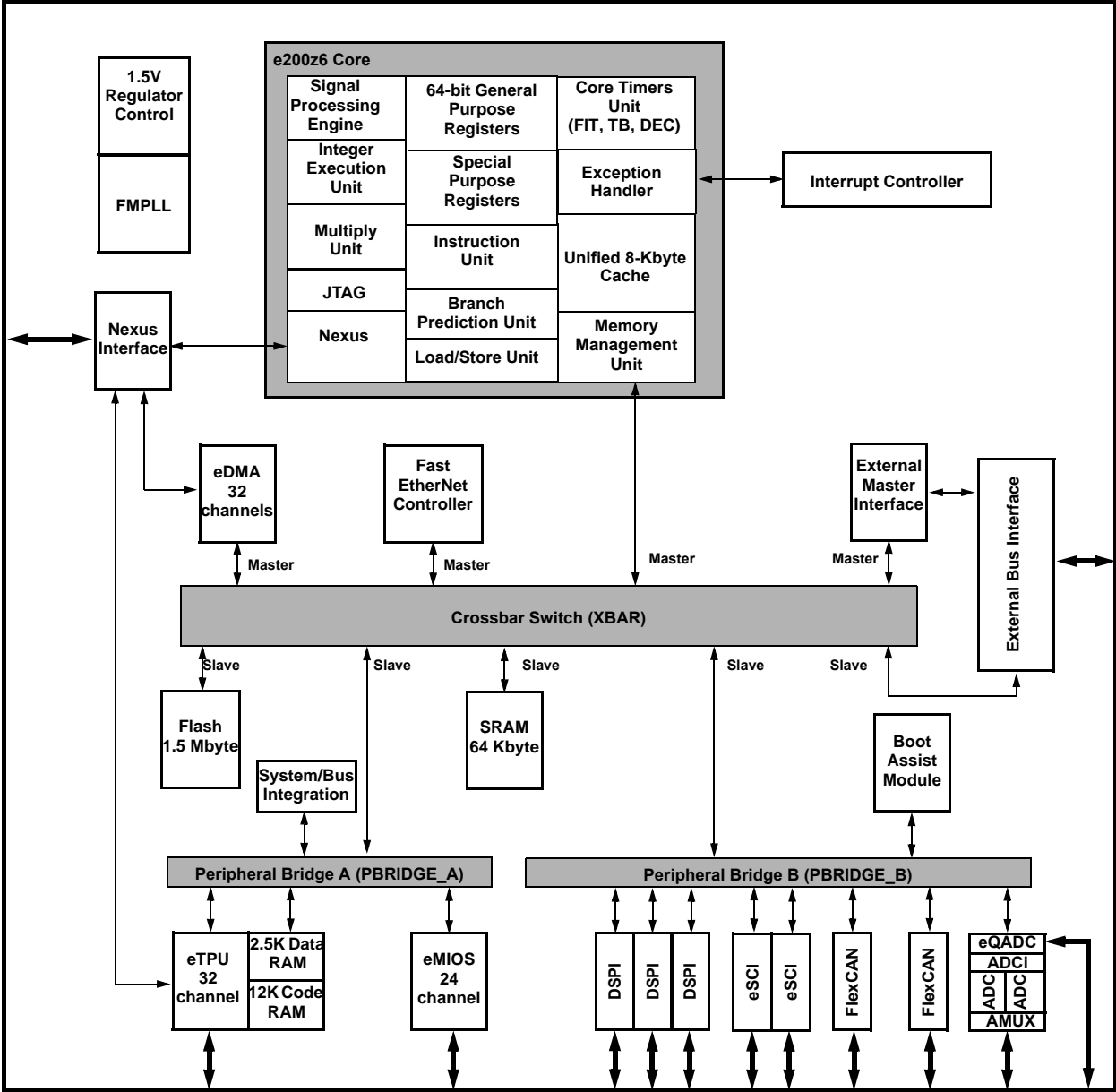
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- 1.5 Mbytes on-chip Flash with Flash bus interface unit (FBIU)
- 64 Kbytes on-chip static RAM
- Boot assist module (BAM)
- 24-channel enhanced modular I/O system (eMIOS)
- 1 32-channel enhanced time processor unit (eTPU)
- 2 enhanced queued analog-to-digital converters (eQADC)
- 3 deserial serial peripheral interface (DSPI) modules
- 2 enhanced serial communication interface (eSCI) modules
- 2 controller area network (FlexCAN) modules
- Fast Ethernet controller (FEC)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)

To locate any published errata or updates for this document, refer to the web site at <http://www.freescale.com/semiconductors>.

1 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5553.



- MPC5500 Device Module Acronyms**
- CAN** – Controller area network (FlexCAN)
 - DSPI** – Deserial/serial peripheral interface
 - DMA** – Enhanced direct memory access
 - eMIOS** – Enhanced modular I/O system
 - eQADC** – Enhanced queued analog/digital converter
 - eSCI** – Enhanced serial communications interface
 - eTPU** – Enhanced time processing units
 - FMPLL** – Frequency modulated phase-locked loop
 - SRAM** – Static RAM
- LEGEND**
- DEC** – Decrementer
 - FIT** – Fixed interval timer
 - TB** – Time base
 - WDT** – Watchdog timer
- e200z6 Core Component Acronyms**

Figure 1. MPC5553 Block Diagram

2 MPC5500 Family Comparison

Table 1 shows the modules and features available on each of the devices in the family.

Table 1. MPC5500 Family Members

Module		MPC5534	MPC5553	MPC5554
Power PC Core		e200z3	e200z6	e200z6
Variable Length Instruction support		Yes	No	No
Cache		None	8k Unified ¹	32k Unified ²
Memory Management Unit		16 entry	32 entry	32 entry
Crossbar		4x5	4x5	3x5
Core Nexus		Class 3+ (NZ3C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)
SRAM		64k	64k	64k
FLASH	Main Array	1M ³	1.5M ⁴	2M ⁴
	Shadow Block	1K	1K	1K
External bus (EBI)	Data Bus	16 bit ⁵	32 bit ⁵	32 bit ⁵
	Address Bus	24	24	24
Calibration Bus		Yes	Partial	No
Direct Memory Access (DMA)		32 channel	32 channel	64 channel
DMA Nexus		None	Class 3	Class 3
Serial		2	2	2
	eSCI_A	Yes	Yes	Yes
	eSCI_B	Yes	Yes	Yes
Controller Area Network (CAN)		2	2	3
	CAN_A	64 buf	64 buf	64 buf
	CAN_B	No	No	64 buf
	CAN_C	64 buf	64 buf	64 buf
	CAN_D	No	No	No
	CAN_E	No	No	No
SPI		3	3	4
	DSPI_A	No	No	Yes
	DSPI_B	Yes	Yes	Yes
	DSPI_C	Yes	Yes	Yes
	DSPI_D	Yes	Yes	Yes
eMIOS		24 channel	24 channel	24 channel
eTPU		32 channel	32 channel	64 channel
	eTPU_A	Yes	Yes	Yes
	eTPU_B	No	No	Yes

Table 1. MPC5500 Family Members (continued)

Module	MPC5534	MPC5553	MPC5554
eTPU Code memory	12k	12k	16k
Parameter RAM	2.5k	2.5k	3k
Nexus	Class 3	Class 3	Class 3
Interrupt controller	210 channel	210 channel	300 channel
Analog to Digital Converter (eQADC)	40 channel	40 channel	40 channel
ADC_0	Yes	Yes	Yes
ADC_1	Yes	Yes	Yes
Fast Ethernet Controller (FEC)	No	Yes ⁶	No
FlexRay	No	No	No
FlexRay Nexus	No	No	No
Phase Lock Loop (PLL)	FM	FM	FM
Voltage Regulator Controller (VRC)	Yes	Yes	Yes

NOTES:

- ¹ 2-way associative
- ² 8-way associative
- ³ 16-Byte flash page size for programming.
- ⁴ 32-Byte flash page size for programming.
- ⁵ May not be externally available in some package configurations.
- ⁶ The FEC signals are shared with Data Bus pins DATA[16:31].

3 Features

This section provides a high-level description of the major features of the MPC5553.

3.1 High-performance e200z6 Core Processor

- 32-bit PowerPC Book E compliant CPU
- 32 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 32-entry, fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 8-Kbyte unified cache with line locking
 - 2-way set associative
 - 2 32-bit fetches per clock
 - 8-entry store buffer
 - Way locking
 - Supports assigning cache as instruction or data only on a per way basis
 - Supports tag and data parity

Features

- Vectored interrupt support
- Interrupt latency < 70 ns @132MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (internal SRAM and Flash)
- Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit GPRs
- Floating point
 - IEEE® 754 compatible with software wrapper
 - Single precision in hardware, double precision with software library
 - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency in the MPC5553. To reduce latency, long cycle time instructions are aborted upon interrupt requests.
- Extensive system development support through Nexus debug module

3.2 Crossbar Switch (XBAR)

- 4 master ports; 5 slave ports
- 32-bit address bus; 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

3.3 Enhanced Direct Memory Access (eDMA) Controller

- 32 channels support independent 8-, 16-, 32-, or 64-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

3.4 Interrupt Controller (INTC)

- 212 total interrupt vectors
 - 191 peripheral interrupt requests
 - plus 8 software settable sources
 - plus 13 reserved interrupts
- Unique 9-bit vector per interrupt source

- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

3.5 Frequency Modulated Phase-locked Loop (FMPLL)

- Input clock frequency from 8 MHz to 20 MHz
- Current controlled oscillator (ICO) range from 50 MHz to maximum device frequency
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 4 selectable modes of operation
- Programmable frequency modulation
- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter (reduces number of external components required)
- Engineering clock output

3.6 External Bus Interface (EBI)

- 1.8V–3.3V I/O nominal I/O voltage
- Memory controller with support for various memory types
- 416 BGA: 32-bit data bus, 24-bit address bus without transfer size indication
- 324 BGA: 16-bit data bus, 20-bit address bus
- 208 MAPBGA: no external bus
- Selectable drive strength
- Configurable bus speed modes
- Support for external master accesses to internal addresses
- Burst support
- Bus monitor
- 4 chip select ($\overline{CS}[0:3]$) signals, but no \overline{CS} signals in the 208 MAPBGA package
- Support for dynamic calibration with up to 3 calibration chip selects ($\overline{CAL_CS}[0 \text{ and } 2:3]$)
- Configurable wait states

3.7 System Integration Unit (SIU)

- Centralized GPIO control of 198 I/O and bus pins
- Centralized pad control on a per-pin basis
- System reset monitoring and generation

Features

- External interrupt inputs, filtering and control
- Internal multiplexer submodule (SIU_DISR, SIU_ETISR, SIU_EIISR)

3.8 Error Correction Status Module (ECSM)

- Configurable error-correcting codes (ECC) reporting for internal SRAM and Flash memories

3.9 On-chip Flash

- 1.5 Mbytes burst Flash memory
- 256K × 64 bit configuration
- Censorship protection scheme to prevent Flash content visibility
- Hardware read-while-write feature that allows blocks to be erased/programmed while other blocks are being read (used for EEPROM emulation and data calibration)
- 16 blocks, ranging from 16 Kbytes to 128 Kbytes, to support features such as boot block, operating system block, and EEPROM emulation
- Read while write with multiple partitions
- Parallel programming mode to support rapid end of line programming
- Hardware programming state machine

3.10 Configurable Cache Memory, 8-Kbyte

- 2-way, set-associative, unified (instruction and data) cache

3.11 On-chip, Internal Static RAM (SRAM)

- 64-Kbyte, general-purpose RAM; 32 Kbytes are on standby power
- ECC performs single-bit correction, double-bit error detection

3.12 Boot Assist Module (BAM)

- Enables and manages the transition of MCU from reset to user code execution in the following configurations:
 - User application can boot from internal or external Flash memory
 - Download and execution of code via CAN or eSCI

3.13 Enhanced Modular I/O System (eMIOS)

- 24 orthogonal channels with double action, PWM, and modulus counter functionality
- Supports all DASM and PWM modes of MIOS14 (MPC5xx)
- 4 selectable time bases plus shared time or angle counter bus

- DMA and interrupt request support
- Motor control capability

3.14 Enhanced Time Processor Unit (eTPU)

- One eTPU engine
- The engine is an event-triggered timer subsystem
- High level assembler/compiler
- 32 channels
- 24-bit timer resolution
- 12-Kbyte shared code memory
- 2.5-Kbyte shared data memory
- Variable number of parameters allocatable per channel
- Double match/capture channels
- Angle clock hardware support
- Shared time or angle counter bus for all eTPU and eMIOS modules
- DMA and interrupt request support
- Nexus Class 3 Debug support (with some Class 4 support)

3.15 Enhanced Queued Analog/Digital Converter (eQADC)

- 2 independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5V
- 40 single-ended inputs channels, expandable to 65 channels with external multiplexers
- 4 pairs of differential analog input channels.
- 10-bit accuracy at 400 ksamples/s, 8-bit accuracy at 800 ksamples/s
- Supports 6 FIFO queues with fixed priority.
- Queue modes with priority-based preemption; initiated by software command, internal (eTPU and eMIOS), or external triggers
- DMA and interrupt request support
- Supports all functional modes from QADC (MPC5xx family)

3.16 Deserial Serial Peripheral Interface Modules (DSPI)

- Three DSPI modules
- SPI
 - Full duplex communication ports with interrupt and eDMA request support
 - Supports all functional modes from QSPI submodule of QSMCM (MPC5xx family)
 - Support for queues in RAM
 - 6 chip selects, expandable to 64 with external demultiplexers
 - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
 - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Deserial serial interface (DSI)
 - Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels
 - Chaining of DSI submodules
 - Triggered transfer control and change in data transfer control (for reduced EMI)

3.17 Enhanced Serial Communication Interface (eSCI) Modules

- Two eSCI modules
- UART mode provides NRZ format and half or full duplex interface
- eSCI bit rate up to 1 Mbps
- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8 or 9 bits
- Separately enabled transmitter and receiver
- LIN Support
- DMA support
- Interrupt request support

3.18 FlexCANs

- Two FlexCANs
- 64 message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Based on and including all existing features of the Freescale TouCAN module
- Programmable acceptance filters
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number

- Listen only mode capabilities
- Programmable clock source: system clock or oscillator clock

3.19 Nexus Development Interface (NDI)

- Per IEEE®-ISTO 5001-2003
- Real time development support for PowerPC core and eTPU engines through Nexus Class 3 (some Class 4 support)
- Data trace of eDMA accesses
- Read and write access
- Configured via the IEEE® 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

3.20 IEEE® 1149.1 JTAG Controller (JTAGC)

- IEEE® 1149.1-2001 Test Access Port (TAP) interface
- A JCOMP input that provides the ability to share the TAP. Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports IEEE® 1149.1-2001 defined instructions
- A 5-bit instruction register that supports additional public instructions
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

3.21 Voltage Regulator Controller

- Provides a low cost solution to power the core logic and reduces the number of power supplies required from the customer power supply chip.

3.22 POR Block

- Provides initial reset condition up to the voltage at which pins ($\overline{\text{RESET}}$) can be read safely. It does not guarantee the safe operation of the chip at specified minimum operating voltages.

3.23 Fast Ethernet Controller (FEC)

- IEEE® 802.3 MAC (compliant with IEEE® 802.3 1998 edition)
- Built-in FIFO and DMA controller

- Support for different Ethernet physical interfaces:
 - 100Mbps IEEE® 802.3 MII
 - 10Mbps IEEE® 802.3 MII
 - 10Mbps 7-wire interface (industry standard)

4 Architecture Overview

The following sections provided detailed information about each of the on-chip modules.

4.1 e200z6 Core

The MPC5553 uses the e200z6 core explained in detail in the *e200z6 PowerPC™ Core Reference Manual*. The e200z6 CPU utilizes a 7-stage pipeline for instruction execution. The instruction fetch 1, instruction fetch 2, instruction decode/register file read, execute1, execute2/memory access1, execute3/memory access2, and register writeback stages operate in an overlapped fashion, allowing single-clock instruction execution for most instructions.

In addition, a signal processing extension (SPE) auxiliary processing unit (APU) is provided to support real-time fixed point and single-precision floating point operations using the 64-bit general purpose registers (GPRs) implemented on the e200z6 core. All arithmetic instructions that execute in the core operate on data in the GPRs. The registers have been extended to 64-bits in order to support vector instructions defined by the SPE APU. These instructions operate on 16-bit or 32-bit data types, and produce vector or scalar results.

4.2 Crossbar Switch

The multi-port crossbar (XBAR) switch supports simultaneous connections between 4 master ports and 5 slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width at all master and slave ports.

The crossbar allows for concurrent transactions to occur from any master port to any slave port. It is possible for all master ports and slave ports to be in use at the same time as a result of independent master requests. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. By default, requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

4.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes an enhanced DMA engine which performs source and destination address calculations and the actual data movement operations, along with an SRAM-based

memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

4.4 INTC

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from 212 interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests. These same software settable interrupt requests can also be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR. Therefore, these software settable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

4.5 FMPLL

The frequency modulated phase-locked loop (FMPLL) allows the user to generate high speed system clocks from an 8 MHz to 20 MHz crystal oscillator or external clock generator. Furthermore, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio, modulation depth, and modulation rate are all software configurable.

4.6 EBI

The external bus interface (EBI) controls data transfers across the crossbar switch to/from memories or peripherals in the external address space. The EBI also enables an external master to access internal address space. The EBI includes a memory controller that generates interface signals to support a variety of external memories. The EBI memory controller supports single data rate (SDR) burst mode Flash, SRAM, and asynchronous memories. In addition, the EBI supports up to 4 regions (via chip selects), along with programmed region-specific attributes.

4.7 SIU

The MPC5553 system integration unit (SIU) controls MCU reset configuration, pad configuration, external interrupt, general-purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration module contains the external pin boot configuration logic. The pad configuration module controls the static electrical characteristics of I/O pins. The GPIO module provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. The SIU is accessed by the e200z6 core through the crossbar switch.

4.8 ECSM

The error correction status module (ECSM) provides status information regarding platform memory errors reported by error-correcting codes.

4.9 Flash

The MPC5553 provides 1.5 Mbytes of programmable, non-volatile, Flash memory storage. The non-volatile memory (NVM) can be used for instruction and/or data storage.

The MPC5553 Flash also contains a Flash bus interface unit (FBIU) that interfaces the system bus to a dedicated Flash memory array controller. The FBIU supports a 64-bit data bus width at the system bus port, and a 256-bit read data interface to Flash memory. The FBIU contains two 256-bit prefetch buffers, and a prefetch controller that prefetches sequential lines of data from the Flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal Flash array accesses are registered in the FBIU and are forwarded to the system bus on the following cycle, incurring 3 wait-states. Prefetch operations may be automatically controlled, and may be restricted to servicing a single bus master. Prefetches may also be restricted to being triggered for instruction or data accesses.

4.10 Cache

The e200z6 core supports a 8-Kbyte, 2-way set-associative, unified (instruction and data) cache with a 32-byte line size. The cache improves system performance by providing low-latency data to the e200z6 instruction and data pipelines, which decouples processor performance from system memory performance. The cache is virtually indexed and physically tagged. The e200z6 does not provide hardware support for cache coherency in a multi-master environment. Software must be used to maintain cache coherency with other possible bus masters.

Both instruction and data accesses are performed using a single bus connected to the cache. Addresses from the processor to the cache are virtual addresses used to index the cache array. The memory management unit (MMU) provides the virtual-to-physical translation for use in performing the cache tag compare. The MMU may also be configured so that virtual addresses are passed through to the cache as the physical address untranslated. If the physical address matches a valid cache tag entry, the access hits in the cache. For a read operation, the cache supplies the data to the processor, and for a write operation, the data from the processor updates the cache. If the access does not match a valid cache tag entry (misses

in the cache) or a write access must be written through to memory, the cache performs a bus cycle on the system bus.

4.11 SRAM

The internal static RAM (SRAM) module provides a general-purpose, 64-Kbyte memory block, of which 32 Kbytes are on standby power.

4.12 BAM

The boot assist module (BAM) is a block of read-only memory that enables and manages the transition of an MCU from reset to user code execution. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports 4 different modes of booting:

- Booting from internal Flash memory
- Single master booting from external memory
- Multi-master booting from external memory with either no arbitration or external arbitration
- Serial boot loading (a program is downloaded into RAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from Flash memory (either internal or external) and configures the MPC5553 hardware accordingly.

4.13 eMIOS

The enhanced modular I/O system (eMIOS) module provides the functionality to generate or measure time events. A unified channel (UC) module is employed, providing a superset of the functionality of all MIOS channels and a consistent user interface. This allows for more flexibility as each unified channel can be programmed for different functions in different applications. In order to identify up to two timed events, each UC contains 2 comparators, a time base selector, and registers. This structure is able to produce match events, which can be configured to measure or generate a waveform. Alternatively, input events can be used to capture the time base, allowing measurement of an input signal.

4.14 eTPU

The enhanced time processor unit (eTPU) of the MPC5553 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU. The eTPU supports several features of the TPU implemented in the MPC500 family of parts, making it easy to port older applications.

The eTPU has 32 channels, each associated with one input and one output signal, 2 independent 24-bit time bases for channel synchronization, an event-triggered microengine, resource sharing features that support channel use of common channel registers, memory, and microengine time, and test and development support.

4.15 eQADC

The enhanced queued analog-to-digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADCs), and a single master to single slave serial interface to an off-chip external device. The 2 on-chip ADCs are architected to allow access to all the analog channels.

The eQADC transfers commands from multiple command FIFOs (CFIFOs) to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into multiple result FIFOs (RFIFOs) in parallel, independently of the CFIFOs. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the CFIFOs to the on-chip ADCs or to the external device. It also monitors the fullness of CFIFOs and RFIFOs, and accordingly generates DMA or interrupt requests to control data movement between the FIFOs and the system memory, which is external to the eQADC.

4.16 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5553 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU channels, eMIOS channels, and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. There are 3 identical DSPI blocks (DSPI_B, DSPI_C, and DSPI_D) on the MPC5553 MCU.

The DSPIs have 3 configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as a SPI with support for queues
- Deserial serial interface (DSI) configuration where the DSPI serializes eTPU and eMIOS output channels and deserializes the received data by placing it on the eTPU and eMIOS input channels
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations, interleaving DSI frames with SPI frames and giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

4.17 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to local interconnect network (LIN) slave devices.

4.18 FlexCAN

The MPC5553 MCU contains 2 controller area network (FlexCAN) blocks. Each FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification Version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each FlexCAN module contains 64 message buffers.

4.19 NDI

The Nexus development interface (NDI) block provides real-time development support capabilities for the MPC5553 PowerPC-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the MPC5553. The NDI block interfaces to the host processor, dual eTPU processors, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCU's internal memory map, and access to the PowerPC and eTPU internal registers during halt, via the auxiliary port. The Nexus interface also supports a JTAG only mode using only the JTAG pins.

4.20 JTAGC

The IEEE 1149.1 JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard.

4.21 FEC

The fast Ethernet controller (FEC) of the MPC5553 supports several standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- 10/100 Mbps MII interface
- 10 Mbps, 7-wire interface that uses a subset of the MII pins

5 Chip Configuration

Various functions of the MPC5553 may be implemented at reset. The following operations may be configured:

- Boot mode
 - Internal memory boot (default)
 - External memory boot (single master)
 - Boot from serial port (FlexCAN or eSCI)
- PLL mode
 - Normal mode with crystal reference (default)
 - Normal mode with external reference
 - Bypass mode
- Watchdog timer enable

6 Documentation

Table 2 lists other documents that provide information related to the MPC5553 and its development support tools. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at <http://www.freescale.com/semiconductors>.

Table 2. MPC5553 and Related Documentation

Document Number	Title	Revision	Status
MPC5554RM/D	MPC5553/MPC5554 Reference Manual	See the MPC5554 web page for the latest version.	Available
ETPURM/D	Enhanced Time Processing Unit (eTPU) Reference Manual		Available
AN1259/D	System Design and Layout Techniques for Noise Reduction in MCU-Based Systems		Available
AN2614	Nexus Interface Options for the MPC5500 Family		Available
AN2706	EMC Guidelines for MPC5500-based Systems		Available

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