MCF5301*x* Product Brief

Supports MCF53010, MCF53011, MCF53012, MCF53013, MCF53014, MCF53015, MCF53016, & MCF53017

by: Microcontroller Solutions Group

The MCF5301*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 3 ColdFire microarchitecture. All MCF5301*x* devices contain a smart card interface, an enhanced Secure Digital host controller, USB On-the-Go controllers, a voice-band audio codec, an IC identification module, as well as other peripherals that enable the MCF5301*x* family for use in point-of-sale, voice-over-wirless-LAN, and analog-telephone-adapter applications. Optional peripherals include a USB host controller, second smart card port, cryptography coprocessor, integrated microphone, speaker, handset, and headphone amplifiers, and voice-over-IP software.

This document provides an overview of the MCF5301*x* microprocessor family, focusing on its highly diverse feature set. It was written from the perspective of the MCF53017 superset device. However, it also pertains to the MCF53010–16. See the following section for a summary of differences between the various devices of the MCF5301*x* family.

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1 Application Examples

The MCF5301*x* family is well suited for voice-over-IP (VOIP) applications that require a broad range of communication peripherals and high performance to enable competitive and cost-effective system solutions. As shown in the following example, this microprocessor is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

1.1 VoIP Telephone

Figure 1 shows the MCF5301*x* used in a typical wireless voice-over-IP telephone application.

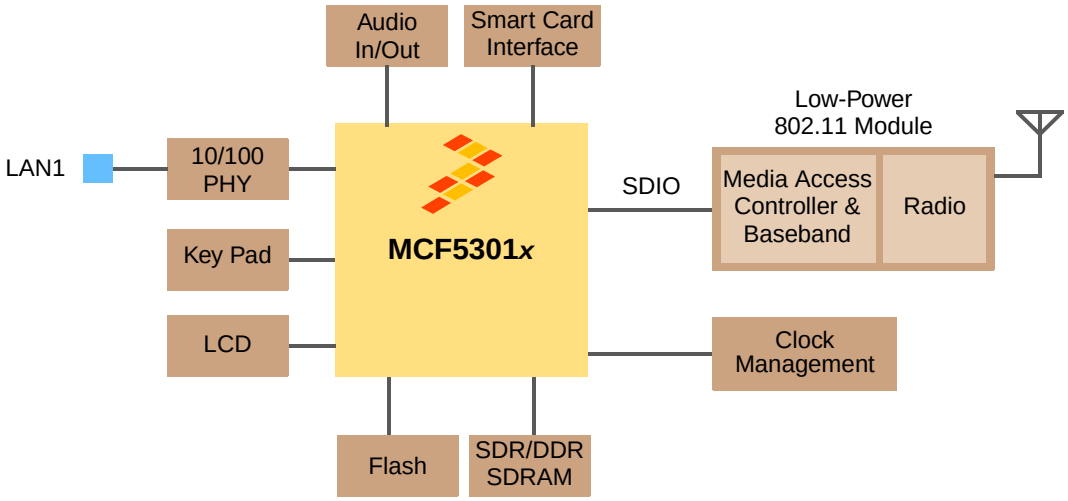


Figure 1. Wireless VoIP Telephone Example

2 Features

2.1 MCF5301*x* Family Comparison

The following table compares the various device derivatives available within the MCF5301*x* family.

Table 1. MCF5301*x* Family Configurations

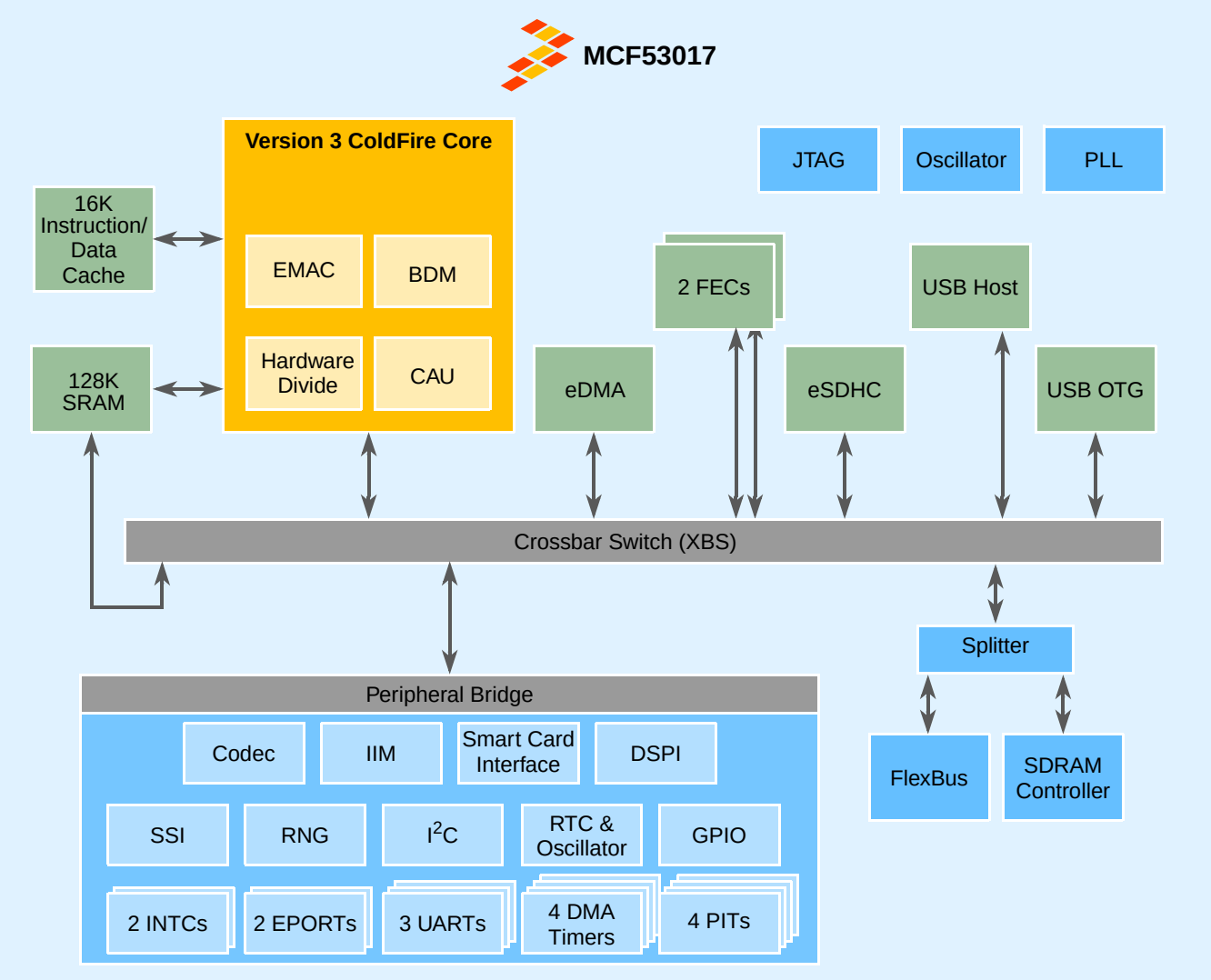
Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
Version 3 ColdFire Core with EMAC (enhanced multiply-accumulate unit)	•	•	•	•	•	•	•	•
Core (system) clock	up to 240 MHz							
Peripheral and external bus clock (Core clock ÷ 3)	up to 80 MHz							
Performance (Dhrystone/2.1 MIPS)	up to 211							

Table 1. MCF5301*x* Family Configurations (continued)

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
Unified data/instruction cache	16 Kbytes							
Static RAM (SRAM)	128 Kbytes							
Voice-over-IP software	—	—	•	•	—	—	•	•
Cryptography acceleration unit (CAU)	—	•	—	•	—	•	—	•
Random number generator	—	•	—	•	—	•	—	•
Smart card interface (SIM)	1 port				2 ports			
Voice-band audio codec	•	•	•	•	•	•	•	•
Integrated audio amplifiers	—	—	—	—	•	•	•	•
IC identification module (IIM)	2 Kbits							
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•	•	•	•
SDR/DDR SDRAM controller	•	•	•	•	•	•	•	•
FlexBus external interface	•	•	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•	•	•
USB 2.0 Host	—	—	—	—	•	•	•	•
Synchronous serial interface (SSI)	•	•	•	•	•	•	•	•
Fast Ethernet controller (FEC)	2	2	2	2	2	2	2	2
UARTs	3	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•	•
DSPI	•	•	•	•	•	•	•	•
Real-time clock	•	•	•	•	•	•	•	•
32-bit DMA timers	4	4	4	4	4	4	4	4
Watchdog timer (WDT)	•	•	•	•	•	•	•	•
Periodic interrupt timers (PIT)	4	4	4	4	4	4	4	4
Edge port module (EPORT)	•	•	•	•	•	•	•	•
Interrupt controllers (INTC)	2	2	2	2	2	2	2	2
16-channel direct memory access (DMA)	•	•	•	•	•	•	•	•
General purpose I/O Module (GPIO)	•	•	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•	•	•
Package	208 LQFP				256 MAPBGA			

2.2 Block Diagram

Figure shows a top-level block diagram of the MCF53017 superset device.



LEGEND

BDM	– Background debug module	**IIM**	– IC identification module
CAU	– Cryptography acceleration unit	**INTC**	– Interrupt controller
DSPI	– DMA serial peripheral interface	**JTAG**	– Joint Test Action Group interface
eDMA	– Enhanced direct memory access module	**PCI**	– Peripheral Component Interconnect
eSDHC	– Enhanced Secure Digital host controller	**PIT**	– Programmable interrupt timers
EMAC	– Enchanced multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random number generator
FEC	– Fast Ethernet Controller	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I²C	– Inter-Integrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

MCF53017 Block Diagram

2.3 Operating Parameters

- 0ºC to 70ºC junction temperature devices are available
- 1.2V core, 3.3V I/O, 1.8V/2.5V/3.3V external memory bus

2.4 Packages

Depending on device, the MCF5301*x* family is available in the following packages:

- 208-pin low-profile quad flat package (LQFP)
- 256-pin molded array process ball grid array (MAPBGA)

2.5 Chip Level Features

The MCF5301*x* system includes these distinctive features:

- Version 3 ColdFire® core with EMAC
- Up to 211 Dhrystone 2.1 MIPS @ 240 MHz
- 16 Kbytes unified instruction/data cache
- 128 Kbytes internal SRAM
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- Enhanced Secure Digital Host Controller (eSDHC)
- Two ISO7816 smart card interfaces
- Voice-band audio codec
- 160 MHz 16-bit (DDR/mobile-DDR) or 80 MHz 32-bit (SDR) SDRAM controller
- USB 2.0 On-the-Go controller
- USB 2.0 host controller
- 2 10/100 Ethernet MACs
- Coprocessor for acceleration of the DES, 3DES, AES, MD5, and SHA-1 algorithms
- Random number generator
- 16 channel DMA controller
- Synchronous serial interface
- 4 periodic interrupt timers
- 4 32-bit timers with DMA support
- DMA supported serial peripheral interface (DSPI)
- 3 UARTs
- I^2C bus interface

2.6 Module-by-Module Feature List

The following is a brief summary of the functional blocks in the MCF53017 superset device. For more details refer to the *MCF53017 ColdFire Microprocessor Reference Manual* (MCF53017RM).

2.6.1 Version 3 ColdFire Variable-Length RISC Processor

- Static operation
- 32-bit address and data path on-chip
- Maximum 240 MHz processor core and 80 MHz bus frequency
- Sixteen total general-purpose 32-bit registers data and address
- Enhanced multiply-accumulate unit (EMAC) for DSP and fast multiply operations
- Hardware divide execution unit supporting various 32-bit operations
- Implements the ColdFire Instruction Set Architecture, ISA_A+

2.6.2 Cryptography Acceleration Unit (CAU)

- Instruction-level coprocessor
- Supports DES, 3DES, AES, MD5, and SHA-1

2.6.3 On-chip Memories

- 128 KByte dual-ported SRAM on CPU internal bus
  - Accessible to non-core bus masters (e.g. FEC, DMA, USB OTG, USB host, and eSDHC controllers) via the crossbar switch
- Non-blocking 16 KByte unified cache organized as 4-way set associative with 16 bytes per cache line and 1024 cache lines, supporting copyback and write-through modes of operation

2.6.4 Phase Locked Loop (PLL)

- 14–40 MHz reference crystal
- Four register-programmable output dividers

2.6.5 Power Management

- Fully static operation with processor sleep and whole chip stop modes
- Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Peripheral power management register to enable/disable clocks to most modules
- Software controlled disable of external clock input for low power consumption

2.6.6 Chip Configuration Module (CCM)

- System configuration during reset
- Bus monitor, abort monitor
- Configurable output pad drive strength and slew rate control
- Unique part identification and part revision numbers

2.6.7 Reset Controller

- Separate reset in and reset out signals
- Seven sources of reset: power-on reset (POR), external, software, watchdog timer, loss of lock, loss of clock, JTAG instruction
- Status flag indication of source of last reset

2.6.8 System Control Module

- Access control registers
- Core watchdog timer with a 2^n (where n = 8:31) clock cycle selectable timeout period
- Core fault reporting

2.6.9 Crossbar Switch

- Concurrent access from different masters to different slaves
- Slave arbitration attributes configured on a slave by slave basis
- Fixed or round-robin arbitration

2.6.10 Enhanced Secure Digital Host Controller (eSDHC)

- Compatible with the following specifications:
  - *SD Host Controller Standard Specification, Version 2.0* (http://www.sdcard.org)
  - *MultiMediaCard System Specification, Version 4.0* (http://www.mmca.org)
  - *SD Memory Card Specification, Version 2.0* (http://www.sdcard.org)
  - *SDIO Card Specification, Version 1.2* (http://www.sdcard.org)
  - *CE-ATA Card Specification, Version 1.0* (http://www.sdcard.org)
- Designed to work with CE-ATA, SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, MMC 4x, and MMC RS cards
- SD bus clock up to 25 MHz
- Supports 1- and 4-bit SD and SDIO modes, 1- and 4-bit MMC modes, and 4-bit CE-ATA devices
- Contains a fully configurable 128 x 32-bit FIFO for read/write data

2.6.11 Smart Card Interface Module (SIM)

- Two ISO7816 smart card interfaces
- Internal one-wire mode (single data pin)
- Programmable clock divisor
- Fourteen total interrupt sources (six transmit, six receive, two control functions)

2.6.12 Voice Band Audio Codec

- Supports various input clock frequency from 16–30 MHz
- Supports 8 KHz/8.1 KHz software interface frequency
- Includes amplifiers for microphone, speaker, handset, and headphone
- Ability to disable codec (battery save mode) via software
- Ability to disable input/output high-pass filter stage via software
- Programmable decimation filter (250–511.75)

2.6.13 IC Identification Module (IIM)

- 2 Kbits of software-programmable polysilicon fuses
- Eight independent fuse banks of 256 bits each
- Ability to write-protect fuses on a per-bank basis

2.6.14 Universal Serial Bus (USB) 2.0 On-The-Go (OTG) Controller

- Support for full speed (FS) and low speed (LS) via a serial interface or on-chip FS/LS transceiver
- Uses 60 MHz reference clock based off of the system clock or from an external pin
- Supports VBUS power enable and VBUS over-current detect to control bus power

2.6.15 Universal Serial Bus (USB) 2.0 Host Controller

- Support for full speed (12 Mbps) and low speed (1.5 Mbps) via serial interface
- On-chip full-speed/low-speed transceiver
- Uses 60 MHz reference clock based off of the system clock or from an external pin
- Supports VBUS power enable and VBUS over-current detect to control bus power

2.6.16 SDR/DDR SDRAM Controller

- Supports a glueless interface to SDR and DDR SDRAM devices
- 16-bit (DDR) or 32-bit (SDR) fixed memory port width
- 16-byte critical word first burst transfer

- Up to 14 lines of row address, up to 12 (in 32-bit mode) or 13 (in 16-bit bus mode) column address lines, 2 bits of bank address, and a maximum of two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit mode
- Supports up to 256 MByte of memory
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode

2.6.17 FlexBus (External Interface)

- Glueless connections to 16-, and 32-bit external memory devices (SRAM, flash, ROM, etc.)
- Support for independent primary and secondary wait states per chip select
- Programmable address setup and hold time with respect to chip-select assertion, per transfer direction
- Glueless interface to SRAM devices with or without byte strobe inputs
- Programmable wait state generator
- 32-bit external bidirectional data bus and 24-bit address bus
- Up to six chip selects available
- Byte/write enables (byte strobes)
- Ability to boot from external memories that are 8, 16, or 32 bits wide

2.6.18 Synchronous Serial Interface (SSI)

- Supports shared (synchronous) transmit and receive sections
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Gated clock mode operation requiring no frame sync
- Programmable data interface modes such as I^2S, LSB aligned, and MSB aligned
- Programmable word length up to 24 bits
- AC97 support

2.6.19 Fast Ethernet Media Access Controllers (FEC MAC)

- Two fast Ethernet controllers
- 10/100 BaseT/TX capability, half duplex or full duplex
- On-chip transmit and receive FIFOs
- Built-in dedicated DMA controller
- Memory-based flexible descriptor rings
- Media independent interface (MII) to external transceiver (PHY)
- Separate RMII gasket to interface with RMII-compatible PHY

2.6.20 Random Number Generator (RNG)

- FIPS-140 compliant for randomness and non-determinism
- Supports key generation
- Integrated entropy sources

2.6.21 Real Time Clock

- Full clock: days, hours, minutes, seconds
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
- User-programmable 16-bit prescaler to support various input clock frequencies

2.6.22 Programmable Interrupt Timers (PIT)

- Four programmable interrupt timers each with a 16-bit counter
- Configurable as a down counter or free-running counter

2.6.23 DMA Timers

- Four 32-bit timers with DMA and interrupt request trigger capability
- Input capture and reference compare modes

2.6.24 DMA Serial Peripheral Interface (DSPI)

- Full-duplex, three-wire synchronous transfer
- Up to five chip selects available
- Master and slave modes with programmable master bit-rates
- Up to 16 pre-programmed transfers

2.6.25 Universal Asynchronous Receiver Transmitters (UARTs)

- Three UARTs with a 16-bit divider for clock generation
- Interrupt control logic
- DMA support with separate transmit and receive requests
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to 2 stop bits in 1/16 increments
- Error-detection capabilities

2.6.26 I²C Module

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- Fully compatible with industry-standard I²C bus
- Master or slave modes support multiple masters
- Automatic interrupt generation with programmable level

2.6.27 Interrupt Controllers

- Two interrupt controllers, supporting up to 64 interrupt sources each, organized as seven programmable levels
- Unique vector number for each interrupt source
- Ability to mask any individual interrupt source plus a global mask-all capability
- Support for service routine software interrupt acknowledge (IACK) cycles
- Combinational path to provide wake-up from low power modes

2.6.28 Edge Port Module

- 2 edge port modules
- Each pin can be individually configured as low level sensistive interrupt pin or edge-detecting interrupt pin (rising, falling, or both)
- Exit stop mode via level-detect function

2.6.29 DMA Controller

- 16 fully programmable channels with 32-byte transfer control
- Data movement via dual-address transfers for 8-, 16-, 32- and 128-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor "nested" counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration.
- External request pins for up to four channels

2.6.30 General Purpose I/O interface

- Up to 83 bits of GPIO for the MCF53012/13 (256 MAPBGA)
- Up to 61 bits of GPIO for the MCF53010/11 (208 LQFP)
- Bit manipulation supported via set/clear functions
- Various unused peripheral pins may be used as GPIO

2.6.31 System Debug Support

- Background debug mode (BDM) Revision B+ for debug features while halted
- Real time debug support, with four PC breakpoint registers and a pair of address breakpoint registers with optional data

2.6.32 JTAG Support

- JTAG part identification and part revision numbers

3 Developer Environment

The MCF5301*x* family of MCUs supports similar tools and third party developers as other Freescale ColdFire products, offering a widespread, established network of tools and software vendors.

The following development support will be available:

- Evaluation boards (EVBs)
- Compilers and debuggers
- Debug interfaces
- Initialization tool

The following software support will be available:

- Code examples
- Various module drivers (e.g., Ethernet, USB, SPI, I^2C)
- Third party real-time operating systems (RTOS)

4 Revision History

Table 2 provides a revision history for this document.

Table 2. MCF53017PB Document Revision History

Rev. No.	Date of Release	Substantive Change(s)
3	12 Aug 2009	Initial public revision.

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