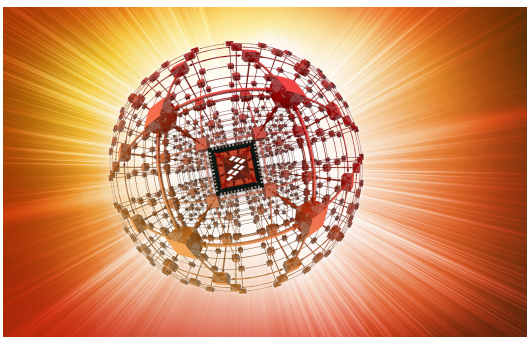
Document Number:KV10PB
Rev 2, 02/2014

KV10 Sub-Family Product Brief



Contents

1 KV10 family introduction

The KV10 MCU family is built on ARM® Cortex®-M0+ based core and enabled by innovative 90 nm thin film storage (TFS) flash process technology. The 1.71 V-3.6 V device consists of 32 KB of flash, 8 KB of RAM memory and has a motor control 6-channel FlexTimer(FTM) , two 2-channel Flextimers, two 12-bit ADC with 1 µs conversion time, and supports 16-bit resolution. For communication, one Flex SCI/UARTs, a SPI, and a I2C/MBUS, are included. Packages supported are 48 LQFP, 32 LQFP, and 32 QFN. These key features make KV10 series ideal for industrial motor control applications, inverters, and low end power conversion applications. The KV10 series MCU is a member of Freescale's Torq motor control and power conversion family of microcontrollers.

© 2014 Freescale Semiconductor, Inc.

2 Features

2.1 Feature summary

The following table lists the features of the KV10 devices. The device features may vary by package.

Table 1. Feature summary

Feature	Details
Hardware characteristics	
Package	48-pin LQFP (7 x 7mm2) 32-pin LQFP (5 x 5 mm^2) 32-pin QFN
Voltage range	1.71 V to 3.6 V
Temperature range (T_A)	-40°C to 105°C
Temperature range (T_J)	-40°C to 125°C
System	
Central processing unit (CPU)	ARM Cortex M0+
Max. CPU frequency	75 MHz
Nested vectored interrupt controller (NVIC)	32
Direct memory access (DMA)	4 channels
DMA request multiplex	64 sources
Non-maskable interrupt (NMI)	Yes
Software watchdog (iWDOG)	Independent clock source with windowed mode
External Watchdog Monitor	Yes with independent clock source
Debug	2-pin serial wire debug (SWD)
Trace	Data watchpoint and trace (DWT)
Boundary scan	No, no JTAG
Unique identification (ID) number	128-bit wide
Memory	
Flash memory	32 KB
Random-access memory (RAM)	8KB
Data memory	No
Cyclic redundancy check (CRC)	16- or 32-bit CRC with programmable generator polynomial
External bus interface	No
Clocks	
External crystal oscillator or resonator	Low range, low power or full-swing: 32 - 40 kHz High range, low power or full-swing: 4 - 20 MHz
External square wave input clock	DC to 20 MHz
Internal clock references	4M Hz IRC

Table continues on the next page...

Table 1. Feature summary (continued)

Feature	Details
	32 kHz IRC 1 kHz LPO
Frequency-locked loop (FLL)	Range: 8 - 75 MHz
Human-machine interface (HMI)	
General-purpose input/output (GPIO)	3 V I/O (Not 5V tolerant) Pin interrupt / DMA request capability Digital glitch filter on all input pins Configurable pull up device on all input pins
Analog	
Power management controller (PMC)	Low voltage warning and detect with selectable trip points
12-bit analog-to-digital converter (ADC)	2 x 16bit SAR ADC Each with 12 channel single-ended/ 2 sets of differential inputs, with dual acquisition /result registers. 1us conversion time
Programmable Gain Amplifier	NO
High-speed comparator (HSCMP) with internal 6-bit digital-to-analog converter (DAC)	2
12 bit DAC	1
Timers	
Motor Control Timer	6 channel FlexTimer (FTM0)
FLexTimer (FTM)	Two 2ch FlexTimer (FTM1& FTM2) with quadrature decoding
Programmable delay block (PDB)	1 PDB with 15 inputs supporting multiple pulse to two ADCs
LPTimer	Low power timer wakes up CPU from low power modes
Communication interfaces	
Serial peripheral interface (DSPI)	One with four word FIFO
Inter-integrated circuit (I^2C)	One with SMBUS support
Flexible Serial Communications Interface (FlexSCI)	Two SCIs

2.2 Block diagram

The block diagram shows the features of the KV10 series MCU. Within each category, the diagram shows the superset of modules and number of module instances on the 44-pin member of the family.

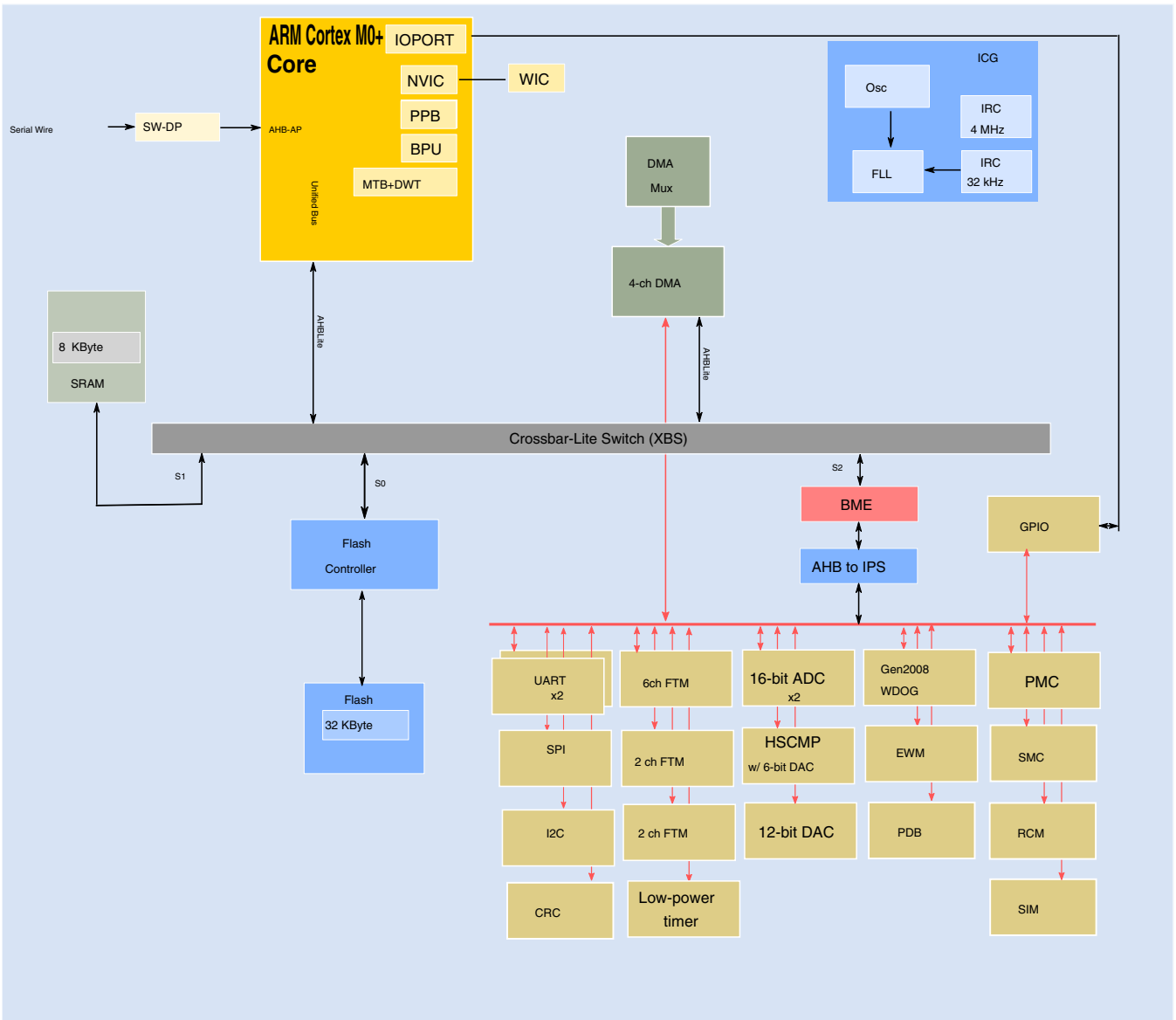


Figure 1. KV10 series block diagram

2.3 Module-by-module feature list

2.3.1 Core Modules

2.3.1.1 ARM Cortex-M0+ Core

- Supports up to 75MHz frequency
- Support up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)

- Decorated Memory Controller for improved bit handling of peripheral modules • Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Basic Branch Buffer (BBB) provides lightweight program trace capabilities using system RAM as the destination memory
- ARMv6M architecture based all features/ISA present in Cortex-M0 to be preserved
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Configurable nested vectored interrupt controller (NVIC)

2.3.1.2 Nested Vectored Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Includes a single nonmaskable interrupt

2.3.1.3 Wake-Up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to Very-Deep-Sleep mode
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a nonmasked interrupt is detected.
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

2.3.1.4 Debug Controller

- Serial Wire JTAG Debug Port (SWJ-DP) combines
  - external interface that provides a serial-wire bidirectional debug interface

2.3.2 Memory

2.3.2.1 On-Chip Memory

- Up to 32KB program flash memory
- Up to 8KB SRAM
- Security circuitry to prevent unauthorized access to RAM and flash contents

2.3.2.2 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit using 16/32-bit shift register
- User Configurable 16/32 bit CRC
- Programmable Generator Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation
- Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in lsb format

2.3.3 Human-machine interface

2.3.3.1 General Purpose Input/Output (GPIO)

- Progammable glitch filter and interrupt with selectable polarity on all input pins
- Hysteresis and configurable pull up/down device on all input pins

2.3.4 Analog

2.3.4.1 16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two's complement 16-bit sign-extended format
  - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Dual acquisition mode with two result registers.
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

2.3.4.2 High-Speed Analog Comparator (CMP)

- Up to Three selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Comparator output may be sampled, windowed(ideal for zero cross detection) or digitally filtered
- Remains operational in low power mode
- Internal 6-bit DAC programmable reference on 4th input

2.3.4.3 6-bit digital-to-analog converter (DAC)

- On-chip programmable reference generator output
- Typically 5 mV of input offset
- Less than 40 µA power consumption in enable mode and less than 1 nA in disable mode (excluding programmable reference generator)
- Fixed ACMP hysteresis from 3 mV to 20 mV
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Remains operational in low power mode

2.3.4.4 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

2.3.5 Timers

2.3.5.1 FlexTimers (FTM)

- 6 channel FlexTimer
- Selectale FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

2.3.5.2 FlexTimers (FTM)

- 2 channel FlexTimer
- Selectale FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- Hall Sensor speed/position support via ORing of 3 input capture pins to one channel - NEW feature.
- Modulation mode support - New feature.

- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

2.3.5.3 Programmable Delay Block (PDB)

- Up to 15 trigger input sources and software trigger source
- PDB channel for ADC hardware trigger
  - One PDB channel is associated with two ADCs.
  - One trigger output for ADC hardware trigger and up to four pre-trigger outputs for ADC trigger select per PDB channel
  - Trigger outputs can be enabled or disabled independently.
  - One 16-bit delay register per pre-trigger output
  - Optional bypass of the delay registers of the pre-trigger outputs
  - Operation in One-Shot or Continuous modes
  - One programmable delay interrupt
  - One sequence error interrupt
  - One channel flag and one sequence error flag per pre-trigger
  - DMA support
- pulse output (pulse-out's)
  - Pulse-out's can be enabled or disabled independently.
  - Programmable pulse width

2.3.5.4 Watchdog Timer (WDOG)

- Independent, configurable clock source input
- Write-once control bits with unlock sequence
- Programmable timeout period
- Ability to test watchdog timer and reset
- Windowed refresh option
- Robust refresh mechanism
- Cumulative count of watchdog resets between power-on resets
- Configurable interrupt on timeout

2.3.5.5 External Watchdog Monitor (EWM)

- Independent 1 kHz LPO clock source
- Output signal to gate an external circuit which is controlled by CPU service or external input

2.3.6 Communication interfaces

2.3.6.1 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability

- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8-bit or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed transfers of large amounts of data
- Support for both transmit and receive by DMA

2.3.6.2 UART

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection

2.3.6.3 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and SMBus version 2 features
- Up to 100 kbps with maximum bus loading, 400kbps supported with limited bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode
- DMA support

3 Revision history

Revision number	Date	Substantial changes
2	02/2014	Initial public release

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale, Freescale logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere.

©2014 Freescale Semiconductor, Inc.

Document Number KV10PB
Revision 2, 02/2014