

# MPC5777C\_3N45H

## Mask Set Errata



# Mask Set Errata for Mask 3N45H

## Revision History

This report applies to mask 3N45H for these products:

- MPC5777C
- MPC5775E
- MPC5775B

**Table 1. Mask Specific Information**

major_mask_rev_num	1
minor_mask_rev_num	0
jtag_id	0x1837_701D

**Table 2. Revision History**

Revision	Date	Significant Changes
SEP2022	9/2022	The following errata were revised. <ul style="list-style-type: none"> <li>• ERR011235</li> </ul>
FEB2022	2/2022	The following errata were added. <ul style="list-style-type: none"> <li>• ERR051156</li> </ul> The following errata were revised. <ul style="list-style-type: none"> <li>• ERR050575</li> </ul>
AUG2021	8/2021	The following errata were added. <ul style="list-style-type: none"> <li>• ERR050789</li> <li>• ERR050782</li> <li>• ERR051044</li> <li>• ERR010963</li> <li>• ERR050575</li> <li>• ERR050312</li> </ul> The following errata were revised. <ul style="list-style-type: none"> <li>• ERR011235</li> <li>• ERR050246</li> </ul>
December 2019	12/2019	Revision history is now shown in reverse chronological order (newest first). Summary table now shows the complete erratum number. <p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR050130</li> </ul>

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**Table 2. Revision History (continued)**

Revision	Date	Significant Changes
		<ul style="list-style-type: none"> <li>• ERR050090</li> <li>• ERR050246</li> </ul>
June 2019	10/2019	<p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR011479</li> </ul> <p>The following errata were revised.</p> <ul style="list-style-type: none"> <li>• ERR007227</li> <li>• ERR007869</li> </ul>
October 2018	10/2018	<p>The following errata were removed.</p> <ul style="list-style-type: none"> <li>• ERR010542</li> </ul> <p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR050016</li> <li>• ERR011030</li> <li>• ERR011048</li> <li>• ERR011031</li> <li>• ERR011456</li> <li>• ERR011028</li> <li>• ERR010586</li> <li>• ERR011238</li> <li>• ERR010755</li> <li>• ERR011457</li> <li>• ERR011469</li> </ul>
May 2018	5/2018	<p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR011321</li> <li>• ERR011235</li> <li>• ERR010853</li> <li>• ERR011295</li> <li>• ERR011294</li> <li>• ERR011213</li> <li>• ERR011293</li> <li>• ERR008341</li> </ul> <p>The following errata were revised.</p> <ul style="list-style-type: none"> <li>• ERR010436</li> <li>• ERR007227</li> </ul>

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**Table 2. Revision History (continued)**

Revision	Date	Significant Changes
		<ul style="list-style-type: none"> <li>• ERR010415</li> <li>• ERR010900</li> </ul>
August 2017	7/2017	<p>The following errata were removed.</p> <ul style="list-style-type: none"> <li>• ERR007231</li> </ul> <p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR010436</li> <li>• ERR010844</li> <li>• ERR010798</li> <li>• ERR010808</li> <li>• ERR010797</li> <li>• ERR010900</li> </ul> <p>The following errata were revised.</p> <ul style="list-style-type: none"> <li>• ERR010610</li> </ul>
February 2017	2/2017	<p>The following errata were removed.</p> <ul style="list-style-type: none"> <li>• ERR003521</li> </ul> <p>The following errata were added.</p> <ul style="list-style-type: none"> <li>• ERR010714</li> <li>• ERR010439</li> <li>• ERR010396</li> <li>• ERR010636</li> <li>• ERR010645</li> <li>• ERR010580</li> <li>• ERR010737</li> <li>• ERR010610</li> <li>• ERR010578</li> <li>• ERR010415</li> <li>• ERR010542</li> </ul> <p>The following errata were revised.</p> <ul style="list-style-type: none"> <li>• ERR010453</li> </ul>
August 2016	8/2016	<p>The following errata were revised.</p> <ul style="list-style-type: none"> <li>• ERR010453</li> <li>• ERR009595</li> </ul>
July 2016	7/2016	<p>The following errata were removed.</p>

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**Table 2. Revision History (continued)**

Revision	Date	Significant Changes
		<ul style="list-style-type: none"> <li>• ERR007544</li> </ul> The following errata were added. <ul style="list-style-type: none"> <li>• ERR010443</li> <li>• ERR010453</li> <li>• ERR010226</li> <li>• ERR002340</li> <li>• ERR010135</li> <li>• ERR010378</li> </ul> The following errata were revised. <ul style="list-style-type: none"> <li>• ERR008195</li> </ul>
March 2016	3/2016	Initial Revision

## Errata and Information Summary

**Table 3. Errata and Information Summary**

Erratum ID	Erratum Title
<a href="#">ERR006990</a>	CJTAG: possible incorrect TAP state machine advance during Check Packet
<a href="#">ERR010439</a>	CMU: CMU_0 OLR is set out of reset when XOSC used in 8mhz mode, due to wrong RCDIV reset value
<a href="#">ERR007116</a>	CRC: AutoSAR 4.0 8-bit CRC8 0x2F is not supported in hardware
<a href="#">ERR051156</a>	CSE: BOOT_MAC calculation is done only on [DATA] during secure boot
<a href="#">ERR008251</a>	DECFIL: timestamp may be lost in edge trigger mode
<a href="#">ERR050090</a>	DSPI/SPI: Incorrect data may be transmitted in slave mode
<a href="#">ERR009783</a>	DSPI: Frame transfer does not restart after DSI frame matches preprogrammed value
<a href="#">ERR009664</a>	DSPI: Frame transfer does not restart in case of DSI parity error in master mode
<a href="#">ERR009656</a>	DSPI: Frame transfer does not restart in case of SPI parity error in master mode
<a href="#">ERR007352</a>	DSPI: reserved bits in slave CTAR are writable
<a href="#">ERR010755</a>	DSPI: Transmit and Receive FIFO fill flags in status register is not cleared when DMA is improperly configured
<a href="#">ERR001147</a>	DSPI: Using DSPI in DSI mode with MTO may cause data corruption
<a href="#">ERR050782</a>	e200: Time Base TBU register contains wrong value during TBL rollover
<a href="#">ERR010797</a>	EBI: Address 31 signal is not available in non-multiplexed mode
<a href="#">ERR007001</a>	EBI: External TA and TEA do not operate properly when internal master does burst aborts to EBI
<a href="#">ERR007546</a>	EBI: Input signal valid to D_CLKOUT posedge (setup time) spec is not met

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Table 3. Errata and Information Summary (continued)

Erratum ID	Erratum Title
<a href="#">ERR011235</a>	EMIOS: Any Unified Channel running in OPWMB or OPWMCB mode may function improperly if the source counter bus is generated by Unified channel in MC mode
<a href="#">ERR050575</a>	eMIOS: Any Unified Channel running in OPWMCB mode may function improperly if the lead or trail dead time insertion features is used and its timebase is generated by Unified channel in MCB mode
<a href="#">ERR011293</a>	EMIOS: For any UC operating in OPWFMB mode the Channel Count register should not be written with a value greater than Channel B Data register value
<a href="#">ERR011295</a>	EMIOS: In OPWFMB mode, A1/B1 registers do not get reloaded with A2/B2 register values if counter value returns 0x1 after counter wrap condition
<a href="#">ERR011294</a>	EMIOS: OPWFMB and MCB mode counter rollover resets the counter to 0x0 instead of 0x1 as mentioned in the specification
<a href="#">ERR009978</a>	eMIOS: Unexpected channel flag assertion during GPIO to MCB mode transition
<a href="#">ERR008313</a>	EQADC: TUE specification not met
<a href="#">ERR009344</a>	eSCI: Late assertion of Transmit Data Ready Interrupt Flag (TXRDY) for Local Interconnect Network (LIN) frame receive (RX) operation
<a href="#">ERR009001</a>	eSCI: Incorrect behavior while in LIN Standard Bit error detection mode
<a href="#">ERR009361</a>	eSCI: Timing of TXRDY interrupt flag assertion is incorrect for LIN TX Frame
<a href="#">ERR009797</a>	eSCI: Unable to send next frame after timeout in LIN mode
<a href="#">ERR005642</a>	ETPU2: Limitations of forced instructions executed via the debug interface
<a href="#">ERR008252</a>	eTPU: ETPU Angle Counter (EAC) Tooth Program Register (TPR) register write may fail
<a href="#">ERR009090</a>	eTPU: Incorrect eTPU angle counter function under certain conditions
<a href="#">ERR009809</a>	eTPU: MDU flags(Overflow/Carry) may be set incorrectly
<a href="#">ERR009338</a>	eTPU: Time base counter values can fail to export properly
<a href="#">ERR008042</a>	FCCU: EOUT signals are active, even when error out signaling is disabled
<a href="#">ERR007099</a>	FCCU: Error pin signal length is not extended when the next enabled fault, with its alarm timeout disabled, occurs
<a href="#">ERR010900</a>	FCCU: False indication of a fault state for a single safe clock period can be generated on the error output pin
<a href="#">ERR007227</a>	FCCU: FCCU Output Supervision Unit (FOSU) will not monitor faults enabled while already pending
<a href="#">ERR007223</a>	FCCU: FCCU_IRQ_EN register is writeable in all operating modes
<a href="#">ERR007230</a>	FCCU: FCCU_IRQ_EN[28] is writeable, but reserved.
<a href="#">ERR009570</a>	FCCU: FOSU may assert reset when a hardware recoverable fault of width less than one safe clock period occurs
<a href="#">ERR007869</a>	FCCU: FOSU monitoring of a fault is blocked for second or later occurrence of the same fault
<a href="#">ERR009670</a>	FCCU: Limitation of error output signal observation test function

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Table 3. Errata and Information Summary (continued)

Erratum ID	Erratum Title
<a href="#">ERR007226</a>	FCCU: the error-out signalling cannot be disabled in non Bi-stable protocols
<a href="#">ERR008505</a>	FCCU: The FCCU on-chip programmable glitch filter on ERRORIN does not operate correctly
<a href="#">ERR010011</a>	FCCU: Unexpected faults may be indicated as a result of FCCU reset
<a href="#">ERR007429</a>	FCCU: Writes to Flash assert FCCU_NCF #17 (FLASH_INIT)
<a href="#">ERR002340</a>	FEC: slot time is designed for 516 bit times; deviation from the 802.3
<a href="#">ERR007547</a>	FEC: Transmit signal hold time reduced
<a href="#">ERR010963</a>	Flash: Memory accesses may be corrupted when flash is operating between 33MHz and 75MHz
<a href="#">ERR009320</a>	FLASH: (SPC5777C) Address Encode False Report (MCR[AEE] and possible FCCU channels)
<a href="#">ERR008004</a>	FLASH: Array Integrity with Breakpoints enabled may skip addresses for certain RWSC and APC combinations
<a href="#">ERR007422</a>	FLASH: Pipeline should not be enabled on the flash
<a href="#">ERR007991</a>	FLASH: Rapid Program or Erase Suspend fail status
<a href="#">ERR009595</a>	FlexCAN: Corrupted frame possible if Freeze Mode or Low Power Mode are entered during a Bus-Off state
<a href="#">ERR007724</a>	FlexCAN: Documentation of ECC registers
<a href="#">ERR008341</a>	FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.
<a href="#">ERR050246</a>	FlexCAN: Receive Message Buffers may have its Code Field corrupted if the Receive FIFO function is used
<a href="#">ERR009527</a>	FlexCAN: The transmission abort mechanism may not work properly
<a href="#">ERR008195</a>	INTC: Interrupt Controller does not work correctly when in hardware vector interrupt mode and FMPPERDIV is set to divide-by-4 or divide-by-
<a href="#">ERR007545</a>	JTAGC: TCK low to TDO data valid spec is not met
<a href="#">ERR007511</a>	LFAST: Maximum data rate is 240Mbps
<a href="#">ERR010586</a>	M_CAN: Configuration NBTP.NTSEG2 = '0' not allowed
<a href="#">ERR050312</a>	M_CAN: Debug message handling state machine not reset to Idle state when CCCR.INIT is set.
<a href="#">ERR050789</a>	M_CAN: Dedicated Tx Buffers configured with the same Message ID are not transmitted in order of lowest buffer number first
<a href="#">ERR011469</a>	M_CAN: Message transmitted with wrong arbitration and control fields
<a href="#">ERR050016</a>	M_CAN: Retransmission in DAR mode due to lost arbitration at the first two identifier bits
<a href="#">ERR051044</a>	M_CAN: Transmission order of the Tx Queue buffers with the same Message ID is impacted by the PUT index functionality
<a href="#">ERR011456</a>	M_CAN: Tx FIFO message sequence inversion
<a href="#">ERR011457</a>	M_CAN: Unexpected High Priority Message (HPM) interrupt

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Table 3. Errata and Information Summary (continued)

Erratum ID	Erratum Title
<a href="#">ERR009517</a>	MCAN: Edge filtering may cause incorrect frame reception
<a href="#">ERR010109</a>	MPC5777C: Enabling pending read optimization (off by default) can cause incorrect operation on the system crossbar
<a href="#">ERR009770</a>	MPC5777C: Incorrect operation of open-drain outputs
<a href="#">ERR009856</a>	MPC5777C: Incorrect operation of Software Watchdog Timers in debug mode
<a href="#">ERR010798</a>	MPC577xC: Asserting RESET pin input while Software System Reset is in progress prevents offline self-test from running
<a href="#">ERR008164</a>	MPC577xC: Current injection causes leakage path across the DSPI and LFAST LVDS pins
<a href="#">ERR010580</a>	MPC577xC: Flash HVD may assert during slow input supply ramp
<a href="#">ERR010714</a>	MPC577xC: Lockstep errors must be ignored when debugging core 1 in lockstep mode
<a href="#">ERR010737</a>	MPC577xC: Nexus Program Trace Sync Message sometimes missing after queue overflow
<a href="#">ERR010853</a>	MPC577xC: Oscillator clock may be disturbed by input/output pin ETPUB31
<a href="#">ERR009332</a>	MPC577xC: Performance degradation caused by optimization control bits on Platform Configuration Module
<a href="#">ERR011479</a>	MPC577xC: PLLCFG2 toggling during reset may cause incorrect XOSC operation
<a href="#">ERR010453</a>	MPC577xC: Reduced accuracy on EQADC_B channels using VDDEH7 power domain
<a href="#">ERR009784</a>	MPC577xC: Reset escalation count is reduced by 1 when configured via UTEST DCF record
<a href="#">ERR010578</a>	MPC577xC: The Temperature Sensor may cause extended reset times
<a href="#">ERR011213</a>	MPC577xC: When an FCCU reset occurs, the Engineering Clock (ENGCLK) output clock and CLKOUT can have a shortened duty cycle.
<a href="#">ERR011238</a>	MPC577xC: When internal resets occur, there may be a delay before the external reset pin asserts
<a href="#">ERR010610</a>	NPC: Core cannot be halted if NPC is not enabled when entering debug mode
<a href="#">ERR008340</a>	NPC: EVTO_B toggles instead of remaining asserted when used by the DTS if Nexus is not enabled
<a href="#">ERR006726</a>	NPC: MCKO clock may be gated one clock period early when MCKO frequency is programmed as SYS_CLK/8 and gating is enabled
<a href="#">ERR007120</a>	NZxC3: DQTAG implemented as variable length field in DQM message
<a href="#">ERR008369</a>	PAD_RING: Reset output (RSTOUT) pin is not driven during Power-On Reset (POR) or Low-Voltage Detect (LVD) assertion
<a href="#">ERR009087</a>	PADRING: Input High Voltage (max) and Hysteresis (min) specs not met
<a href="#">ERR009250</a>	PASS: JTAG password not working during reset
<a href="#">ERR010396</a>	PASS: Password challenge to PASS fails while program erase ongoing in any block in memory partition 0
<a href="#">ERR007904</a>	PASS: Programming Group Lock bit (PGL) can be de-asserted by multiple masters writing the correct password sections to the CINn registers.

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Table 3. Errata and Information Summary (continued)

Erratum ID	Erratum Title
<a href="#">ERR050130</a>	PIT: Temporary incorrect value reported in LMTR64H register in lifetimer mode
<a href="#">ERR011321</a>	PIT_RTI: Generates false RTI interrupt on re-enabling
<a href="#">ERR010844</a>	PMC: During PMC Self Test, an external reset or FOSU reset could cause a POR type reset instead
<a href="#">ERR010226</a>	PMC: In SMPS mode, during input supply power down, core voltage can exceed specification limits
<a href="#">ERR009804</a>	PMC: LVD/HVD Event Status Register does not consistently indicate the reset source
<a href="#">ERR010135</a>	PMC: Resets that occur during the PMC Self Test process can cause corrupted results.
<a href="#">ERR011030</a>	PMC: Self Test can repeat when clearing the result flag
<a href="#">ERR011028</a>	PMC: Self Test result flag clears on any write to the ST_RESULT field
<a href="#">ERR011031</a>	PMC: When a disabled LVD/HVD is tested via PMC Self Test, the self test may fail
<a href="#">ERR011048</a>	PMC: When using an external regulator and a reset occurs, the core supply voltage needs to be above 1.22V and below 1.300V to exit from reset
<a href="#">ERR005887</a>	PSI5: Detection of a received bit causes an electrical error in specific conditions
<a href="#">ERR009863</a>	PSI5: Enabling interrupts in the General Interrupt Control Register (PSI5_CH0_GICR) has no effect
<a href="#">ERR006992</a>	PSI5: IS_DEBUG_FREEZE bit is not documented
<a href="#">ERR007234</a>	PSI5: No transfer error generated for accesses within the unused range of the PSI5 peripheral window
<a href="#">ERR005073</a>	PSI5: Possible message reception errors due to incorrect data latency reference point
<a href="#">ERR006553</a>	PSI5: T bit error Ambiguity is noticed in Synchronous mode
<a href="#">ERR008368</a>	REACM2: ETPU_C clock does not halt if REACM2 Module Disable (MDIS) is set to 1
<a href="#">ERR008367</a>	REACM: Register is unexpectedly written after exiting halted state
<a href="#">ERR010415</a>	SDADC: Additional DMA requests generated when using watchdog threshold crossover event
<a href="#">ERR008711</a>	SDADC: Digital filter and FIFO not disabled when MCR[EN] is cleared
<a href="#">ERR008225</a>	SDADC: FIFO Flush Reset command requires clearing the Data FIFO Full Flag
<a href="#">ERR010378</a>	SDADC: Incorrect data provided when FIFO is disabled and FIFO overwrite is enabled
<a href="#">ERR006906</a>	SDADC: Invalid conversion data when output settling delay value is less than 23
<a href="#">ERR008631</a>	SDADC: low threshold watchdog cannot be used with signed data
<a href="#">ERR007356</a>	SDADC: The SDADC FIFO does not function correctly when FIFO overwrite option is used
<a href="#">ERR008710</a>	SDADC: Watchdog Crossover event missed if FM Peripheral Clock frequency is less than or equal to the sigma-delta ADC clock frequency
<a href="#">ERR007204</a>	SENT: Number of Expected Edges Error status flag spuriously set when operating with Option 1 of the Successive Calibration Check method

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Table 3. Errata and Information Summary (continued)

Erratum ID	Erratum Title
<a href="#">ERR008082</a>	SENT: A message overflow can lead to a loss of frames combined with NUM_EDGES_ERR being set
<a href="#">ERR007425</a>	SENT: Unexpected NUM_EDGES_ERR error in certain conditions when message has a pause pulse
<a href="#">ERR010645</a>	SIU: WKPCFG is not applied until after initial reset negation
<a href="#">ERR009658</a>	SPI: Inconsistent loading of shift register data into the receive FIFO following an overflow event
<a href="#">ERR007431</a>	STCU2: LBIST does not accept programmable seed value
<a href="#">ERR007339</a>	STCU2: STCU2 fault injected by FCCU is self clearing
<a href="#">ERR010636</a>	STCU: Improper behavior in some cases at hot temperatures during offline LBIST and MBIST operation.
<a href="#">ERR010808</a>	STCU: Chip may get stuck-in-reset if PLL Loss-of-Lock occurs during STCU Offline Self-Test
<a href="#">ERR010443</a>	STCU: Improper behavior in some cases when external reset is asserted during LBIST execution
<a href="#">ERR010025</a>	SWT: System clock source must be set to IRC prior to changing SWT clock selection
<a href="#">ERR009336</a>	TDM: Erase of TDR flash block may be blocked by the TDM - CSE systems
<a href="#">ERR007236</a>	XBIC: XBIC may trigger false FCCU alarm
<a href="#">ERR008310</a>	XBIC: Crossbar Integrity Checker may miss recording information from an initial fault event in the case of back-to-back faults
<a href="#">ERR008730</a>	XBIC: XBIC may store incorrect fault information when a fault occurs
<a href="#">ERR010436</a>	ZipWire: SIPI can have only one initiator with one outstanding write frame at time

# Known Errata

## ERR010443: STCU: Improper behavior in some cases when external reset is asserted during LBIST execution

### Description

If the external reset pin (RESET) is asserted during Self-Test Control Unit (STCU) Logic Built-In Self Test (LBIST) execution, incorrect operation may be observed in some cases. This incorrect operation will have one of two possible effects:

(1) Following external reset assertion, the device will be unable to read Device Configuration Format (DCF) records and will experience the STCU initialization timeout of 8.6ms, after which DCF records will load correctly and normal operation will resume. after which DCF records will load correctly and normal operation will resume.

(2) Following external reset assertion, the device will reload DCF records and attempt to restart self test procedure. It will, however, be unable to restart self test and will experience the STCU watchdog timeout programmed in the STCU2 Watchdog Register Granularity (STCU2\_WDG). After this timeout, the device will reset and not attempt self test execution again. Normal operation will resume.

Effect #1 will be observed in either online or offline (or both) execution of one or more LBIST partitions and the external reset is asserted during LBIST execution of partition 0, 1, 2, 3, or 4. This case occurs regardless of whether MBIST is configured or not.

Effect #2 will be observed if offline execution of one or more MBIST partitions is configured and offline or online execution (or both) of one or more LBIST partitions is performed and the external reset pulse is asserted during test of LBIST partition 5.

All other combinations of self test execution online or offline (or both) are not affected by this issue.

### Workaround

For effect #1: After normal operation resumes, the device will report the cause of reset as external reset in System Integration Unit Reset Status Register (SIU\_RSR). STCU status registers will indicate no self-test has executed. At this point, the application can either re-run self test online or, if possible, signal an external device to apply external reset in order to cause offline self-test to run again.

For effect #2:

Ensure that the BIST watchdog timer (STCU2\_WDG[WDGEOC]) is properly initialized to limit the amount of time that the device will remain in reset due to this issue. The maximum value for the watchdog (0xffff\_ffff) causes a very long timeout and the device may appear to be stuck in reset indefinitely. For example, if the system clock is configured to 50MHz for the test execution and STCU clock configuration (STCU2\_CFG[CLK\_CFG]) is set to divide-by-2, the watchdog timeout period will be  $(0xffff\_ffff * 16 \text{ STCU clocks}) / 12.5\text{MHz}$  or about 1.5 hours.

## ERR009087: PADRING: Input High Voltage (max) and Hysteresis (min) specs not met

### Description

The datasheet specifications for Input High Voltage,  $V_{ih}$  (max), and Hysteresis (min) are not met in this device.

The original specifications are:

$V_{ih} \text{ max} = (0.55 * VDDE).$

$V_{ih} \text{ max with hysteresis enabled} = (0.65 * VDDE).$

$\text{Hysteresis min} = (0.10 * VDDE).$

The actual values met by this device are:

$V_{ih} \text{ max} = (0.57 * VDDE).$

$V_{ih} \text{ max with hysteresis enabled} = (0.67 * VDDE).$

Hysteresis min = (0.09 \* VDDE).

#### Workaround

Ensure that external devices connected as inputs are compatible with these actual input level specifications. A future revision of the datasheet will be updated to reflect these new values.

## ERR008164: MPC577xC: Current injection causes leakage path across the DSPI and LFAST LVDS pins

#### Description

The General Purpose Input/Output (GPIO) digital pins (including all digital CMOS input or output functions of the pin) connected to the differential LVDS drivers of the Deserial/Serial Peripheral Interface (DSPI), high-speed debug, and LVDS Fast Asynchronous Serial Transmit Interface (LFAST) do not meet the current injection specification given in the operating conditions of the device electrical specification. When the LVDS transmitter or receiver is disabled and current is positively or negatively injected into one pin of the GPIO pins connected to the differential pair, a leakage path across the internal termination resistor of the receiver or through the output driver occurs potentially corrupting data on the complementary GPIO pin of the differential pair. All LFAST and DSPI LVDS receive and transmit GPIO pairs on the MPC577xC exhibit the current injection issue.

There is an additional leakage path for the LFAST receive pins through the loopback test path when current is negatively injected into a GPIO pin connected to an LFAST pair. In this case current will be injected into the same terminal of the GPIO pin connected through the loopback path (positive terminal to positive terminal, negative terminal to negative terminal). The pins affected by the loopback path on the MPC577xC are: SIPI\_TXP to/from SIPI\_RXP, and SIPI\_TXN to/from SIPI\_RXN.

There is no leakage issue when the pins are operating in normal LVDS mode (both LVDS pairs of the LFAST interface configured as LVDS).

#### Workaround

As long as the GPIO pad pins are operated between ground (VSS) and the Input/Output supply (VDDEHx) then no leakage current between the differential pins occurs. If the GPIO pad is configured as an input buffer then DC current injection must be limited to a maximum of 2.5mA. In this case, the adjacent CMOS pin will see a shift in the VOH/VOL levels and A/C timing if configured as an output. If the GPIO pad is configured as an output care should be taken to prevent undershoot/overshoot/ringing during transient switching of capacitive loads. This can be done by carefully configuring the output drive strength to the capacitive load and ensuring board traces match the characteristic impedance of the output buffer to critically damp the rising and falling edges of the output signal.

## ERR009338: eTPU: Time base counter values can fail to export properly

#### Description

Time base counters from the Enhanced Time Processor Unit (eTPU) may sometimes fail to export on the Shared Time and Angle Counter (STAC) bus to other eTPU engines or to the Enhanced Modular Input Output Subsystem (eMIOS). This issue can occur when the clock ratio between eTPU and eMIOS is switched from 1:1 to 2:1 (in other words, when the eTPU operates at twice the frequency of the eMIOS).

#### Workaround

The reset default clock ratio for eTPU:eMIOS is 1:1. If the application requires switching to 2:1 clock ratio, perform this clock ratio switch early in the application initialization procedure while the system clock is still being driven by the Internal RC Oscillator (IRCOSC) and before any other changes are made to any Phased Lock Loop (PLL) or System Integration Unit (SIU) system clock tree divider settings.

Perform a single write to the SIU System Clock Register eTPU Divider (SIU\_SYSDIV[ETPUDIV] = 1). This switches the clock ratio from 1:1 to 2:1 in such a way that the STAC bus logic can properly register the change in clock ratios. Once this change has been

made, ensure that no other subsequent writes to the SIU\_SYSDIV register change the value of the ETPUDIV field from 1 back to 0 until the next reset event. Writes to other fields in SIU\_SYSDIV are allowed and will not affect this workaround.

## ERR010436: ZipWire: SIPI can have only one initiator with one outstanding write frame at time

### Description

The Serial Inter-processor Interface (SIPI) module of the Zipwire interface only supports one initiator and one outstanding write frame at a time.

If a new write is initiated (by setting SIPI\_CCRn[WRT] = 0b1, where n is the respective channel number for the transmission), or a new streaming write is initiated (by setting SIPI\_CCRn[ST] = 0b1) with acknowledgement of a previous frame pending, then the initiator node may get a timeout error (indicated by SIPI\_ERR[TOEn]=0b1). The previous write frame last byte may also be corrupted at the target node.

This also means that the target node cannot initiate a write transfer while the initiator node is in the process of a write transfer.

### Workaround

The initiator should maintain only one outstanding write/streaming write frame to the target node at any one time.

The user must ensure that before initiating a new write request or initiating a new streaming write that it has received an acknowledgement for the previous write transaction (indicated by SIPI\_CSRn[ACKR] = 0b1). The write acknowledgement interrupt can be enabled by setting SIPI\_CIRn[WAIE]=0b1.

Implement a protocol that ensures both sides of the link cannot initiate a transfer at the same time. For example, a token-passing protocol could be implemented using the SIPI trigger command feature. Send a trigger command to pass the token to the other end of the link. Upon receipt of the trigger command, either initiate a write transfer if one is pending, or pass the token back by sending a trigger command. If a write transfer is initiated, wait until ACK is received and then send a trigger command to pass the token back. In this manner, if each side agrees only to initiate a transfer when it obtains the token, there will be no simultaneous transfers that can cause the problem described.

## ERR010714: MPC577xC: Lockstep errors must be ignored when debugging core 1 in lockstep mode

### Description

When debugging core 1 in lockstep mode, Fault Collection and Control Unit (FCCU) faults NCF 10 and/or NCF 11 (Safety core out of sync) may be indicated. These are not real faults in the hardware but are instead due to debug tool access.

### Workaround

In the FCCU, do not configure NCF 10 and NCF 11 reactions to generate a reset. Instead, use an interrupt reaction and program the interrupt handler to ignore these faults when debug mode is in use.

## ERR050016: M\_CAN: Retransmission in DAR mode due to lost arbitration at the first two identifier bits

### Description

When the Modular Controller Area Network module (M\_CAN) is configured in DAR mode (CCCR.DAR = '1') the Automatic Retransmission for transmitted messages that have been disturbed by an error or have lost arbitration is disabled. When the transmission attempt is not successful, the Tx Buffer's transmission request bit (TXBRP.TRPxx) shall be cleared and its cancellation finished bit (TXBCF.CFxx) shall be set. When the transmitted message loses arbitration at one of the first two identifier bits, it may happen, that instead of the bits of the actually transmitted Tx Buffer, the TXBRP.TRPxx and TXBCF.CFxx bits of the previously started Tx Buffer (or Tx Buffer 0 if there is no previous transmission attempt) are written (TXBRP.TRPxx = '0', TXBCF.CFxx = '1'). If in this case the TXBRP.TRPxx bit of the Tx Buffer that lost arbitration at the first two identifier

bits has not been cleared, retransmission is attempted. When the M\_CAN loses arbitration again at the immediately following retransmission, then actually and previously transmitted Tx Buffer are the same and this Tx Buffer's TXBRP.TRPxx bit is cleared and its TXBCF.CFxx bit is set.

This erratum is limited to the case when the M\_CAN loses arbitration at one of the first two transmitted identifier bits while in DAR mode. The problem does not occur when the transmitted message has been disturbed by an error.

#### Workaround

No workaround is necessary as there is no lasting impact to this erratum. When this issue occurs, only one retransmission attempt will be made.

## ERR011321: PIT\_RTI: Generates false RTI interrupt on re-enabling

#### Description

A false Real-Time Interrupt (RTI) may be observed when the RTI module is re-enabled if, after servicing an RTI interrupt (by clearing TFLGn[TIF]), the clocks to the RTI module are disabled.

This occurs only if the RTI module clock is disabled within four RTI clock cycles of an RTI Interrupt being cleared.

#### Workaround

Option 1: The user should check the RTI interrupt flag, TFLGn[TIF] before servicing the interrupt, this flag won't be set for the false/spurious interrupts.

Option 2: Ensure that the module clock to the RTI module is not disabled within four RTI clock cycles after servicing an RTI interrupt. Consult the chip-specific documentation to determine the clock period of the RTI module and implement a time delay of at least five times this period before disabling the RTI module clock.

## ERR006726: NPC: MCKO clock may be gated one clock period early when MCKO frequency is programmed as SYS\_CLK/8 and gating is enabled

#### Description

The Nexus auxiliary message clock (MCKO) may be gated one clock period early when the MCKO frequency is programmed as SYS\_CLK/8 in the Nexus Port Controller Port Configuration Register (NPC\_PCR[MCKO\_DIV]=111) and the MCKO gating function is enabled (NPC\_PCR[MCKO\_GT]=1). In this case, the last MCKO received by the tool prior to the gating will correspond to the END\_MESSAGE state. The tool will not receive an MCKO to indicate the transition to the IDLE state, even though the NPC will transition to the IDLE state internally. Upon re-enabling of MCKO, the first MCKO edge will drive the Message Start/End Output (MSEO=11) and move the tool's state to IDLE.

#### Workaround

Expect to receive the MCKO edge corresponding to the IDLE state upon re-enabling of MCKO after MCKO has been gated.

## ERR010439: CMU: CMU\_0 OLR is set out of reset when XOSC used in 8mhz mode, due to wrong RCDIV reset value

#### Description

Clock Monitor Unit 0 (CMU\_0) asserts "Oscillator frequency less than reference" (OLR) event coming out of reset when the crystal oscillator (XOSC) is used in 8MHz mode, resulting in Fault Collection and Control Unit (FCCU) fault NCF 25 being set. This is because the reset value of the Reference Clock Divider CMU\_0\_CSR[RCDIV] = 0x0 (instead of 0x3), resulting in XOSC clk (8MHz) < IRC (16MHz).

### Workaround

Before enabling FCCU NCF 25 event, clear OLRI bit by writing CMU\_0\_CSR[RCDIV] to 0x3 first and then CMU\_ISR[OLRI] to 1 (the bit is write-1-to-clear).

## ERR011479: MPC577xC: PLLCFG2 toggling during reset may cause incorrect XOSC operation

### Description

If the user is toggling the pin PLLCFG2 during reset, the crystal oscillator (XOSC) may go into an unsettled state and delay crystal startup. This can occur regardless of the setting of the Legacy Mode (LEG) bit in the UTEST Miscellaneous Device Configuration Format (DCF) record.

### Workaround

In order to avoid increased startup time for the crystal oscillator, do not toggle the pin PLLCFG2 during reset.

## ERR009517: MCAN: Edge filtering may cause incorrect frame reception

### Description

The MCAN may fail to correctly receive the first bit of the frame when edge filtering is activated in the CAN Core Control Register's Edge Filtering during Bus Integration field (CCCR.EFBI = '1') and when the end of the integration phase coincides with a falling edge at the receive (Rx) input pin. In this case, the Cyclic Redundancy Check (CRC) will detect that the received frame is faulty and an error frame will be sent.

When that frame is re-transmitted, the integration phase has finished and the frame is received correctly. Edge filtering is only applied during the integration phase. It is never used during normal operation.

The MCAN enters integration phase under the following conditions:

- When the Initialization control field (CCCR.INIT) is set to '0' after start-up
- After a protocol exception event where protocol exception handling is enabled (CCCR.PXHD = 0)

### Workaround

Disable edge filtering or expect re-transmissions when this issue occurs.

## ERR010453: MPC577xC: Reduced accuracy on EQADC\_B channels using VDDEH7 power domain

### Description

Analog inputs for the Enhanced Queued Analog to Digital Converter B (EQADC\_B) which are on the VDDEH7 power domain, including channels ANB[8:23] and ANB[40-45] may experience higher Total Unadjusted Error (TUE) due to noise coupling in the pad ring. This effect can occur when other input/output pins on the same VDDEH7 power domain are being driven. These may be output signals from internal peripheral modules or general purpose Input/Output. Input signals, if driven to the minimum or maximum allowable voltage levels may also cause the effect.

At 16MHz ADC sampling frequency, there is no impact to the TUE specification.

At 32MHz ADC sampling frequency, the impact to TUE specification is as follows:

- Worst case condition is cold temperature (-40C), where the TUE impact is an additional 6 counts (total of 14 counts).
- At room(25C) or hot (150C) junction temperature, the impact is lessened, with the TUE affected by an additional 4 counts (total of 12 counts).

The magnitude of the additional error is application-specific and depends on the usage of VDDEH7 domain input/output signals.

#### Workaround

If possible, use a sampling frequency of 16MHz or less with these inputs. If not, use averaging of multiple samples on these channels to reduce error impact and/or assign inputs with less need for accuracy to these channels. Move those requiring more sensitive measurements to EQADC\_A channels or to unaffected EQADC\_B channels that are on the VDDA\_EQ supply domain.

### **ERR007230: FCCU: FCCU\_IRQ\_EN[28] is writeable, but reserved.**

#### Description

The Fault Collection and Control Unit (FCCU) Interrupt (IRQ) Enable Register (FCCU\_IRQ\_EN) bit position 28 is writable, even though the bit is documented as reserved.

#### Workaround

Expect the FCCU\_IRQ\_EN[28] bit to be writable, not reserved. For future compatibility software should set this bit to the reset value of 0b0 any time this register is written.

### **ERR007227: FCCU: FCCU Output Supervision Unit (FOSU) will not monitor faults enabled while already pending**

#### Description

The Fault Collection and Control Unit (FCCU) Output Supervision Unit (FOSU) will not monitor the FCCU reaction to fault inputs that are enabled with an already pending notification. The FOSU monitoring is triggered by an edge from a fault input. The edge detection will be blocked in following cases:

- 1) When a fault input occurs before it is enabled in the FCCU.
- 2) When a fault input is enabled in the FCCU and a fault occurs in the CONFIG state.

FOSU edge detection remains blocked until it gets initialized by a FCCU reaction or a destructive reset.

#### Workaround

Case 1: Before enabling a fault, check if any fault is pending in the corresponding Noncritical Fault Status Register (FCCU\_NCF\_Sx). If it is any pending, implement one of the workarounds below. Regardless of whether or not the faults are pending and after implementing the workaround (if necessary) subsequently enabling the desired fault will require entering CONFIG mode where it is possible to have Case 2 occur. So proceed to Case 2 handling next.

Case 2: Any time FCCU CONFIG mode is entered for any reason, check for pending faults immediately after exiting CONFIG mode. If any fault is pending, implement one of the workarounds below.

Workaround 1: Generate interrupt FCCU reaction by any fault to recover FOSU monitoring of the pending faults using the Noncritical Fake Fault register (FCCU\_NCFF)

Workaround 2: Generate a destructive reset.

Caveat: If the fault in question is found to be pending immediately after reset, then workaround 2 is ineffective and workaround 1 must be employed.



## ERR007869: FCCU: FOSU monitoring of a fault is blocked for second or later occurrence of the same fault

### Description

The Fault Collection and Control Unit (FCCU) Output Supervision Unit (FOSU) will not monitor the FCCU for the second or later occurrence of a given fault in the following cases:

1. Reset is programmed as the only reaction for the fault.
2. Assertion of the fault coincides with the long/short functional reset reaction to a fault previously asserted.

### Workaround

Enable either Alarm state (NCFTOEx) or at least one other type of Fault-state reaction: Non-maskable Interrupt (NMI) or error out (EOUT) signaling reaction for the faults that have a reset reaction enabled only. Restrictions of combining reset reaction with additional reactions may be written in the chip specific sub-section of the FCCU chapter.

## ERR011030: PMC: Self Test can repeat when clearing the result flag

### Description

During a normal Power Management Controller (PMC) Self Test of all of the Low-Voltage Detect / High-Voltage Detect (LVD/HVD) events, initiated by writing 2'b01 to the Self Test Mode field of the Voltage Detect User Mode Register (PMC\_SELF\_TEST\_UM\_VD\_REG[ST\_MODE]), the self test completes and clears the ST\_MODE field automatically. However, during a single LVD/HVD test, initiated by writing a non-zero value into the Voltage Detect Self Test Control field (PMC\_SELF\_TEST\_UM\_VD\_REG[VD\_ST\_CTRL]), the ST\_MODE bits do not clear automatically when the test completes. If the self test result flag (PMC\_SELF\_TEST\_UM\_VD\_REG[ST\_RESULT]) is cleared without first clearing the ST\_MODE field, the self test will run again.

### Workaround

When testing individual LVD/HVDs via the PMC Self Test, clear the ST\_MODE field manually via software after the test completes and then clear the ST\_RESULT flag.

## ERR050789: M\_CAN: Dedicated Tx Buffers configured with the same Message ID are not transmitted in order of lowest buffer number first

### Description

When several Tx Buffers are configured with the same Message ID and transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests, it may happen that the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first) when there will be two or more TX requests with the same Message ID pending.

### Workaround

In case a defined order of transmission is required:

- 1) Use the TXBAR features:
  - a. Write the group of Tx message buffers with same Message ID to the Message RAM
  - b. Request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request.
- 2) Tx buffers shall be requested in ascending order with lowest buffer number first.
- 3) A single Tx Buffer can be used to transmit those messages one after the other.
- 4) The Tx FIFO shall be used for transmission of messages with the same Message ID.

## ERR010396: PASS: Password challenge to PASS fails while program erase ongoing in any block in memory partition 0

### Description

If the device is in a Censored state (enabled by programming the censorship DCF in UTEST) and a JTAG password is configured to enable device debug access, then the password challenge to the PASS module would be initiated by programming the Challenge Selector Register (PASS\_CHSEL) to determine the password group, then programming the Challenge Input Registers (PASS\_CINn) with the correct password. Programming the correct password would then allow enabling of debug interface access.

However, this operation will fail if a program or erase operation is ongoing on any flash block in memory partition 0, since this is shared with the UTEST block where the JTAG password resides.

### Workaround

Users should ensure that no program or erase operations are occurring on any memory partitions shared with the UTEST block before initiating a password challenge. This can be monitored through the flash module configuration register program and erase status bits (C55FMC\_MCR[PGM], C55FMC\_MCR[ERS]).

## ERR007352: DSPI: reserved bits in slave CTAR are writable

### Description

When the Deserial/Serial Peripheral Interface (DSPI) module is operating in slave mode (the Master [MSTR] bit of the DSPI Module Configuration Register [DSPIx\_MCR] is cleared), bits 10 to 31 (31 = least significant bit) of the Clock and Transfer Attributes Registers (DSPIx\_CTARx) should be read only (and always read 0). However, these bits are writable, but setting any of these bits to a 1 does not change the operation of the module.

### Workaround

There are two possible workarounds.

Workaround 1: Always write zeros to the reserved bits of the DSPIx\_CTARn\_SLAVE (when operating in slave mode).

Workaround 2: Mask the reserved bits of DSPIx\_CTARn\_SLAVE when reading the register in slave mode.

## ERR050130: PIT: Temporary incorrect value reported in LMTR64H register in lifetimer mode

### Description

When the Programmable interrupt timer (PIT) module is used in lifetimer mode, timer 0 and timer 1 are chained and the timer load start value (LDVAL0[TSV] and LDVAL1[TSV]) is set according to the application need for both timers. When timer 0 current time value (CVAL0[TVL]) reaches 0x0 and subsequently reloads to LDVAL0[TSV], then timer 1 CVAL1[TVL] should decrement by 0x1.

However this decrement does not occur until one cycle later, therefore a read of the PIT upper lifetime timer register (LTMR64H) is followed by a read of the PIT lower lifetime timer register (LTMR64L) at the instant when timer 0 has reloaded to LDVAL0[TSV] and timer 1 is yet to be decremented in next cycle then an incorrect timer value in LTMR64H[LTH] is expected.

### Workaround

In lifetimer mode if the read value of LTMR64L[LTL] is equal to LDVAL0[TSV] then read both LTMR64H and LTMR64L registers one additional time to obtain the correct lifetime value.

## ERR006990: CJTAG: possible incorrect TAP state machine advance during Check Packet

### Description

While processing a Check Packet, the IEEE 1149.7 module (CJTAG) internally gates the TCK clock to the CJTAG Test Access Port (TAP) controller in order to hold the TAP controller in the Run-Test-Idle state until the Check Packet completes. A glitch on the internally gated TCK could occur during the transition from the Preamble element to the first Body element of Check Packet processing that would cause the CJTAG TAP controller to change states instead of remaining held in Run-Test-Idle

If the CJTAG TAP controller changes states during the Check Packet due to the clock glitch, the CJTAG will lose synchronization with the external tool, preventing further communication.

### Workaround

To prevent the possible loss of JTAG synchronization, when processing a Check Packet, provide a logic 0 value on the TMS pin during the Preamble element to avoid a possible glitch on the internally gated TCK clock.

## ERR008710: SDADC: Watchdog Crossover event missed if FM Peripheral Clock frequency is less than or equal to the sigma-delta ADC clock frequency

### Description

In the Sigma-Delta Analog-to-Digital Converter (SDADC), the watchdog monitor Lower and Higher threshold crossover events may get missed if the FM peripheral clock (FM\_PER\_CLK) has a frequency less than or equal to the SDADC clock (SD\_CLK). Therefore, the Watchdog Upper Threshold Cross Over Event (WTHH) and Watchdog Lower Threshold Cross Over Event (WTHL) bits of the Status Flag Register (SDADC.SFR) may not be set and the corresponding Direct Memory Access (DMA) or interrupts are not triggered.

### Workaround

When setting the different clocks in the System Integration Unit (SIU), ensure that FM\_PER\_CLK frequency is always greater than SD\_CLK. This includes the variation in FM\_PER\_CLK due to frequency modulation, if enabled.

## ERR009320: FLASH: (SPC5777C) Address Encode False Report (MCR[AEE] and possible FCCU channels)

### Description

During Flash Read while Write operations (RWW), it is possible for a Program or Erase operation to corrupt the Address Encode feature of the flash, and falsely give an Address Encode Error (AEE) event. The false AEE event only occurs for RWW operations to partitions in the Low, Mid or High address spaces, and may only occur if the read and write occur both in Even RWW partitions (i.e. 0, 2, or 4), or if the read and write occur both in Odd RWW partitions (i.e. 1, 3, or 5).

Reads to even numbered RWW partitions while writing to odd numbered RWW partitions will not trigger this false AEE condition. Likewise, reads to odd numbered RWW partitions while writing to even numbered RWW partitions will not trigger this false AEE condition.

Reads and Writes to 256K blocks, do not show the address encode corruption issue.

Read Data and ECC Parity bits returned for these Reads while writing are valid and not corrupted.

### Workaround

Disable the Fault Collection and Control Unit (FCCU) Failure input channels 31 and 32 by clearing the corresponding bits in the Non-Recoverable Fault Enable Registers 0 and 1 (FCCU\_NCF\_E0 and FCCU\_NCF\_E1). FCCU input channel 31 is the Encoding Error Flash, and covers the C55FMC\_MCR[AEE] event indication in addition to Flash Read Voltage Error (C55FMC\_MCR[RVE])

and Flash Read Reference Error (C55FMC\_MCR[RRE]) indications and is controlled by the FCCU\_NCF\_E0[bit 0]. FCCU input channel 32 is the flash controller address feedback event indication and is controlled by the FCCU\_NCF\_E1[bit 31].

Address Encode Error (AEE) fault recognition is a safety mechanism used to detect potential permanent and transient faults in the flash address decode logic. Even with AEE detection disabled, most faults that would be detected by AEE are still detected by other mechanisms as part of the MPC57xxM redundant safety concept. Consequently, disabling the AEE fault notifications in the FCCU has no impact to the overall functional safety integrity of the device, and the ISO26262 ASIL D target is achieved.

With the FCCU channels 31 and 32 disabled, the Read Voltage Error and Read Reference error may be monitored by reading the fields from the Flash Module Configuration register (C55FMC\_MCR[RVE], C55FMC\_MCR[RRE]).

## ERR001147: DSPI: Using DSPI in DSI mode with MTO may cause data corruption

### Description

Using the DSPI in Deserial Serial Interface (DSI) Configuration (DSPIx\_MCR[DCONF]=0b01) with multiple transfer operation (DSPIx\_DSICR[MTOE=1]) enabled, may cause corruption of data transmitted out on the DSPI master if the clock Phase is set for leading edge capture DSPIx\_CTARn[CPHA]=0. The first bit shifted out of the master DSPI into the slave DSPI module will be corrupted and will convert a '0' to read as a '1'.

### Workaround

There are three possible workarounds for this issue.

- 1) Select CPHA=1 if suitable for external slave devices.
- 2) Set first bit to '1', or ignore first bit. This may not be a workable solution if this bit is required.
- 3) Connect SOUT from the master to SIN of the first slave externally instead of using internal signals. This is achieved by setting the DSPI Input Select Register (SIU\_DISR) to set the SINSELx field of the first slave DSPI to '00' and configuring this slave's SIN pin and master SOUT pin as DSPI SIN/SOUT functions respectively. This workaround is suitable only if these two signals are available to be connected externally to each other.

## ERR008082: SENT: A message overflow can lead to a loss of frames combined with NUM\_EDGES\_ERR being set

### Description

In the case of a Single Edge Nibble Transfer (SENT) receiver (Rx) message overflow (CHn\_STATUS[FMSG\_OFLW] = 1) and if the following registers are continuously being read without clearing the FMSG\_RDY[F\_RDYn] bit, there is a possibility that one message will be lost. Additionally, if the pause pulse feature is enabled, the module assert up to two NUM\_EDGES\_ERR in the status register (CHn\_STATUS). In this case up to two frames can be lost.

Note that some debuggers perform a continuous read of memory which can cause this issue to occur.

Table:

Register	Register Name
CHn_FMSG_DATA	Channel Fast Message Data Read Register
CHn_FMSG_CRC	Channel Cyclic Redundancy Check Register
CHn_FMSG_TS	Channel Fast Message Time-stamp Register

### Workaround

1. Software should ensure that SENT message overflow does not occur.

If interrupts are used (when the Enable FDMA (FDMA\_EN) bit of Fast Message DMA Control Register (SRX\_FDMA\_CTRL) is set to 0 ) to read the SENT messages, the interrupt for data reception should be enabled by setting the Enable for Fast Message Ready Interrupt (FRDY\_IE[n]) bit of Fast Message Ready Interrupt Control Register (SRX\_FRDY\_IE) for every channel n and the interrupt priority should be such that the software is able to read the message before the next message arrives.

When using Direct Memory Accesses (eDMA) to access the SENT (when the Enable FDMA (FDMA\_EN) bit of Fast Message DMA Control Register (SRX\_FDMA\_CTRL) is set to 1), the DMA request from the SENT module should be serviced before the next message arrives.

The minimum duration between the reception of two consecutive messages in one channel is 92 times the utick length (time).

2. Ensure that the following registers are not read continuously either in the software code or as a result of a debugger being connected. The following registers should be read once per message and the FMSG\_RDY[F\_RDYn] bit should be cleared after the reads.

Table:

Register	Register Name
CHn_FMSG_DATA	Channel Fast Message Data Read Register
CHn_FMSG_CRC	Channel Cyclic Redundancy Check Register
CHn_FMSG_TS	Channel Fast Message Time-stamp Register

## ERR010636: STCU: Improper behavior in some cases at hot temperatures during offline LBIST and MBIST operation.

### Description

At hot temperatures, the JTAG Compliance (JCOMP) input pin is not effectively pulled down internally and may prevent the Self-Test Control Unit (STCU) from performing a configured off-line self-test operation (MBIST and/or LBIST).

### Workaround

After normal operation resumes after a reset, the device will report the cause of reset as a reset in the System Integration Unit Reset Status Register (SIU\_RSR). STCU status registers may indicate that no self-test has executed. At this point, the application can re-run self-test in online mode.

## ERR010226: PMC: In SMPS mode, during input supply power down, core voltage can exceed specification limits

### Description

When the Switch Mode Power Supply (SMPS) of the Power Management Controller (PMC) is used for internal regulation and the PMC input supply (VDDPMC) ramps down, the output of the regulator (core voltage supply) may briefly rise above specification limits for a duration which is dependent on the ramp down rate. This core over-voltage condition may, over time, cause reliability issues with the device.

The issue is more likely to occur when:

- 1) VDDPMC and VDDPWR (PMC SMPS driver supply) supply inputs are driven from different sources and VDDPMC ramps down before VDDPWR. Note that on some devices these two supplies are required to be tied together. Refer to the device data sheet.
- 2) In the case where VDDPMC/VDDPWR are tied together, the problem is most likely to occur when the ramp down time is long, that is, for slow ramp down rates.

The issue occurs when the PMC stops driving the Regulator Control (REGCTL) output while it is in the low (on) position. This leaves the external p-MOSFET device on until the pull-up resistor can shut the device off. For large values of the resistor, this can require enough time that the core voltage output of the regulator briefly drives above specification limits.

### Workaround

An external pull-up resistor in the range of 2K to 4.7K ohms must be used between REGCTL and VDDPWR.

VDDPMC and VDDPWR supplies must ramp down through the voltage range from 2.5v to 1.5v in less than 1 second. Slower ramp down times may result in reduced lifetime reliability of the device

## ERR006906: SDADC: Invalid conversion data when output settling delay value is less than 23

### Description

In the Sigma Delta Analog to Digital Converter (SDADC), if the Output Settling Delay field of the Output Settling Delay register (OSDR[OSD]) is programmed to a value less than 23 then the initial converted data from SDADC block is "0000" instead of the correct conversion result.

### Workaround

Program the OSDR[OSR] value equal to or greater than 23.

## ERR011048: PMC: When using an external regulator and a reset occurs, the core supply voltage needs to be above 1.22V and below 1.300V to exit from reset

### Description

When using an external regulator, if any type of reset occurs while the core supply voltage (VDD) is below 1.22V, VDD will have to rise above 1.22V before the device will exit from reset. Similarly, if when using an external regulator and VDD is above 1.300V when a reset occurs, VDD will have to fall below 1.300V before the device will exit from reset.

This issue also applies to initial power-on reset of the device since it begins in reset below 1.22V. Core voltage detectors may not release reset until VDD is above 1.22V initially. Ramp rate of 200V/s or more avoids the power up issue.

Note that this issue does not affect falling Low-Voltage Detect and rising High-Voltage Detect (LVD/HVD) entry threshold levels during normal operation. These voltage levels remain as specified in the datasheet. This issue occurs only when any type of reset, for example an external RESET pin assertion, occurs while at the same time the core voltage is below 1.22V or above 1.300V.

### Workaround

Disable the Core Cold LVD and Core HVD via the Reset Event Enable Control (REE CTRL) DCF client bit 0 (for Core Cold LVD) and bit 2 (for Core HVD) and then enable both of these events in software by writing to the Core Cold LVD and Core HVD bits of the Power Management Controller Reset Event Enable (PMC\_REE) register.

## ERR006992: PSI5: IS\_DEBUG\_FREEZE bit is not documented

### Description

Bit 0 (the most significant bit of the register, MSB) of the Peripheral Sensor Interface 5 General Interrupt Status Register (PSI5\_GISR) is not documented. This bit is the IS\_DEBUG\_FREEZE bit and is set when the PSI5 module is stopped in debug freeze mode. To enable the debug freeze mode, both PSI5 Debug mode Enable and the Debug Freeze Control bits must be set in the PSI5 Channel Control register (PSI5\_PCCR[DEBUG\_EN] = 0b1 and PSI5\_PCCR[DEBUG\_FREEZE\_CTRL] = 0b1). When the PSI5 module receives the request to enter the debug mode, it finishes the current processing and is stopped coherently. At this stage, the IS\_DEBUG\_FREEZE bit is set to "1". This bit automatically gets cleared by the hardware when the debug mode is exited.

### Workaround

Expect bit 0 (MSB) of the PSI5\_GISR register to be set when the PSI5 module is stopped in debug freeze mode if both DEBUG\_EN and DEBUG\_FREEZE\_CTRL are set. The documentation will be updated.

## ERR051156: CSE: BOOT\_MAC calculation is done only on [DATA] during secure boot

### Description

When the BOOT\_MAC is calculated according to the SHE specification the SECURE\_BOOT command fails. The reason is that the specification defines the MAC calculation over ["0..0"96|SIZE|DATA] but the CSE calculates the MAC during the secure boot process only over the [DATA].

When the first secure boot is executed and the BOOT\_MAC is not programmed on the device then the CSE will calculate it (only over the [DATA]) and store it automatically into the BOOT\_MAC slot.

### Workaround

BOOT\_MAC must be calculated only over the [DATA].

## ERR010844: PMC: During PMC Self Test, an external reset or FOSU reset could cause a POR type reset instead

### Description

While the Power Management Controller (PMC) self test is running in either the default mode (power on) or software-triggered mode and an external reset (from RESET pin) or a Fault Collection and Control Unit Output Supervisor Unit (FOSU) reset occurs, a Power-On Reset (POR) may result.

### Workaround

The only noticeable impact of this issue is that the System Integration Unit Reset Status Register (SIU\_RSR) will report a POR reset source rather than an external or FOSU reset source. All three of these reset sources result in a reset of all internal modules and require software to do full reinitialization. Thus no software workaround is possible or necessary. External testing that may be checking reaction to RESET pin or FOSU reset sources needs to be aware that this issue can cause misidentification of the reset source. No other action is necessary.

## ERR010798: MPC577xC: Asserting RESET pin input while Software System Reset is in progress prevents offline self-test from running

### Description

This issue applies only when Device Configuration Format (DCF) records are programmed to enable offline Self-Test Control Unit (STCU) self-test.

When the RESET input pin is asserted while a previous Software System Reset is still being processed, the following unintended effects may occur (as a group):

- STCU offline will not run
- RSTOUT pin will not negate until STCU watchdog times out
- STCU watchdog timeout period, in this case, will be approximately 256ms (with STCU2\_CFG[CLK\_CFG]=001) regardless of programmed timeout value

### Workaround

Start-up code that executes after Software System Reset should read the STCU2\_RUN[RUN] bit. If that bit is set to 1, then the device is in an erroneous state and another RESET input pin assertion should be performed to ensure a clean reset of the STCU with subsequent offline self-test execution.

## ERR002340: FEC: slot time is designed for 516 bit times; deviation from the 802.3

### Description

The Fast Ethernet Controller (FEC) slot time is 516 bit times which is longer than the 512 bit times specified by the IEEE 802.3 standard.

If a collision occurs after the standard 512 bit times (but prior to 516 bit times), the FEC may generate a retry that a remote ethernet device may identify as late. In addition, the slot time is used as an input to the backoff timer, therefore the FEC retry timing could be longer than expected.

### Workaround

No software workaround is needed or available.

## ERR011031: PMC: When a disabled LVD/HVD is tested via PMC Self Test, the self test may fail

### Description

When a Power Management Controller (PMC) Low-Voltage Detect or High-Voltage Detect (LVD/HVD) event is disabled either via a Device Configuration Format (DCF) client or a write to the Reset Event Enable (PMC\_REE) register, the PMC Self Test function still tests this LVD/HVD during the testing process. This may incorrectly indicate a failure in the PMC Self Test results for the disabled LVD/HVD event(s).

This applies to both the automatic PMC self test which runs during reset and any "software triggered self test" run by writing 2b'01 to the Self Test Mode field of the Voltage Detect User Mode Register (PMC\_SELF\_TEST\_UM\_VD\_REG[ST\_MODE]). It would also apply if the application performed a "Single VD test" (ST\_MODE=2b'10) on a disabled LVD or HVD.

In the case of automatic self test during reset, the issue only applies if any LVD/HVD is disabled via DCF client. For self tests initiated by the application software, the issue applies if any LVD/HVD is disabled either by DCF or by PMC\_REE.

### Workaround

If any LVD or HVD is disabled via a DCF client, application software should ignore any PMC Self Test failure results indicated after an exit from reset.

If any LVDs/HVDs are disabled (whether by DCF or by application software writes to PMC\_REE) the application should avoid using the "software triggered self test" option and instead perform "Single VD test" on each LVD/HVD that is enabled, skipping any that are disabled.

## ERR007431: STCU2: LBIST does not accept programmable seed value

### Description

The Logic Built-In Self Test (LBIST) feature is specified to include a Pseudo-Random Pattern Generator (PRPG) load value that would allow a user to experiment with different seed values for running the self-test. This feature is non-functional. A default seed value will be used instead and programming values in registers STCU2\_LB\_PRPG/Hn will have no effect.

### Workaround

The programmable seed value feature cannot be used. This does not affect the usability of the self-test feature as the default seed value is sufficient. Appropriate values for input test cycle length and expected MISR (Multiple-Input Signature Register) result should be found in user documentation for this device.



## ERR008505: FCCU: The FCCU on-chip programmable glitch filter on ERRORIN does not operate correctly

### Description

The Fault Collection and Control Unit (FCCU) external error input (ERRORIN) can be filtered by the FCCU on-chip programmable glitch filter but is routed directly to the FCCU Output Supervision Unit (FOSU) without passing through the glitch filter. In addition, when the glitch filter is programmed using the FCCU Control Register (FCCU\_CTRL) FILTER\_WIDTH field, the effective duration may vary depending on the ERRORIN signal arrival instant.

As a result of these issues, it is possible for the FOSU to recognize an event on ERRORIN that is ignored by the FCCU resulting in a reset when the FOSU timeout period expires.

### Workaround

Bypass the FCCU on-chip glitch filter by writing a 1 to FCCU Control Register FILTER\_BYPASS field (FCCU\_CTRL[FILTER\_BYPASS]). Use an external glitch filter instead of the on-chip filter to ensure that only valid external error events are recognized by the FCCU.

## ERR007546: EBI: Input signal valid to D\_CLKOUT posedge (setup time) spec is not met

### Description

The External Bus Interface (EBI) specification for input signal valid to D\_CLKOUT posedge (setup time) was originally 5ns. This device requires 7ns.

### Workaround

Ensure external devices connected via EBI provide the required input signal setup time.

## ERR009344: eSCI: Late assertion of Transmit Data Ready Interrupt Flag (TXRDY) for Local Interconnect Network (LIN) frame receive (RX) operation

### Description

Assertion of the Transmit Data Ready Interrupt Flag (TXRDY) in the Interrupt Flag and Status Register 2 (eSCI\_IFSR2) indicates that data written to the LIN Transmit Register (eSCI\_LTR) has been processed by the eSCI module. For the first three data writes to the eSCI\_LTR during LIN frame generation, the TXRDY flag is asserted one clock cycle after the write access. During LIN RX operation, assertion of the TXRDY flag that coincides with the fourth data write to the eSCI\_LTR is delayed. The TXRDY flag is not asserted until the LIN RX frame has been completely received from the slave device. The TXRDY flag is asserted when the Frame Complete Interrupt (FRC) flag of the eSCI\_IFSR2 register is asserted.

### Workaround

Application software should expect a delay in the assertion of the TXRDY flag after the fourth data write to the eSCI\_LTR. Instead of expecting TXRDY assertion within one clock cycle of the fourth data write to the eSCI\_LTR, application software should expect assertion of the TXRDY flag after the LIN RX frame has been completely received from the slave device.

## ERR009332: MPC577xC: Performance degradation caused by optimization control bits on Platform Configuration Module

### Description

The "Pending Read Enable" (PRE\_x) optimization option on the Platform Configuration Module (PCM) Bus Bridge Configuration Registers (PCM\_IAHB\_BEn) may introduce a performance degradation in some cases.

On this device, the Cryptographic Services Engine (CSE) and Serial Interprocessor Interface (SIPI) bus masters will always exhibit a degradation if the pending read optimization is enabled for the master port 6 concentrator ( $\text{PCM\_IAHB\_BE2[PRE\_M6]} = 1$ ). The Fast Ethernet Controller (FEC) will exhibit the problem when the Frequency Modulation Peripheral Clock Divider is set to divide-by-two ( $\text{SIU\_SYSDIV[FMPELPERDIV]} = 0$ ) and the pending read optimization is enabled for FEC ( $\text{PCM\_IAHB\_BE2[PRE\_FEC]} = 1$ ).

These pending read enable bits ( $\text{PCM\_IAHB\_BEn[PRE\_x]}$ ) are enabled (set) by default.

#### Workaround

Disable the pending read optimization for the M6 concentrator ( $\text{PCM\_IAHB\_BE2[PRE\_M6]} = 0$ ) if using the CSE and/or SIPI. Disable the pending read optimization for the FEC ( $\text{PCM\_IAHB\_BE2[PRE\_FEC]} = 0$ ) if the FM peripheral clock divider is set to divide-by-2. Other FM peripheral clock ratios are unaffected.

## ERR010011: FCCU: Unexpected faults may be indicated as a result of FCCU reset

#### Description

When a Fault Collection and Control Unit (FCCU) reset occurs (as a result of a fault that is configured for reset reaction), there may be additional faults incorrectly recorded in the FCCU status registers.

#### Workaround

Write software such that it does not depend on the FCCU status registers to contain only real faults after reset. Ignore interrupt-reaction faults when reading FCCU status registers after an FCCU reset. If multiple reset-reaction faults are recorded, be aware that likely only one is a valid fault.

## ERR009090: eTPU: Incorrect eTPU angle counter function under certain conditions

#### Description

The eTPU Angle Counter (EAC) can function incorrectly in some scenarios when all of the following conditions apply:

- EAC Tooth Program Register (TPR), Angle Ticks Number in the Current Tooth field ( $\text{TICKS} = 0$ ) [ $\text{TPR.TICKS} = 0$ ]

and

- Tick Rate Register (TRR) and the eTPU Engine Time Base Configuration Register prescaler field [ $\text{eTPU\_TBR\_TBCR\_ENgn.TCRnP}$ ] satisfy the following condition:

$(\text{TRR} - 1) * (\text{TCRnP} + 1) < 3$ , where TRR is the non-zero 15-bit integer part (the 15 most significant bits).

When the above conditions are met, three possible scenarios can cause the EAC to function incorrectly:

Scenario 1:

1. The EAC is in High Rate Mode,  $\text{TRR} = 1$ , and TPR Missing Tooth Counter field = 0 [ $\text{TPR.MISSCNT} = 0$ ]
2. On an EAC transition from High Rate Mode to Normal mode, a positive value is written to  $\text{TPR.MISSCNT}$
3. The first microcycle in Normal Mode coincides with a tick timing and either

a. A tooth does not arrive

or

b. A tooth arrives

Expected EAC behavior:

a. Nothing happens

or

b. The EAC transitions back to High Rate Mode

Actual (incorrect) EAC behavior:

a. The EAC transitions to Halt Mode, even though  $TPR.MISSCNT > 0$

or

b. The EAC stays in Normal Mode, even though a tooth arrived before expected and  $TPR.MISSCNT > 0$ . The values of  $TPR.MISSCNT$  and  $TPR.LAST$  are reset, even though the EAC does not transition to High Rate Mode.

Scenario 2:

$TCRnP = 0$ ,  $TRR = 1$  (integer part) and a new value is written to  $TPR.MISSCNT$  when the EAC transitions from High Rate Mode to Normal Mode. In this scenario,  $TPR.MISSCNT$  decrements on every microcycle, but the time the EAC takes to transition to Halt Mode is determined by the previous

$TPR.MISSCNT$  value, so that one of the following unique situations is observed:

a.  $TPR.MISSCNT$  reaches zero, but the EAC transitions to Halt Mode only after a number of microcycles equal to the  $TPR.MISSCNT$  value before the write.

b. EAC transitions to Halt Mode with  $TPR.MISSCNT > 0$  while, decrementing  $MISSCNT$  one more time. If  $TPR.MISSCNT > 1$  during the mode transition, the EAC will stay in Halt mode with a non-zero value of  $TPR.MISSCNT$ .

Scenario 3:

1. The EAC transitions to Normal mode from High Rate or Halt Mode

2. The EAC enters Normal mode with  $TPR.LAST = 1$

3. A tooth is received on the second or third microcycle after the EAC transitions to Normal mode. The tooth may be either a physical tooth or a dummy physical tooth generated by setting the Insert Physical Tooth (IPH) field of the TPR register ( $TPR.IPH = 1$ ).

Observed result:

The EAC resets the values of  $TPR.LAST$ ,  $TPR.IPH$  and the eTPU Engine Time Base2 (TCR2) register, but the EAC goes to Halt mode.

If a new  $TPR.TICKS$  value is written with the EAC in Normal mode, the value is effective after a new tooth is received in Halt mode, with TCR2 counting from 0.

### Workaround

Limit the angle tick period to a minimum value that satisfies the condition  $(TRR - 1) * (TCRnP + 1) > 2$ , where TRR is the non-zero 15-bit integer part (the 15 most significant bits).

## ERR011456: M\_CAN: Tx FIFO message sequence inversion

### Description

A message sequence inversion can occur if the following condition occurs. The condition requires that there be two transmit (TX) messages in the TX FIFO and a higher priority non-Tx FIFO message is added, such as to a TX dedicated buffer. The sequence of events is as follows:

Transmission of TX FIFO message 1 is started (from position 1 of the TX FIFO).

A second message is in the second position of the TX FIFO

The message buffer then contains:

Position 1: TX FIFO message 1 (transmission ongoing)

Position 2: TX FIFO message 2

Position 3: -

A higher priority non-TX FIFO message is input into the CAN module and will be the next message to be transmitted. This message will be inserted into the message flow after the message that is being transmitted and the previous second message is pushed down in the transmission buffer.

After the following two message scans the output pipeline has the following content:

Position 1: TX FIFO message 1 (transmission ongoing)

Position 2: non TX FIFO message with higher CAN priority

Position 3: TX FIFO message 2

If the first message that is being transmitted is not successful, due to lost arbitration or CAN bus error, the higher priority (non-TX FIFO) message will be transmitted. The aborted message is put back in the output pipeline. However, instead of being put behind the non-TX FIFO message, it is placed after the previous second message in the TX FIFO.

The output pipeline will then appear as follows:

Position 1: non TX FIFO message with higher CAN priority (transmission ongoing)

Position 2: TX FIFO message 2

Position 3: TX FIFO message 1

At this point, TX FIFO message 2 is in the output pipeline in prior to TX FIFO message 1 and they are transmitted in that order, resulting in a message sequence inversion.

The scope of erratum describes the case when the M\_CAN uses both dedicated TX Buffers and a TX FIFO (TXBC.TQFM = '0') and the messages in the TX FIFO do not have the highest internal CAN priority. The above described sequence inversion may also occur between two non TX FIFO messages (TX Queue or dedicated TX Buffers) that have the same CAN identifier and that should be transmitted in the order of their buffer numbers (not the intended use).

### Workaround

When transmitting messages from a dedicated TX Buffer with higher priority than the messages in the TX FIFO, choose one of the following workarounds:

#### First Workaround

Use two dedicated TX Buffers, for example, use TX Buffers 4 and 5 instead of the TX FIFO. The pseudo-code below replaces the function that fills the TX FIFO.

Write message to TX Buffer 4

Transmit Loop:

- Request TX Buffer 4 by setting TXBAR.AR[27] bit to 1
- Write message to TX Buffer 5
- Wait until transmission of TX Buffer 4 completed by reading IR.TC and TXBTO.TO[27]
- Request TX Buffer 5 by setting TXBAR.AR[26] bit to 1
- Write message to TX Buffer 4
- Wait until transmission of TX Buffer 5 completed by reading IR.TC and TXBTO.TO[26]

#### Second Workaround

Assure that only one TX FIFO element is pending for transmission at any time. The TX FIFO elements may be filled at any time with messages to be transmitted, but their transmission requests are handled separately. Each time a TX FIFO transmission has completed and the TX FIFO gets empty (IR.TFE = '1') the next TX FIFO element is requested.

#### Third Workaround

Use only a TX FIFO. Send the message with the higher priority also from TX FIFO. However, this workaround has a drawback: the higher priority message has to wait until the preceding messages in the TX FIFO have been sent.

## ERR007236: XBIC: XBIC may trigger false FCCU alarm

### Description

The Crossbar Integrity Checker (XBIC) will incorrectly signal a fault alarm when a system bus request results in a bus error termination from a crossbar client. The Fault Correction and Collection Unit (FCCU) alarm number corresponding to the XBIC will be signaled.

### Workaround

Software should handle faults on FCCU alarm corresponding to the XBIC in case of a system bus error.

## ERR006553: PSI5: T bit error Ambiguity is noticed in Synchronous mode

### Description

When the Peripheral Sensor Interface (PSI5) module is configured in synchronous mode and two frames are consecutive, the T bit error flag, in the PSI5 Message Receive Register High (PSI5\_PMRRH), may incorrectly be set in the PSI5 Message Receive Register High (PSI5\_PMRRH) of the second frame. This happens when the duration of the gap between the frames is less than the duration of one idle T bit.

### Workaround

Ensure a delay of one idle T bit period between two consecutive data frames in synchronous mode.

One Idle T bit duration is 32 cycles of the PSI5 sampling clock.

## ERR008004: FLASH: Array Integrity with Breakpoints enabled may skip addresses for certain RWSC and APC combinations

### Description

For certain combinations of the Flash Read Wait State Control (RWSC) and Address Pipeline Control (APC) settings in the Platform Flash Configuration Register (PFLASH\_PCFR1) the Flash's array integrity (AI) check when run with breakpoints enabled may skip addresses resulting in an incorrect Multiple Input Signature Register (MISR) value or in the case of back to back ECC event errors (EER) or Single Bit Correction (SBC) events, a skipped breakpoint. This occurs for the following combinations:

RWSC=1 and APC=1

RWSC=3 and APC=2

RWSC=5 and APC=3

If breakpoints are enabled and an EER or SBC cause a breakpoint to occur the address after the breakpoint will be skipped, and the resulting MISR will not match expectations. Likewise, if there are back to back errors (EER or SBC) during AI with the above RWSC/APC combinations the 2nd error (and breakpoint) will be missed.

Margin Read (which by specification is a self timed event and is independent of wait states selected) is not affected by this erratum. This erratum only applies to Array Integrity.

### Workaround

One workaround is to follow the recommended RWSC and APC combinations for given frequencies. If this is done, Array Integrity with Breakpoints feature works as expected. Valid RWSC/APC combinations listed in the specification are:

Table:

Flash Operating Frequency	RWSC	APC
<i>Table continues on the next page...</i>		

30 MHz	0	0
100 MHz	2	1
133 MHz	3	1
167 MHz	4	1
200 MHz	5	2

A second workaround is if the above RWSC and APC combinations (listed in the description) are desired to be checked, do so without enabling breakpoints. In this case, the first EER or SBC event will be logged, and the MISR will correctly reflect the result of all reads being executed.

## ERR008368: REACM2: ETPU\_C clock does not halt if REACM2 Module Disable (MDIS) is set to 1

### Description

In this device, the Enhanced Time Processor Unit C (ETPU\_C) and Reaction Module (REACM2) share the same clock domain. A clock halt request performed by setting System Integration Unit Halt 1 ETPU\_C bit (SIU\_HLT1[ETPUC]) requires an acknowledge response from both modules to correctly complete. If REACM2 Module Configuration Register Module Disable bit (REACM2\_MCR[MDIS]) is set to 1, REACM2 will not return the required acknowledge signal. As such, the ETPU\_C clock will not halt.

### Workaround

Before submitting a halt request to ETPU\_C, ensure that REACM2 is in its active mode (REACM2\_MCR[MDIS]=0).

## ERR009670: FCCU: Limitation of error output signal observation test function

### Description

The Fault Collection and Control Unit (FCCU) I/O Control Register (FCCU\_EINOUT) provides an option to observe the EOUT[1:0] signals (ERROR1 and ERROR0 pins) in input mode in either the Test0 or Test2 fault output modes.

The ERROR[1:0] signals on this device are available on multi-function pins whose function is meant to be selectable either by Device Configuration Format (DCF) record or by System Integration Unit (SIU) registers. However, due to this issue, the observation of error signals provided by FCCU\_EINOUT only functions properly when the pins have been configured by DCF record and does not function correctly if the pin function has been selected via the SIU Pad Configuration Register (PCR) instead.

### Workaround

In order to use the FCCU\_EINOUT features to properly observe the error signals in input mode, the Error Functions Pads Configuration DCF record must be programmed in the user DCF records section of user test (UTEST) flash. Do not use Pad Configuration Registers SIU\_PCR117 or SIU\_PCR125 to select the error pin functions.

## ERR008711: SDADC: Digital filter and FIFO not disabled when MCR[EN] is cleared

### Description

When the Enable bit (EN) of the Sigma-Delta Analog to Digital Converter (SDADC) Module Configuration Register (MCR) is cleared (MCR[EN]=0), the digital part of the SDADC continues operating and does not go to low power mode if the module is disabled while a valid conversion is already in process and the application software continues to initiate conversions. As a consequence, the digital block of the SDADC still produces new conversion results in the Channel Data Register (CDR) and dummy data are transferred to the result First-In, First-Out (FIFO) buffers. In addition, interrupt and/or Direct Memory Access (DMA) events are still generated.

Note: the analog part does enter the power-down mode, reducing the consumption on the ADC high voltage supply domain (VDDA\_SD).

#### Workaround

Do not initiate a conversion prior to enabling the SDADC (MCR[EN]=1). In addition, once the SDADC has been enabled (MCR[EN]=1), if the SDADC needs to be disabled (MCR[EN]=0), prior to clearing the EN bit, either turn off the clock to the SDADC module in the System Integration Unit (SIU) or Select the External Modulator Mode (EMSEL) by setting the MCR[EMSEL] bit along with the clearing the MCR[EN].

### ERR005887: PSI5: Detection of a received bit causes an electrical error in specific conditions

#### Description

During the Peripheral Sensor Interface 5 (PSI5) bit extraction from the Manchester encoded receive data, if the transition of the data occurs in the first two clock periods of the detection window then the transition is not recognized and the electrical error bit (PSI5\_PMRRH[E]) will be set in the PSI5 Message Receive Register High.

#### Workaround

PSI5 sensors are specified to have a 45%/55% duty cycle output worst case. If the external PSI5 bus line circuit is not balanced then this can potentially alter the duty cycle of the sensor data received by the PSI5 module. The user must ensure that the sensor bus circuit is designed such that the Manchester Coded signal received by the PSI5 module has a worst case 30%/70% duty cycle

### ERR050782: e200: Time Base TBU register contains wrong value during TBL rollover

#### Description

The e200 Time Base (TB) facility is a 64-bit structure provided for maintaining the time of day and operating interval timers. The TB consists of two 32-bit registers - time base upper (TBU) and time base lower (TBL). TBU and TBL are concatenated to provide a long-period 64-bit counter. TBL increments until its value becomes 0xFFFF\_FFFF. The intended behavior is that at the next increment when the TBL value becomes 0x0000\_0000 that the TBU value is incremented. But the actual behavior is that after the TBL value becomes 0x0000\_0000, the TBU value will not increment until the transition of the TBL value to 0x0000\_0001.

#### Workaround

Software will need to take care about the wrong TBU value during TBL rollover. Use the following sequence for reading TBU and TBL values:

loop:

```
mfscr r12, TBL
mfscr r3, TBU
mfscr r4, TBL
cmpl r4,r12
se_blt loop
```

### ERR005073: PSI5: Possible message reception errors due to incorrect data latency reference point

#### Description

The Peripheral Sensor Interface (PSI5) module incorrectly defines the end of the message to coincide with the detection of idle, which occurs one T-Bit (bit time in counts of the sample clock) duration after the midpoint transition of the CRC0 (Cyclic

Redundancy Check) or Parity bit of the frame. However the PSI5 specification defines the end of the frame as the midpoint transition of the CRC/Parity bit. This difference means that a correctly timed PSI5 frame could be interpreted as arriving before the previous frame had completed.

### Workaround

The error can cause at least one of the following status bits to be set:

PSI5 Message receive register low "C-bit" (PSI5\_PMRRL[C]) - Indicates CRC recalculation error in message

PSI5 Message receive register high "E-bit" (PSI5\_PMRRH[E]) -Indicates Electrical error

PSI5 Message receive register high "T-bit" (PSI5\_PMRRH[T]) -Indicates Timing error

Software can monitor these bits, and if these errors are present on several concurrent messages then the software can re-initialize the system

## ERR050090: DSPI/SPI: Incorrect data may be transmitted in slave mode

### Description

If the Serial Peripheral Interface (SPI or the Deserial/Serial Peripheral Interface) is operating in slave mode, incorrect or stale data may be transmitted in next transaction without underflow interrupt generation if the set up time of the Peripheral Chip Select (PCS) to the SPI Serial Clock (SCLK) is short and the transmit FIFO may become empty after one transaction.

This can occur if the PCS to SCK is less than:

$$4 \times \text{IPG\_CLOCK\_PERIOD} + 4 \times \text{DSPI\_CLOCK\_PERIOD} + 0.5 \times \text{SCK\_CLOCK\_PERIOD}$$

Where:

IPG\_CLOCK is the internal bus clock ("system" clock)

DSPI\_CLOCK is the protocol clock.

SCK\_CLOCK is the Line-Side Serial Communication Clock.

### Workaround

When operating in slave mode, software must ensure that the time interval between PCS assertion to start of SCK Clock is greater than  $4 \times \text{IPG\_CLOCK\_PERIOD} + 4 \times \text{DSPI\_CLOCK\_PERIOD} + 0.5 \times \text{SCK\_CLOCK\_PERIOD}$ .

To meet this requirement, the Master SPI can either lengthen the PCS to SCK assertion time or decrease the frequency of the communication interface, or both.

## ERR051044: M\_CAN: Transmission order of the Tx Queue buffers with the same Message ID is impacted by the PUT index functionality

### Description

When multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission (lowest buffer number is transmitted first). An Add request points the PUT Index always to that free buffer of the Tx Queue with the lowest buffer number, and thus the buffer transmission order is not predictable.

### Workaround

In case a defined order of transmission is required for message with some ID:

1) Use the TXBAR features:

a. Write the group of Tx message buffers with same Message ID to the Message RAM



- b. Request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID ensure that no message with this Message ID has a pending Tx request.
- 2) Tx buffers shall be requested in ascending order with lowest buffer number first.
- 3) A single Tx Buffer can be used to transmit those messages one after the other.
- 4) The Tx FIFO shall be used for transmission of messages with the same Message ID.

## **ERR007429: FCCU: Writes to Flash assert FCCU\_NCF #17 (FLASH\_INIT)**

### **Description**

When programming Flash, Fault Control and Collection Unit event #17, "Flash Initiation Error" may be incorrectly asserted when no actual error has occurred.

### **Workaround**

By default there is no reaction to this event. The user must not program a reaction for this fault channel when flash programming is required. It is intended only for debug purposes.

## **ERR011235: EMIOS: Any Unified Channel running in OPWMB or OPWMCB mode may function improperly if the source counter bus is generated by Unified channel in MC mode**

### **Description**

The Unified channel (UC) configured in Center Aligned Output Pulse Width Modulation Buffered (OPWMCB) or Output Pulse Width Modulation Buffered (OPWMB) modes is not working properly when it is sourced from the UC configured in Modulus Counter (MC) mode by setting the channel control register MODE bitfield to 0x10 or 0x11 and any of its pre-scalers (internal or global) divider ratio is higher than 1.

### **Workaround**

When a counter bus is generated by the UC set in the MC mode with any pre-scaler (internal or global) divider ration higher than 1, don't use this counter bus for the UC set in OPWMCB or OPWMB mode.

## **ERR010808: STCU: Chip may get stuck-in-reset if PLL Loss-of-Lock occurs during STCU Offline Self-Test**

### **Description**

If Phase-Locked Loop (PLL) Loss-of-Lock occurs during Self-Test Control Unit (STCU) offline self-test, the device may get stuck in reset (RSTOUT pin stays low), requiring power to be cycled down and then back up to recover the device (power-on reset).

This applies to both the Memory Built-In Self-Test (MBIST) sequence and the Logic Built-In Self-Test (LBIST) sequence or any combination of the two.

Recommended self-test sequences are documented in Application Note AN5288, "MPC5777C STCU Quick Start Guide" available at <http://www.nxp.com>. Failure rates due to this erratum for these recommended sequences can be expressed as follows:

The failure rate for the full LBIST/MBIST offline sequence (50MHz PLL) is < 0.02 times the failure rate of the PLL reference clock (e.g. crystal oscillator failure rate, if a crystal reference is used).

The failure rate for MBIST-only offline sequence (200MHz PLL) is < 0.0002 times the failure rate of the PLL reference clock.

### Workaround

If the expected failure rate cannot be tolerated, program the Device Configuration Format (DCF) record for the STCU\_RUN client such that offline self test is bypassed (RUN=0 and BYP=1).

Online self-test is not affected by this issue and can be used in place of offline test.

## ERR011028: PMC: Self Test result flag clears on any write to the ST\_RESULT field

### Description

When running a Power Management Controller (PMC) Self Test, any write to the self test result flag of the Voltage Detect User Mode Register (PMC\_SELF\_TEST\_UM\_VD\_REG[ST\_RESULT]) clears the flag, not just when writing a 1.

### Workaround

Do not write any value to the PMC\_SELF\_TEST\_UM\_VD\_REG register while a test is running (ST\_DONE=0) in order to avoid unintentionally clearing the result flag.

## ERR008730: XBIC: XBIC may store incorrect fault information when a fault occurs

### Description

The Crossbar Integrity Checker (XBIC) may incorrectly identify a fault's diagnostic information in the case when the slave response signals encounter an unexpected fault when crossing the crossbar switch (XBAR) during the data phase. While the fault event is detected, the diagnostic status information stored in the XBIC's Error Status Register (XBIC\_ESR) and Error Address Register (XBIC\_EAR) does not reflect the proper master and slave involved in the fault. Instead, the preceding master or slave ID may be recorded.

### Workaround

Expect that when a fault is reported in the XBIC\_EAR and XBIC\_ESR registers the actual fault information may be from the preceding transition.

## ERR009361: eSCI: Timing of TXRDY interrupt flag assertion is incorrect for LIN TX Frame

### Description

When generating a Local Interconnect Network (LIN) Transmit (TX) Frame, the Transmit Data Ready Interrupt flag (eSCI\_IFSR2[TXRDY]) should assert after the transmission of the Identifier (ID) field. In the TX frame generation, however, the eSCI\_IFSR2[TXRDY] asserts after the Sync field. All subsequent TXRDY Interrupt flags in the current frame assert after each subsequent byte field has been transmitted except for the final TXRDY Interrupt flag. The last TXRDY Interrupt flag asserts after the transmission of the checksum field.

### Workaround

The timing of the TXRDY Interrupt flag cannot be changed from the incorrect behavior. The incorrect TXRDY Interrupt flag behavior does not affect LIN functionality. Even though the TXRDY Interrupt flag asserts earlier than expected, the TXRDY Interrupt flag still signals that the content of the LIN Transmit Register (eSCI\_LTR) was processed by the LIN Protocol Engine.

## ERR009527: FlexCAN: The transmission abort mechanism may not work properly

### Description

The Flexible Controller Area Network (FlexCAN) is not able to abort a transmission frame and the abort process may remain pending in the following cases:

- a) If a pending abort request occurs while the FlexCAN is receiving a remote frame.
- b) When a frame is aborted during an overload frame after a frame reception.
- c) When an abort is requested while the FlexCAN has just started a transmission.
- d) When Freeze Mode request occurs and the FlexCAN has just started a transmission.

#### Workaround

Use the Mailbox Inactivation mechanism instead of the transmission abort mechanism. The Abort Enable bit (AEN) of the Module Configuration Register should be kept cleared and the abort code value "0b1001" should not be written into the CODE field of the Message Buffer Control and Status word.

### ERR008310: XBIC: Crossbar Integrity Checker may miss recording information from an initial fault event in the case of back-to-back faults

#### Description

When the Crossbar Integrity Checker (XBIC) detects back-to-back faults on a system bus path through the crossbar switch (AXBS), the fault information captured in the XBIC Error Status Register (XBIC\_ESR) and the XBIC Error Address Register (XBIC\_EAR) does not correspond to the initial fault event, but rather the subsequent fault event. While the fault event is properly detected, diagnostic status information in the XBIC\_ESR and XBIC\_EAR registers describing the initial fault event is lost. This defect can only occur in the event of a series of bus transactions targeting the same crossbar slave target, where the series of bus transactions are not separated by idle or stall cycles.

#### Workaround

Expect that the XBIC\_EAR and XBIC\_ESR registers may not contain the initial fault information, but will contain the latest fault information.

### ERR009783: DSPI: Frame transfer does not restart after DSI frame matches preprogrammed value

#### Description

In the Deserial Serial Peripheral Interface module, in the scenario when:

1. Master/slave mode select bit of module configuration register is set (MCR[MSTR]=0b1) to configure the module in master mode
2. Deserial Serial Interface (DSI) communication is selected via DSPI Configuration field (DCONF) in the Module Configuration Register (MCR [DCONF] = 0b01)
3. Preprogrammed value for data match with received DSI frame is configured using DSI De-serialized Data Polarity Interrupt Register (DPIR) and DSI De-serialized Data Interrupt Mask Register (DIMR)
4. Data Match Stop (DMS) bit of DSI configuration register0 is set (DSICR0 [DMS] =0b1) which stops DSI frame transfer in case of a data match with a preprogrammed value
5. DSI frame is received with bits matching preprogrammed value.

Under these conditions, the next frame transfer is stopped, DSI Data Received with Active Bits bit of status register is set (SR [DDIF] =0b1) and the corresponding DDIF interrupt is asserted. Even after the interrupt is serviced and SR [DDIF] is reset, the frame transfer does not restart.

#### Workaround

DSI frame transfer stop in case of DSI data match condition should be disabled. For this, keep the data match stop bit of DSI configuration register 0 de-asserted (DSICR0 [DMS]=0b0).

## ERR010135: PMC: Resets that occur during the PMC Self Test process can cause corrupted results.

### Description

Some system resets, if they occur while the Power Management Controller (PMC) self test is running, can result in the PMC self test logic being left in a corrupted state. The affected reset sources are: System software reset, Fault Collection and Control Unit (FCCU) reset fault reactions, and debug (JTAG) reset.

### Workaround

After a reset caused by one of the affected reset sources, check the status of the self test by reading the PMC Voltage Detect User Mode Test Register (PMC\_SELF\_TEST\_UM\_VD\_REG). If a PMC self test failure is indicated, run the PMC self test again to confirm the failure.

## ERR008252: eTPU: ETPU Angle Counter (EAC) Tooth Program Register (TPR) register write may fail

### Description

When the TPR is written with the Insert Physical Tooth (IPH) bit set to 1, and a physical tooth arrives at near the same time, the buffering of a second write to the TPR may fail, even if the required wait for one microcycle after the IPH write is observed.

### Workaround

Wait at least two microcycles between consecutive writes to the TPR register, if the first write sets the IPH bit.

## ERR007724: FlexCAN: Documentation of ECC registers

### Description

FlexCAN ECC registers listed below have issues in their descriptions.

#### 1) Error Injection Address Register (CAN\_ERRIAR):

FlexCAN registers and data structures located in RAM are 32-bit (4 bytes) wide, therefore, the two least significant bits in INJADDR bit field are don't care. Read attempts to this register will result in address values multiple of 0x4.

#### 2) Error Report Data Register (CAN\_RERRDR):

RDATA bit field is read-only.

#### 3) Error Report Syndrome Register (CAN\_RERRSYNR):

BE3, BE2, BE1, BE0, SYND3, SYND2, SYND1 and SYND0 bit fields are read-only.

### Workaround

No workaround needed.

## ERR010645: SIU: WKPCFG is not applied until after initial reset negation

### Description

After power-up of the device, Weak-pull Configuration (WKPCFG) is not applied until after the negation of the initial reset input (RESET pin).

If Self-Test Control Unit (STCU) offline self-test is disabled, then WKPCFG is applied once, just before Reset Output (RSTOUT) is negated.

If STCU offline self-test is enabled, then WKPCFG is applied twice: first just before STCU self-test begins, and second just before RSTOUT is negated (re-applying WKPCFG value from DCF or pin each time),

Therefore, the pad state during reset for initial reset assertion for pins that use WKPCFG is determined by the default value of the System Integration Unit Pad Configuration Register Weak Pull State bit (SIU\_PCR[WPS]) for each pin, not by WKPCFG.

The pad state during reset for subsequent resets is based on the previously applied WKPCFG value (from prior RSTOUT negation). Then at subsequent reset negation, the present value of WKPCFG is applied.

The SIU\_PCR[WPS] reset value for all pins that use WKPCFG is 0. These pins are PCR numbers: 114-145, 147-204, 432-437, 441-472, and 475-491.

#### Workaround

System must not rely on internal weak pull up or down for WKPCFG-controlled pins during reset assertion. External circuits monitoring such pins should mask out the value while reset is asserted, or add external pull resistors if needed.

### ERR010580: MPC577xC: Flash HVD may assert during slow input supply ramp

#### Description

During power up, under slow input ramp rates (10ms or slower to reach operating voltage level), a High-Voltage Detection (HVD) event may be observed. This HVD event is generated by the detector monitoring the flash regulator output (HVD\_FLASH).

This may have the effect of prolonging the reset duration until the supply voltage reaches operational levels but does not lead to any incorrect operation of the device.

#### Workaround

Use a ramp rate faster than 10ms to reach operational voltage levels. If a slower ramp rate is used, check and clear Flash HVD status after each power up so that subsequent voltage detection events can be properly indicated.

### ERR007099: FCCU: Error pin signal length is not extended when the next enabled fault, with its alarm timeout disabled, occurs

#### Description

In the Fault Collection and Control Unit (FCCU), when the following conditions are met:

- two faults occur
- the second fault arises with a delay ( $T_{\text{delay}}$ ) from the first error
- the second fault has its alarm timeout disabled
- $T_{\text{delay}}$  is lower than the FCCU error pin minimum active time ( $T_{\text{min}}$ , defined in the Delta T register (FCCU\_DELTA\_T))

Then the error output signal is not extended and its duration is only  $T_{\text{min}}$ , if the faults are cleared before the timer expires.

The expected behavior is to have the error output signal duration of  $T_{\text{min}} + T_{\text{delay}}$ , if the faults are cleared before the timer expires.

#### Workaround

Take into account that the error out signal duration will only be  $T_{\text{min}}$ , if the faults are cleared before the timer expires.

The timer count is meaningful only when the Error pin is driven low, which can be checked by reading the pin status FCCU\_STAT[ESTAT].

## ERR010963: Flash: Memory accesses may be corrupted when flash is operating between 33MHz and 75MHz

### Description

Error Correction Code (ECC) errors may be generated in the flash due to corrupted data when all of the following conditions are met:

- The flash operating frequency is greater than 33MHz and less than or equal to 75MHz
- Read Wait State Control (PFLASH\_PFCR1[RWSC]) = 2 and Address Pipeline Control (PFLASH\_PFCR1[APC]) = 1
- Pipelined reads which are executed between the UTEST flash block and any other flash block. Pipelined reads are overlapping reads, where before the previous read is completed a new read is requested.

Device has UTEST memory space and remaining flash area is the main array memory space. This issue condition occurs if pipelined reads are executed between UTEST and the main array space. If pipelined reads are executed between UTEST and UTEST memory space or between main array and main array memory space, this issue condition will not be seen.

### Workaround

When the flash clock frequency is greater than 33MHz and less than or equal to 75MHz configure PFLASH\_PFCR1[RWSC] = 2 and PFLASH\_PFCR1[APC] = 0. The configuration for all other flash clock frequencies is specified in the MCU datasheet.

## ERR010586: M\_CAN: Configuration NBTP.NTSEG2 = '0' not allowed

### Description

In the Modular CAN (M\_CAN) module, when the following conditions are present:

- the Nominal Time segment after sample point (NTSEG2) field of the Nominal Bit Timing and Prescaler register (NBTP) value is 0 (NBTP.NTSEG2 = 0b0, i.e. the phase 2 duration is 1 time quantum (tq))
- there is a pending transmission request

Then the M\_CAN module may transmit the first identifier bit as dominant instead of recessive.

Additional information:

The ISO 11898-1 specifies the minimum configuration range for Phase 2 duration to be between 2 and 8 tq.

Only the NBTP register, used to configure the baudrate for the arbitration phase, is impacted. The Data Bit Timing and Prescaler Register (DBTP) is not impacted.

### Workaround

Use a configuration range for NBTP.NTSEG2 from 1 to 127.

## ERR011238: MPC577xC: When internal resets occur, there may be a delay before the external reset pin asserts

### Description

When an internal reset occurs, a number of clocks are needed before the external reset pin (RSTOUT) will assert. This delay can be significant (up to 2.5uS) if the reset is caused by the Fault Collection and Control Unit (FCCU).

### Workaround

Any external devices that depend on the microcontroller's external reset pin must be tolerant of the delay. Other output signals on the microcontroller will be returning to reset default levels and drive characteristics during this time and may do so before the RSTOUT pin asserts.

## ERR010737: MPC577xC: Nexus Program Trace Sync Message sometimes missing after queue overflow

### Description

When the core nexus trace functionality is enabled, the expected Program Trace Sync or Data Trace Sync Message following a FIFO overflow error message may not be reported, causing a larger window of uncorrelated trace information until the next sync message is transmitted.

### Workaround

Avoid queue overflow by using the core Nexus stall feature. If using the stall feature is not desirable, the following actions may help reduce the occurrence of the condition.

- Use Branch History Mode to reduce the frequency of messages.
- Use triggers to disable and re-enable trace in areas of code where continuity of trace is not essential.

## ERR009978: eMIOS: Unexpected channel flag assertion during GPIO to MCB mode transition

### Description

When changing an Enhanced Modular IO Subsystem (eMIOS) channel mode from General Purpose Input/Output (GPIO) to Modulus Counter Buffered (MCB) mode, the channel flag in the eMIOS Channel Status register (eMIOS\_Sn[FLAG]) may incorrectly be asserted. This will cause an unexpected interrupt or DMA request if enabled for that channel.

### Workaround

In order to change the channel mode from GPIO to MCB without causing an unexpected interrupt or DMA request, perform the following steps:

- (1) Clear the FLAG enable bit in the eMIOS Control register (eMIOS\_Cn[FEN] = 0).
- (2) Change the channel mode (eMIOS\_Cn[MODE]) to the desired MCB mode.
- (3) Clear the channel FLAG bit by writing '1' to the eMIOS Channel Status register FLAG field (eMIOS\_Sn[FLAG] = 1).
- (4) Set the FLAG enable bit (eMIOS\_Cn[FEN] = 1) to re-enable the channel interrupt or DMA request reaction.

## ERR009770: MPC5777C: Incorrect operation of open-drain outputs

### Description

When pins are configured as open-drain the high-drive for the output buffer is normally disabled. However, due to this Issue, during the transition to or from this non-driven state, the output may momentarily drive high. The duration of this drive is 0-10ns.

### Workaround

Strong external drivers connected to the pin need to ensure they do not attempt to drive the pin within 10ns of the MCU transitioning to or from the non-driven state. This will prevent contention between the internal and any external drive sources.

## ERR007116: CRC: AutoSAR 4.0 8-bit CRC8 0x2F is not supported in hardware

### Description

The Cyclic Redundancy Check (CRC) module does not implement the 8-bit CRC-8-H2F required to support the Autosar 4.0 specification. The CRC-8-H2F uses a polynomial generator seed of 0x2F and an equation of  $x^5 + x^3 + x^{2+x+1}$ .

## Workaround

Do not set the Polynomial selection to 0b11 in the CRC Configuration register (CRC\_CFG). The 8-bit CRC-8-H2F function must be written in software to support AuroSAR 4.0.

## ERR005642: ETPU2: Limitations of forced instructions executed via the debug interface

### Description

The following limitations apply to forced instructions executed through the Nexus debug interface on the Enhanced Time Processing Unit (ETPU):

- 1- When a branch or dispatch call instruction with the pipeline flush enabled (field FLS=0) is forced (through the debug port), the Return Address Register (RAR) is updated with the current program counter (PC) value, instead of PC value + 1.
- 2- The Channel Interrupt and Data Transfer Requests (CIRC) instruction field is not operational.

### Workaround

Workaround for limitation #1 (branch or dispatch call instruction):

Increment the PC value stored in the RAR by executing a forced Arithmetic Logic Unit (ALU) instruction after the execution of the branch or dispatch call instruction.

Workaround for limitation #2 (CIRC):

To force an interrupt or DMA request from the debugger:

- 1- Program a Shared Code Memory (SCM) location with an instruction that issues the interrupt and/or DMA request. Note: Save the original value at the SCM location.
- 2- Save the address of the next instruction to be executed.
- 3- Force a jump with flush to the instruction position.
- 4- Single-step the execution.
- 5- Restore the saved value to the SCM location (saved in step 1).
- 6- Force a jump with flush to the address of the next instruction to be executed (saved in step 2).

NOTE: This workaround cannot be executed when the eTPU is in HALT\_IDLE state.

## ERR008369: PAD\_RING: Reset output (RSTOUT) pin is not driven during Power-On Reset (POR) or Low-Voltage Detect (LVD) assertion

### Description

RSTOUT, as an output pin, is expected to always be driven either high or low. However, in low-voltage conditions during POR and/or LVD reset (core VDD or Input/Output VDDEX supply domains), the RSTOUT pin will be in a high-impedance (hi-z) state until voltages reach the operational ranges specified in the datasheet.

Once out of POR/LVD state, RSTOUT pin is driven low until the device completes start-up and leaves reset condition..

### Workaround

Add an external pull-down resistor if the application requires RSTOUT to always be driven low during any reset condition.



## ERR009784: MPC577xC: Reset escalation count is reduced by 1 when configured via UTEST DCF record

### Description

The Reset Escalation Threshold (RET) value is stored in the System Integration Unit Reset Control Register (SIU\_RCR). This value may be initialized either by writing to this register in normal operation or by Device Configuration Format (DCF) record stored in UTEST flash.

However, there is a difference in the effective reset escalation threshold depending on whether the SIU\_RCR[RET] field is loaded via DCF record or written directly by code executing on the device. Writing SIU\_RCR[RET] directly will cause the reset escalation counter to expire in the expected (RET+1) counts as stated in the Reference Manual.

If instead the SIU\_RCR[RET] value is loaded via the UTEST Reset Escalation Configuration DCF record, then the escalation counter expires after a number of resets equal the the RET value rather than the value of RET+1.

### Workaround

When configuring the SIU\_RCR[RET] count via the UTEST Reset Escalation Configuration DCF client, be aware that the number of resets before expiration will be equal to RET rather than RET+1. Set the value of RET in the DCF record according to the number of reset cycles desired before reset escalation action is to be taken.

## ERR007226: FCCU: the error-out signalling cannot be disabled in non Bi-stable protocols

### Description

In the Fault Collection and Control Unit (FCCU) module, the error out signalling can only be disabled when using the Bi-stable protocol and not all of the protocols.

The Error Out (EOUT) Signaling Enable Register (FCCU\_EOUT\_SIG\_ENx) registers, which can be used for disabling error out signalling, are applicable only for bi-stable mode and do not affect the other protocols. (Various protocols like Bi-stable, Dual rail and other protocols are selected by programming the Fault Output Mode (FOM) field of the Configuration Register (FCCU\_CFG)).

### Workaround

Do not expect and program the EOUT\_SIGN\_ENx register to support anything other than bi-stable protocol.

The EOUT Signaling Enable (EOUTENx) field description of FCCU\_EOUT\_SIG\_EN should be read as follows:

0 = EOUT signaling is disabled for error Recoverable Fault (RF) source x for bi-stable protocol. Error pins behave as if in Non-Faulty state.

1 = EOUT signaling is enabled for error RF source x for bi-stable protocol.

## ERR010853: MPC577xC: Oscillator clock may be disturbed by input/output pin ETPUB31

### Description

When pin ETPUB31 (GPIO178) is used as an input or output for any function, it may disturb the crystal oscillator circuit and cause a loss of clock if the Automatic Level Control (ALC) mode is enabled on the oscillator.

### Workaround

If a loss of clock is observed which is coincident with an ETPUB31 pin transition, then disable ALC by setting the XOSC\_ALC\_DIS bit to '1' in the UTEST Miscellaneous Device Configuration Format (DCF) record. Disabling the ALC feature will change the characteristics of the oscillator circuit and require re-characterization of the clock circuit on the application board.

Note that the disturbance of the oscillator may only occur when the ETPUB31 pin transitions from high to low or from low to high. If the pin is used at a constant level, no change is required.

## ERR010109: MPC5777C: Enabling pending read optimization (off by default) can cause incorrect operation on the system crossbar

### Description

The default setting for pending read optimization is disabled. If pending read optimization is enabled, this can cause the masters on the system crossbar (XBAR) to stall, receive wrong read data, or perform a spurious read access when uncorrectable Error Correcting Code (ECC) errors are reported by a XBAR slave. For a read transaction following an uncorrectable ECC error, these masters can stall or receive the wrong data.

### Workaround

Do NOT enable pending read optimization (leave `PCM_IAHB_BEn[PRE*] = 0`, the default value) for all XBAR masters.

Core0: Clear bits `PRE_CORE0_I` and `PRE_CORE0_D` in register `PCM_IAHB_BE1`.

Core1: Clear bits `PRE_CORE1_I` and `PRE_CORE1_D` in register `PCM_IAHB_BE1`.

eDMA\_A: Clear bit `PRE_DMA_A` in register `PCM_IAHB_BE2`.

eDMA\_B: Clear bit `PRE_DMA_B` in register `PCM_IAHB_BE2`.

CSE2/SIPI: Clear bit `PRE_M6` in register `PCM_IAHB_BE2`.

FEC: Clear bit `PRE_FEC` in register `PCM_IAHB_BE2`.

Performance note: Pending read optimization has an effect on performance of back-to-back reads issued by the given master. A general statement about performance impact of disabling this optimization cannot be made as it depends on data traffic patterns for all involved masters in the system. However, the following steps can be taken to reduce or eliminate any impact of disabling the pending read optimization for these masters:

For Core0 and Core1, enable instruction cache and data cache.

For Enhanced Direct Memory Access masters (eDMA\_A and eDMA\_B), program Transfer Control Descriptors (TCDs) where source size (ssize) and destination size (dsize) parameters are set to the same value. There is no performance impact in this case as the DMA does not perform back to back reads.

Cryptographic Services Engine (CSE2), Serial Interprocessor Interface (SIPI), and Fast Ethernet (FEC) masters typically do not benefit from pending read optimization and are therefore usually unaffected by disabling the feature.

## ERR009656: DSPI: Frame transfer does not restart in case of SPI parity error in master mode

### Description

In the Deserial Serial Peripheral Interface (DSPI) module, in the scenario when:

1. Master/slave mode select bit (MSTR) of Module Configuration register (MCR) is set (`MCR[MSTR]=0b1`) to configure the module in master mode
2. SPI communication is selected via DSPI Configuration field (DCONF) in MCR (`MCR[DCONF] = 0b00`)
3. Parity reception check on received frame is enabled by setting the Parity Enable or Mask tASC delay (`PE_MASC`) bit of DSPI PUSH FIFO Register In Master Mode (PUSHR), i.e. `PUSHR[PE]=0b1`.
4. Parity Error Stop bit (PES) of MCR is set (`MCR[PES]=0b1`) which stops SPI frame transfer in case of parity error
5. Parity error is detected on received frame.

Then the next frame transfer is stopped, the SPI Parity Error Flag bit (SPEF) of the DSPI Status Register (DSPI\_SR) is set (`SR[SPEF]=0b1`) and the corresponding SPI parity error interrupt is asserted. Even after the interrupt is serviced and `SR[SPEF]` is reset, the frame transfer does not restart.

### Workaround

Do not use SPI frame transfer stop in case of parity error detection for SPI transmission in master mode. For this, keep the Parity Error Stop bit of Module Configuration Register de-asserted (MCR[PES] = 0b0).

## ERR010797: EBI: Address 31 signal is not available in non-multiplexed mode

### Description

The reference manual specifies that the address 31 signal of the External Bus Interface (EBI) should be available on pin D\_CS2 in non-multiplexed mode. Instead, Data 31 is available on this pin.

Address 31 is needed for the Address by Port Size feature (EBI\_OR[APS]=1) or for non-chip-select accesses that require byte addressing.

### Workaround

Do not use the Address by Port Size feature (EBI\_OR[APS]=1) in non-multiplexed mode. Use APS=0 with non-multiplexed, or use APS=0/1 in multiplexed mode.

Do not perform non-chip-select accesses in non-multiplexed mode to external devices that require byte addressing.

## ERR010755: DSPI: Transmit and Receive FIFO fill flags in status register is not cleared when DMA is improperly configured

### Description

The Deserial/Serial Peripheral Interface Transmit and Receive First In/First Out (FIFO) buffers can request additional information to be transferred via the Direct Memory Access (DMA) module when either the Transmit or Receive FIFO Fill/Drain Flags are set in the DSPI Status Register (SR[TFFF/RDF]). However, the Transmit Fill Flag indicates that at least 1 location each (2 bytes each) in the Transmit and Command FIFOs is available to be written. It does not indicate that the FIFO is empty. Similarly, Receive FIFO fill flag only indicates at least 1 location (2 bytes) of the FIFO is available to be read. It does not indicate that the FIFO is full. If the DMA is configured to transfer more than 1 FIFO location size of data, the FIFO Fill/Drain Flags may not be properly cleared indicating that the FIFO is not full even when the FIFO is actually full (for Transmit FIFO) and not empty when the FIFO is actually empty (for Receive FIFO).

### Workaround

Properly configure the DMA to fill/drain only 2 bytes to Transmit, Command and Receive FIFOs. Use the DMA loop to transfer more data if needed.

## ERR007234: PSI5: No transfer error generated for accesses within the unused range of the PSI5 peripheral window

### Description

The Peripheral Sensor Interface (PSI5) uses 4 Kbytes of the 16 Kbytes range of the peripheral bridge slot assigned to it.

Accesses after the 4 Kbytes (from offset 0x1000 to offset 0xFFFF) will not generate a transfer error.

Note: accesses to unimplemented locations within the 4 Kbyte window will correctly generate a transfer error.

### Workaround

Take into account that no transfer error will be generated outside the 4 Kbyte region used by the PSI5 module.

In case such accesses must be detected, use the memory protection unit (MPU) to limit accesses.

## ERR009809: eTPU: MDU flags(Overflow/Carry) may be set incorrectly

### Description

The MAC Carry (MC) & MAC Overflow (MV) flags can be incorrectly set on a MAC instruction if it is the first MDU operation in a thread and the last MDU operation in previous thread was aborted/terminated (thread ended before the operation finished).

### Workaround

There are 2 workarounds:

(1) Do not abort/terminate a MDU operation

or

(2) Do not use a MAC instruction as the first MDU operation in a thread

## ERR007356: SDADC: The SDADC FIFO does not function correctly when FIFO overwrite option is used

### Description

In the Sigma-Delta Analog-to-Digital Converter (SDADC), when the FIFO Over Write Enable bit (FOWEN) of the FIFO Control Register (FCR) is set (FCR[FOWEN]=1), the following flags of the Status Flag Register (SFR) may not reflect the correct status:

- Data FIFO Full Flag (DFFF)
- Data FIFO Empty Flag (DFEF)

When the number of entries received by the FIFO reaches 2x the FIFO size (field FSIZE of FIFO Control Register (FCR)):

- SFR[DFFF] is cleared, incorrectly indicating the FIFO is not full
- SFR[DFEF] is set, incorrectly indicating the FIFO is empty

The expected behavior is that:

- SFR[DFFF] remains set until data is read out of the FIFO
- SFR[DFEF] remains clear until all data is read out of the FIFO

### Workaround

Do not use the FIFO Overwrite option to overwrite FIFO contents. Software shall clear the FIFO overrun condition (if necessary) and flush the FIFO contents before expecting valid data in the FIFO.

## ERR008367: REACM: Register is unexpectedly written after exiting halted state

### Description

If the Reaction Module (REACM) is set to low-power mode by asserting the associated Enhanced Time Processor Unit C (ETPU\_C) halt bit in the System Integration Unit Halt 1 register (SIU\_HLT1) and then writes are performed to REACM registers during the halted state, the first such write access will actually take effect when the REACM module later exits the halted state. Read and write accesses during the halted state will still generate the appropriate bus error indications.

### Workaround

Workaround 1: Detect improper accesses during the halted state by using the bus error exception and then either re-initialize REACM to a known-good state after exiting the halted state or restore its register contents from a backup area in RAM created prior to entering the halted state.

Workaround 2: Prevent access to the REACM during the halted state by using a Memory Protection Unit (MPU) region.

## ERR009658: SPI: Inconsistent loading of shift register data into the receive FIFO following an overflow event

### Description

In the Serial Peripheral Interface (SPI) module, when both the receive FIFO and shift register are full (Receive FIFO Overflow Flag bit in Status Register is set (SR [RFOF] = 0b1)) and then the Clear Rx FIFO bit in Module Configuration Register (MCR [CLR\_RXF]) is asserted to clear the receive FIFO, shift register data is sometimes loaded into the receive FIFO after the clear operation completes.

### Workaround

1. Avoid a receive FIFO overflow condition (SR[RFOF] should never be 0b1). To do this, monitor the RX FIFO Counter field of the Status Register (SR[RXCTR]) which indicates the number of entries in receive FIFO and clear before the counter equals the FIFO depth.
2. Alternatively, after every receive FIFO clear operation (MCR[CLR\_RXF] = 0b1) following a receive FIFO overflow (SR[RFOF] = 0b1) scenario, perform a single read from receive FIFO and discard the read data.

## ERR008631: SDADC: low threshold watchdog cannot be used with signed data

### Description

Each Sigma Delta Analog to Digital Converter (SDADC) provides a watchdog (WDG) to monitor the converted data range. This watchdog should trigger when a converted value is either higher than the value configured in the WDG Threshold Register Upper Threshold Value bit-field (SDADC\_WTHHLR[THRH]), or lower than the value configured in the Lower Threshold Value bitfield (SDADC\_WTHHLR[THRL]). Instead, the low WDG threshold acts as a high WDG threshold, triggering when a converted value is greater than the value configured in SDADC\_WTHHLR[THRL].

### Workaround

There are two workarounds available:

- 1) Do not use the WDG function by clearing the SDADC Module Control Register Watchdog Enable Bit (SDADC\_MCR[WDGEN]).
- 2) Configure the WDG low threshold SDADC\_WTHHLR[THRL] to the value 0x7FFF. This guarantees that a low threshold trigger will not be generated. The WDG high threshold (SDADC\_WTHHLR[THRH]) can be used without restriction.

## ERR008195: INTC: Interrupt Controller does not work correctly when in hardware vector interrupt mode and FMPERDIV is set to divide-by-4 or divide-by-

### Description

Hardware vector interrupt mode is selected for a e200z7 core by setting the corresponding Hardware Vector Enable bit in the Interrupt Controller (INTC) Module Configuration Register (INTC\_MCR[HVEN\_PRC0/1]). If this mode is used in conjunction with a Frequency Modulated Peripheral Clock Divider (FMPERDIV) value of divide-by-4 or divide-by-8, multiple interrupt requests may be indicated when only a single interrupt event has occurred. This affects any peripheral interrupt request.

INTC software vector mode is not affected and works correctly regardless of FMPERDIV setting.

### Workaround

Use software interrupt vector mode, if possible.

If hardware interrupt vector mode is required, use only FMPERDIV setting of divide-by-2.

## ERR009863: PSI5: Enabling interrupts in the General Interrupt Control Register (PSI5\_CH0\_GICR) has no effect

### Description

Interrupt sources described in the Peripheral Sensor Interface 5 (PSI5) General Interrupt Control Register (PSI5\_CH0\_GICR) cannot cause an interrupt. Enabling interrupt control bits in this register has no effect. The pending interrupt status for these events, however, will be correctly indicated in the General Interrupt Status Register (PSI5\_CH0\_GISR).

### Workaround

In order to respond to these events, the system must poll the status bits in the PSI5\_CH0\_GISR register.

## ERR050575: eMIOS: Any Unified Channel running in OPWMCB mode may function improperly if the lead or trail dead time insertion features is used and its timebase is generated by Unified channel in MCB mode

### Description

The Unified channel (UC) configured in Center Aligned Output Pulse Width Modulation Buffered (OPWMCB) mode is not working properly when:

1. It's timebase is sourced from the UC configured in Modulus Counter Buffered (MCB) mode.
2. The lead or trail dead time insertion features is used.
3. Its channel prescaler is different than timebase channel prescaler.

### Workaround

Channel configured in OPWMCB mode with lead or trail dead time insertion features enabled must have channel prescaler equal to the timebase channel prescaler configured in MCB mode.

## ERR009856: MPC5777C: Incorrect operation of Software Watchdog Timers in debug mode

### Description

While the device is in debug mode, if one e200z7 core is single-stepped while the other core is halted, the Software Watchdog Timers (SWT) for both cores will start and then continue to run instead of stopping after the step is executed. If both cores are single-stepped at the same time, the SWTs will halt as expected after the step.

### Workaround

During debug mode, an e200z7 core should not be allowed to single-step while the other core is halted. The debug tool should be updated to always step both cores at the same time when a step is requested on either core by the user.

## ERR008313: EQADC: TUE specification not met

### Description

The Enhanced Queued Analog-to-Digital Converter (EQADC) Total Unadjusted Error (TUE) specification in the device datasheet lists separate error levels for ADC clock of 16.5MHz and 33MHz, respectively. Neither the specification of +/- 4 counts at 16.5MHz, nor the specification of +/- 6 counts at 33MHz is met. Specifications for "Gain with Calibration" (GAINWC) and "Offset with Calibration" (OFFWC), which contribute to TUE, are also not met.

Regardless of ADC clock speed, the TUE, GAINWC, and OFFWC specifications are each +/- 8 counts. A future release of the device datasheet will reflect the new specification level.

### Workaround

Ensure that application use-cases can tolerate the updated error specifications. If greater accuracy is required, some improvement can be gained by performing multiple conversions and averaging results to reduce noise-related errors.

## ERR007904: PASS: Programming Group Lock bit (PGL) can be de-asserted by multiple masters writing the correct password sections to the CINn registers.

### Description

The eight Challenge Input Registers (CINn) in the Password and Device Security Module (PASS) where the 256-bit unlock lock password (8 x 32-bit registers) is provided, can be written by multiple masters. If the written password is correct even though it has been provided from different masters, the password Group Lock (PASS PGL) in the Password Group n Lock 3 Status register (PASS\_LOCK3\_PGn) is de-asserted and UnLockMaster (MSTR) is set to 0xF.

Therefore, internal registers would not be writable by any of the master other than master whose ID is 0xF if the Master Only (MO) bit is set PASS\_LOCK3\_PGn.

If a Master wants to update internal registers, it needs to unlock the PASS by writing into all the 8 Password registers.

### Workaround

Set the master only bit inside the PASS (LOCK3\_PGn.MSTR) to block other master accesses to the unlocked registers. If the written password has been provided from different masters, a single master should perform the unlock operation again by writing into all the 8 password registers.

## ERR008251: DECFIL: timestamp may be lost in edge trigger mode

### Description

The Enhanced Queued Analog-to-Digital Converter (eQADC) supports a conversion command that configures it to send a timestamp along with the specified ADC conversion data to the Decimation Filter (DECFIL) for digital processing. The DECFIL receives the data and the timestamp, and updates internal registers with these two values. When the DECFIL is configured for edge triggered output by setting the Triggered Output Result Enable bit in the Module Configuration Register (DECFIL\_MCR[TORE]) and setting the Trigger Mode bitfield to either 2b00 or 2b10, and a trigger edge is detected, the DECFIL loads an Internal Output Buffer register (DECFILT\_JOB) with the conversion data, and then the timestamp data. This register is intended to hold data to be returned on one of the two Parallel Side Interfaces (PSI0 or PSI1). In the case where a trigger edge occurs and DECFILT\_JOB is loaded with the conversion and timestamp data, and then a second trigger edge occurs before any new conversion and timestamp data has been received by the DECFILT, the DECFILT will provide only the initial conversion data, and will not provide the initial timestamp data.

The level triggered mode is not affected by this issue.

### Workaround

When the DECFILT has been configured for edge triggered output buffer mode, ensure that the trigger edge rate is slower than the input data rate of the decimation filter. That is, be sure that there is always a new conversion arriving at the DECFILT before any new output trigger edge is detected. If the DECFILT is not receiving timestamps from the eQADC, this limitation is not required.

## ERR010610: NPC: Core cannot be halted if NPC is not enabled when entering debug mode

### Description

When attempting to halt a core via the corresponding COREn bit of the SIU\_HLTn register while in debug mode and if the core Nexus interface is enabled, the Nexus Port Controller (NPC) tracing must also be enabled or the core will not halt. Nexus is enabled in the core if any Nexus feature is accessed by a tool (executing the Nexus\_enable command to use the Nexus Read/Write Access feature to access memory), even if trace (program, data, ownership, watchpoint, data acquisition) is not enabled.

This also affects the ability to reset a single core via the SIU\_RSTVECn[RST] bit. Normally, if both SIU\_RSTVEC[RST] and SIU\_HLT1[COREn] bit is set for a particular core, that core will enter reset. The problem described above will prevent that unless the workaround is employed. Attempting to reset both cores simultaneously, however, will still generate a system internal reset as described in the reference manual, regardless of this errata condition.

#### Workaround

Enable NPC tracing by enabling the Message Clock Output (MCKO) in the NPC Port Configuration Register (NPC\_PCR) when a debugger is connected to allow a core to halt when requested.

### **ERR011295: EMIOS: In OPWFMB mode, A1/B1 registers do not get reloaded with A2/B2 register values if counter value returns 0x1 after counter wrap condition**

#### Description

In Output Pulse-Width and Frequency Modulation Buffered (OPWFMB) mode, A1/B1 registers do not get reloaded with A2/B2 register values if counter value returns 0x1 after counter wrap condition.

In order to avoid the counter wrap condition make sure internal counter value is within the 0x1 to B1 register value range when the OPWFMB mode is entered. Also overwriting of Channel Count register by forcing 'freeze' in OPWFMB mode should not take internal counter outside 0x1 to B register value.

#### Workaround

In order to avoid the counter wrap condition:

1. Make sure internal counter value is within the 0x1 to (B1 register) value range when the OPWFMB mode is entered.
2. Overwrite of Channel Count register by forcing 'freeze' in OPWFMB mode should not be outside the range of 0x1 to (B register) value.

### **ERR011294: EMIOS: OPWFMB and MCB mode counter rollover resets the counter to 0x0 instead of 0x1 as mentioned in the specification**

#### Description

When the enhanced Modular Input/Output System (eMIOS) is used in Output Pulse-Width and Frequency Modulation Buffered (OPWFMB) or Modulus Counter Buffered (MCB) modes, when the counter rolls over, the counter returns to 0x0 instead of 0x1 as specified in the reference manual.

#### Workaround

In order to avoid the counter wrap condition:

1. Make sure internal counter value is within the 0x1 to (B1 register) value range when the OPWFMB mode is entered.
2. Overwrite of Channel Count register by forcing 'freeze' in OPWFMB mode should not be outside the range of 0x1 to (B register) value.

### **ERR010025: SWT: System clock source must be set to IRC prior to changing SWT clock selection**

#### Description

The Software Watchdog Timer (SWT) Control Register Clock Select bit (SWT\_CR[CSL]) must only be changed from 0 to 1 or from 1 to 0 while the system clock source is set to Internal RC Oscillator (IRC). Otherwise, unpredictable behavior may result.



## Workaround

Follow this procedure to change the SWT clock selection:

1. Set the system clock source to IRC.
2. Write SWT\_CR[CSL] to change its value from 0 to 1 or from 1 to 0.
3. If desired, the system clock source may now be changed without affecting proper operation of the device.

## ERR011213: MPC577xC: When an FCCU reset occurs, the Engineering Clock (ENGCLK) output clock and CLKOUT can have a shortened duty cycle.

### Description

When a Fault Collection and Control Unit (FCCU) reset occurs, the Engineering Clock (ENGCLK) and CLKOUT output pins will abruptly drive low potentially resulting in a shortened duty cycle (or truncation of the clock pulse) on that output where the high phase of the clock is either shorter than normal or does not reach the high output level.

The reset output pin (RSTOUT) assertion may occur after a delay following the stopping of ENGCLK, thus the shortened clock pulse may occur while the RSTOUT is not yet asserted.

### Workaround

Any external circuit or device that uses the ENGCLK output or CLKOUT output should be evaluated to ensure it can withstand receiving a shortened clock pulse. For example, an external memory may be disturbed or an external device may operate incorrectly when receiving a shortened clock pulse on its clock input.

## ERR011457: M\_CAN: Unexpected High Priority Message (HPM) interrupt

### Description

The High Priority Message (HPM) Interrupt flag IR.HPM is set erroneously in the following cases:

Configuration A:

- At least one Standard Message ID Filter Element is configured with priority flag set (S0.SFEC = "100"/"101"/"110")
- No Extended Message ID Filter Element configured
- Non-matching extended frames are accepted (GFC.ANFE = "00"/"01")

In configuration A, the HPM interrupt flag is set erroneously on reception of a non-high-priority extended message under the following conditions:

(1) A standard HPM frame is received, and accepted by a filter with priority flag set. Interrupt flag IR.HPM is set as expected for this message.

(2) Next an extended frame is received and accepted because of GFC.ANFE configuration. Interrupt flag IR.HPM is set erroneously for this message.

Configuration B:

- At least one Extended Message ID Filter Element is configured with priority flag set (F0.EFEC = "100"/"101"/"110")
- No Standard Message ID Filter Element configured
- Non-matching standard frames are accepted (GFC.ANFS = "00"/"01")

The HPM interrupt flag is set erroneously on reception of a non-high-priority standard message under the following conditions:

(1) An extended HPM frame is received, and accepted by a filter with priority flag set. Interrupt flag IR.HPM is set as expected for this message.

(2) Next a standard frame is received and accepted because of GFC.ANFS configuration. Interrupt flag IR.HPM is set erroneously for this message.

### Workaround

For configuration A:

Set up an Extended Message ID Filter Element with the following configuration:

- F0.EFEC = "001"/"010" - select Rx FIFO for storage of extended frames
- F0.EFID1 = any value - value not relevant as all ID bits are masked out by F1.EFID2
- F1.EFT = "10" - classic filter, F0.EFID1 = filter, F1.EFID2 = mask
- F1.EFID2 = zero - all bits of the received extended ID are masked out

Now all extended frames are stored in Rx FIFO 0 or Rx FIFO 1 depending on the configuration of F0.EFEC.

Configuration B:

Set up a Standard Message ID Filter Element with the following configuration:

- S0.SFEC = "001"/"010" - select Rx FIFO for storage of standard frames
- S0.SFID1 = any value - value not relevant as all ID bits are masked out by S0.SFID2
- S0.SFT = "10" - classic filter, S0.SFID1 = filter, S0.SFID2 = mask
- S0.SFID2 = zero - all bits of the received standard ID are masked out

Now all standard frames are stored in Rx FIFO 0 or Rx FIFO 1 depending on the configuration of S0.SFEC.

## ERR008225: SDADC: FIFO Flush Reset command requires clearing the Data FIFO Full Flag

### Description

When the Sigma-Delta Analog-to-Digital Converter (SDADC) FIFO is flushed by writing '1' to the FIFO Control Register FIFO Flush Reset bit (SDADC\_FCR[FRST]), the FIFO is correctly flushed, but the Status Flag Register Data FIFO Full Flag (SDADC\_SFR[DFFF]) may be incorrectly asserted, indicating the FIFO is full when it is empty..

### Workaround

Clear SDADC\_SFR[DFFF] by writing a '1' to this field after performing a FIFO Flush Reset command or after the FIFO is disabled.

## ERR007991: FLASH: Rapid Program or Erase Suspend fail status

### Description

If a flash suspend operation occurs during a 5us window during a verify operation being executed by the internal flash program and erase state machine, and the suspend rate continues at a consistent 20us rate after that, it is possible that the flash will not exit the program or erase operation. A single suspend during a single program or erase event will not cause this issue to occur.

Per the flash specification, a flash program or erase operation should not be suspended more than once every 20 us, therefore, if this requirement is met, no issue will be seen. IF the suspend rate is faster than 20 us continuously, a failure to program/erase could occur.

### Workaround

When doing repeated suspends during program or erase ensure that suspend period is greater than 20us.

## ERR010578: MPC577xC: The Temperature Sensor may cause extended reset times

### Description

This device enables the Temperature Sensor Reset Enable bits (REE) by default during reset, and during reset, the Temperature Sensor analog block is powered down for a portion of the reset time.

This could lead to a condition where supply transitions while the Temperature Sensor analog block powers up may cause the Temperature Sensor flags to set, which would start the reset sequence over.

This could result in a longer reset cycle.

### Workaround

The UTEST Power Management Controller (PMC) Temperature Sensor Reset Event Enable Control (REE TSPSNS) DCF client should be updated twice. The first value should be 0x00000040 (to load zeros into the REE bits), and the second value should be 0x00000000 (to allow software writes to make updates again).

After that, the UTEST PMC TS REE DCF should never be written to enable the Temp Sensor resets. This should be done via software updates to the PMC\_REE\_TD register.

In addition, when exiting from reset, check PMC\_ESR\_TD. If any of these bits are set to 1, the temperature should be checked by using the Temperature Sensor ADC measurement. If the temperature is within the valid range, then the PMC\_ESR\_TD bits should be cleared (by writing a 1 to their locations). After this, the PMC\_REE\_TD bits can be enabled to allow subsequent temperature event resets.

## ERR007422: FLASH: Pipeline should not be enabled on the flash

### Description

Enabling of pipelining of the Flash Address Pipeline Control (APC) bits in the Platform Flash Configuration Register 1 (PFLASH\_PFCR1) does not give optimum system performance. Pipelining the accesses will actually decrease the performance of the flash when there are multiple flash masters. The APC should be set to a value of 0x4.

### Workaround

Disable pipelined flash accesses by properly setting the Address Pipeline Control bits in the Platform Flash Configuration Register 1 to Pipelined accesses disabled and one wait state (PFLASH\_PFCR1[APC] = 0x4).

## ERR010415: SDADC: Additional DMA requests generated when using watchdog threshold crossover event

### Description

If the Sigma-Delta Analog-to-Digital Converter (SDADC) is configured to generate DMA requests for the watchdog threshold crossover event (SDADC\_MCR[WDGEN]=0b1 and SDADC\_RSER[WTHDIRS]=0b1) the DMA may transfer more data than is actually available.

### Workaround

If it is necessary to use the watchdog threshold crossover event, configure the SDADC to use interrupt requests instead of DMA requests (SDADC\_RSER[WTHDIRS]=0b0).

## ERR011293: EMIOS: For any UC operating in OPWFMB mode the Channel Count register should not be written with a value greater than Channel B Data register value

### Description

For any Unified Channel (UC) running in Output Pulse-Width and Frequency Modulation Buffered (OPWFMB) mode, Channel Control Register MODE bitfield = 7'h1011000 or 7'h1011010, the internal counter runs from 0x1 to Channel B Data register value. The internal counter can be overwritten by software using the Channel Count register during 'freeze' operation.

If a counter wrap occurs due to overwriting of the counter with a value greater than its expiry value (B Data Register value); then the output signal behavior cannot be guaranteed.

### Workaround

For any UC operating in OPWFMB mode the Channel Count register should not be written with a value greater than Channel B Data register value.

## ERR007223: FCCU: FCCU\_IRQ\_EN register is writeable in all operating modes

### Description

In the Fault Collection and Control Unit (FCCU), the FCCU Interrupt Enable register (FCCU\_IRQ\_EN) is writable (and readable) in all states (NORMAL, CONFIG, FAULT and ALARM) while in some revisions of the documentation it is stated "This register is writable only in the CONFIG state".

### Workaround

Take into account that FCCU\_IRQ\_EN register can be written in all the states of the FCCU.

Please ignore the following text in the description of FCCU\_IRQ\_EN register if you find it in the documentation revision in hand: "This register is writable only in the CONFIG state."

## ERR009336: TDM: Erase of TDR flash block may be blocked by the TDM - CSE systems

### Description

Erase of a flash block associated with a Tamper Detect Region (TDR) may be improperly blocked by the Tamper Detect Module (TDM) in a system with an active CSE (Cryptographic Services Engine). When this occurs, the erase operation will be shown as complete with Program/Erase Good (c5FMC\_MCR.DONE=1 and C55FMC\_MCR.PEG=1), but the block will not be erased.

### Workaround

Avoid CSE program/erase operations when erasing a flash block covered by a TDR. Alternatively, when erase of a flash block is attempted, but it completes with C55FMC\_MCR.PEG=1 and is not erased, a new diary entry should be written before attempting to erase the flash block again.

## ERR007120: NZxC3: DQTAG implemented as variable length field in DQM message

### Description

The e200zx core implements the Data Tag (DQTAG) field of the Nexus Data Acquisition Message (DQM) as a variable length packet instead of an 8-bit fixed length packet. This may result in an extra clock ("beat") in the DQM trace message depending on the Nexus port width selected for the device.

### Workaround

Tools should decode the DQTAG field as a variable length packet instead of a fixed length packet.

## ERR010900: FCCU: False indication of a fault state for a single safe clock period can be generated on the error output pin

### Description

The error out pin from the Fault Collection and Control Unit (FCCU) may pulse to a logic low (0b0) when the following conditions are fulfilled:

- software changes the error out protocol from a toggling protocol to a not-toggling protocol, and programs the FCCU\_CFG.FCCU\_SET\_AFTER\_RESET bit to 0b1
- software switches the Fault Collection and Control Unit (FCCU) state machine from CONFIG to NORMAL state

The duration of the glitch is equal to a single clock period of the Internal RC oscillator and there is a 50% of probability of the pulse occurring.

### Workaround

Split the configuration of the FCCU in 2 phases.

During the first phase, software should do the following:

- 1) move the FCCU to the CONFIG state
- 2) configure the FCCU including the error out protocol, but without setting the FCCU\_CFG.FCCU\_SET\_AFTER\_RESET flag to 0b1 (leave as 0b0)
- 3) exits to the NORMAL state

During the second phase, software should do the following:

- 4) move the FCCU to the CONFIG state
- 5) set the FCCU\_CFG.FCCU\_SET\_AFTER\_RESET flag to 0b1
- 6) exit to the NORMAL state

Note: The default (after reset) error out protocol is the Dual Rail. Since this is a toggling protocol, the software must execute the above steps each time the user wants to switch to a non-toggling error out protocol.

## ERR007545: JTAGC: TCK low to TDO data valid spec is not met

### Description

The datasheet specification for Test Clock (TCK) low to Test Data Out (TDO) valid is not met on this device. The original spec is 10ns. This device requires 14ns.

### Workaround

Use modified timing to latch data on the falling edge of TCK.

## ERR009250: PASS: JTAG password not working during reset

### Description

The Debug Interface Access cannot be enabled by supplying the JTAG password during reset.

## Workaround

To enable the Debug Interface Access, supply the JTAG password after reset.

## ERR009595: FlexCAN: Corrupted frame possible if Freeze Mode or Low Power Mode are entered during a Bus-Off state

### Description

In the Flexible Controller Area Network (FlexCAN) module, if the Freeze Enable bit (FRZ) of the Module Configuration Register (MCR) is asserted and the Freeze Mode is requested by asserting the Halt bit (HALT) of the MCR register during the Bus Off state, the transmission after exiting the Bus-Off condition will be corrupted. The issue occurs only if a transmission is pending before the freeze mode request. In addition, the same issue can happen if Low-Power Mode is requested instead of Freeze Mode.

### Workaround

The workaround depends on whether the bus-off condition occurs prior to requesting Freeze mode or low power mode.

A) Procedure to enter Freeze Mode:

1. Set the Freeze Enable bit (FRZ) in the Module Control Register (MCR).
2. Check if the Module Disable bit (MDIS) in MCR register is set. If yes, clear the MDIS bit.
3. Poll the MCR register until the Low-Power Mode Acknowledge (LPMACK) bit in MCR is cleared (timeout for software implementation is 2 CAN Bits length).
4. Read the Fault Confinement State (FLTCONF) field in the Error and Status 1 Register (ESR1) to check if FlexCAN is in bus off state. If yes, go to step 5A. Otherwise, go to step 5B.
- 5A. Set the Soft Reset bit (SOFTTRST) in MCR.
- 6A. Poll the MCR register until the Soft Reset (SOFTTRST) bit is cleared (timeout for software implementation is 2 CAN Bits length).
- 7A. Poll the MCR register until the Freeze Acknowledge (FRZACK) bit is set (timeout for software implementation is 2 CAN Bits length).
- 8A. Reconfigure the Module Control Register (MCR).
- 9A. Reconfigure all the Interrupt Mask Registers (IMASKn).
- 5B. Set the Halt FlexCAN (HALT) bit in MCR.
- 6B. Poll the MCR register until the Freeze Acknowledge (FRZACK) bit is set (timeout for software implementation is 178 CAN Bits length).

NOTE: The time between step 4 and step 5B must be less than 1353 CAN bit periods.

B) Procedure to enter in Low-Power Mode:

1. Enter in Freeze Mode (execute the procedure A).
2. Request the Low-Power Mode.
3. Poll the MCR register until the Low-Power Mode Acknowledge (LPMACK) bit in MCR is set (timeout for software implementation is 2 CAN Bits length).

## ERR007511: LFAST: Maximum data rate is 240Mbps

### Description

The LVDS Fast Asynchronous Serial Transmission (LFAST) module in this device will operate at a maximum data rate of 240Mbps instead of the 320Mbps maximum rate specified in the device datasheet.

## Workaround

Do not operate the LFAST module at any data rate greater than 240Mbps.

## ERR050246: FlexCAN: Receive Message Buffers may have its Code Field corrupted if the Receive FIFO function is used

### Description

If the Code Field of a Receive Message Buffer is corrupted it may deactivate the Message Buffer, so it is unable to receive new messages. It may also turn a Receive Message Buffer into any type of Message Buffer as defined in the Message buffer structure section in the device documentation.

The Code Field of the FlexCAN Receive Message Buffers (MB) may get corrupted if the following sequence occurs.

- 1- A message is received and transferred to an MB (i.e. MBx)
- 2- MBx is locked by software for more than 20 CAN bit times (time determines the probability of erratum to manifest).
- 3- SMB0 (Serial Message Buffer 0) receives a message (i.e. message1) intended for MBx, but destination is locked by the software (as depicted in point 2 above) and therefore NOT transferred to MBx.
- 4- A subsequent incoming message (i.e. message2) is being loaded into SMB1 (as SMB0 is full) and is evaluated by the FlexCAN hardware as being for the FIFO.
- 5- During the message2, the MBx is unlocked. Then, the content of SMB0 is transferred to MBx and the CODE field is updated with an incorrect value.

The problem does not occur in cases when only Rx FIFO or only a dedicated MB is used (i.e. either RX MB or Rx FIFO is used). The problem also does not occur when the Enhanced Rx FIFO and dedicated MB are used in the same application. The problem only occurs if the FlexCAN is programmed to receive in the Legacy FIFO and dedicated MB at the same application.

### Workaround

This defect only applies if the Receive FIFO (Legacy Rx FIFO) is used. This feature is enabled by RFEN bit in the Module Control Register (MCR). If the Rx FIFO is not used, the Receive Message Buffer Code Field is not corrupted.

If available on the device, use the enhanced Rx FIFO feature instead of the Legacy Rx FIFO. The Enhanced Rx FIFO is enabled by the ERFEN bit in the Enhanced Rx FIFO Control Register (ERFCR).

The defect does not occur if the Receive Message Buffer lock time is less than or equal to the time equivalent to 20 x CAN bit time.

The recommended way for the CPU to service (read) the frame received in a mailbox is by the following procedure:

1. Read the Control and Status word of that mailbox.
2. Check if the BUSY bit is deasserted, indicating that the mailbox is not locked. Repeat step 1) while it is asserted.
3. Read the contents of the mailbox.
4. Clear the proper flag in the IFLAG register.
5. Read the Free Running Timer register (TIMER) to unlock the mailbox

In order to guarantee that this procedure occurs in less than 20 CAN bit times, the MB receive handling process in software (step 1 to step 5 above) should be performed as a 'critical code section' (interrupts disabled before execution) and should ensure that the MB receive handling occurs in a deterministic number of cycles.

## ERR010378: SDADC: Incorrect data provided when FIFO is disabled and FIFO overwrite is enabled

### Description

The Sigma-Delta Analog-to-Digital Converter (SDADC) allows continuous data acquisition. When the overwrite functionality is enabled (FCR[FOWEN] = 1) in the FIFO Control Register (FCR), previously converted data will eventually be overwritten if it is not read before new data is available. In case the overwrite functionality is enabled (FCR[FOWEN] = 1) in the FIFO Control Register (FCR) together with the disabling of the associated FIFO buffer (FCR[FE] = 0), the Data FIFO Empty flag in the Status Flag register (SFR[DFEF]) will toggle high (Data FIFO is empty) and low (Data FIFO is not empty). If the Converted Data Register (CDR) is read while in the "Data FIFO is empty" state, then the previous converted data is provided rather than newest converted data.

### Workaround

Always disable the FIFO overwrite functionality in the FIFO Control Register (FCR[FOWEN]=0) if the FIFO buffer is disabled (FCR[FE]=0).

## ERR007547: FEC: Transmit signal hold time reduced

### Description

The Fast Ethernet Controller (FEC) Media Independent Interface (MII) transmit signal hold time specification is reduced from 5ns to 4.5ns on this device.

### Workaround

Ensure Ethernet physical interface (PHY) devices connected via MII are able to tolerate the reduced hold time specification.

## ERR007339: STCU2: STCU2 fault injected by FCCU is self clearing

### Description

In the Self-Test Control Unit (STCU2), a fault can be injected by the Fault Collection and Control Unit (FCCU) in order to verify the correct behavior of the interface (fake fault).

The STCU\_LMBIST\_USR\_ERR signal, which is connected to the FCCU input #8, generates only a pulse when an error is injected to this signal by the FCCU.

This is different to other signals from STCU2, where injected faults remain asserted until explicitly cleared.

### Workaround

Use a software recoverable fault (select-able with FCCU\_RF\_CFG) for FCCU input #8, when a fault is injected into the STCU2.

## ERR009570: FCCU: FOSU may assert reset when a hardware recoverable fault of width less than one safe clock period occurs

### Description

The Fault Collection and Control Unit Output Supervision Unit (FOSU) may issue a reset if all of the following conditions are present:

- An input fault is programmed as hardware recoverable in a FCCU Non-Critical Fault Configuration Register (FCCU\_NCF\_CFGn)
- The only reaction programmed for this fault is FCCU Error Output signaling (FCCU\_EOUT\_SIG\_ENn)
- The source of the fault signal is asserted for less than one safe clock period. The safe clock for this device is the internal RC oscillator (IRC).



### Workaround

(1) Program "Request reset pulse" in the associated FCCU Non-Critical Fault State Configuration (FCCU\_NCFS\_CFGn) register for that hardware recoverable fault in addition to the EOUT signaling.

(2) Alternatively, if the reset reaction is not desired, configure the fault as software recoverable.

## ERR009804: PMC: LVD/HVD Event Status Register does not consistently indicate the reset source

### Description

The Power Management Controller (PMC) LVD/HVD Event Status Register (PMC\_LVD\_HVD\_EVENT\_STATUS) does not always indicate the reset source for a High-Voltage Detect (HVD) or Low-Voltage Detect (LVD) event when reset is enabled through the PMC Reset Event Enable register (PMC\_REE), although the reset itself occurs.

### Workaround

Disable LVD/HVD resets in PMC\_REE by clearing all bits to zero. Instead, configure the Fault Collection Control Unit (FCCU) reaction to reset the part upon LVD or HVD fault events. These are Non-Critical Fault (NCF) channels 1 and 2. After any reset event caused by the FCCU LVD/HVD faults, reading the PMC\_LVD\_HVD\_EVENT\_STATUS register will correctly identify the reset source.

Example of configuration and reset source check sequence:

- 1) Configure PMC\_REE = 0x0000 to disable all LVD/HVDs reset
- 2) Configure FCCU registers to generate reset  
FCCU.LVD\_ERROR(NCF=1) and/or  
FCCU.HVD\_ERROR(NCF=2)
- 3) Over/under operating voltages can generate HVD/LVD reset
- 4) Check if reset was generated through FCCU
- 5) Check FCCU registers indicate source of reset
- 6) Check PMC LVD HVD Status occurrence

Note that this FCCU workaround has a limited selection resolution regarding the LVD/HVD source that causes a reset event when compared to PMC\_REE configuration. The FCCU cannot individually enable/distinguish which LVD source caused the FCCU LVD request. The same applies to HVD.

## ERR009001: eSCI: Incorrect behavior while in LIN Standard Bit error detection mode

### Description

After a Local Interconnect Network (LIN) wake-up signal frame is transmitted from a master device while in Standard Bit error detection mode (eSCI\_CR2[FBR] = 0), a bit error is detected in any subsequent LIN Transmit (TX) or Receive (RX) frames sent from the master device. After the bit error is detected, the Bit Error Interrupt Flag (eSCI\_IFSR1[BERR]) is asserted, and the LIN controller will not generate TX or RX frames.

### Workaround

Workaround 1: Reset the LIN Protocol Engine of the eSCI controller by writing 1 and then a 0 to the LIN Protocol Engine Stop and Reset bit in LIN Control Register 1 (eSCI\_LCR1[LRES]) after a complete wake-up frame is sent.

Workaround 2: Use the LIN module in Fast Bit error detection mode, and do not use the Standard Bit error detection mode. Fast Bit Error detection mode can be enabled by writing 1 to the Fast Bit Error Detection bit in Control Register 2 (eSCI\_CR2[FBR]=1).

## ERR008042: FCCU: EOUT signals are active, even when error out signaling is disabled

### Description

Every time the Fault Collection and Control Unit (FCCU) moves into fault state caused by an input fault for which the error out reaction is disabled (`FCCU_EOUT_SIG_ENn[EOUTENx]=0`), the Error Out 1 and 2 (`EOUT[0]` and `EOUT[1]`) will become active for a duration of 250 us plus the value programmed into the FCCU Delta Time register (`FCCU_DELTA_T[DELTA_T]`). EOUT is not affected if the FCCU moves into the alarm state that generates an interrupt (IRQ), if the Fault is cleared before the alarm timeout.

This erratum does not affect the outputs of other pins (for example, for communication modules like CAN/Flexray). Only the EOUT signal is impacted.

### Workaround

There are three possible workarounds:

- 1) Enable EOUT signaling for all enabled error sources.
- 2) In case external device (which evaluates EOUT) can communicate with the MCU, the following procedure could be used:
  - a) Program any duration of EOUT as per application needs (`FCCU_DELTA_T[DELTA_T]`)
  - b) For faults requiring error out reaction, the software shall validate EOUT via separate communication channel (like I2C) while EOUT is asserted.
  - c) External device shall implement a timeout mechanism to monitor EOUT validation by separate channel.
  - d) Following scenarios shall be considered as valid EOUT reactions:
    - d1) Validation is performed while EOUT is asserted
    - d2) Timeout occurs but no validation and EOUT is still asserted.
- 3) In case external device (which evaluates EOUT) cannot communicate with the MCU, following procedure could be used:
  - a) Program the error out duration to a duration  $x$  (`FCCU_DELTA_T[DELTA_T]`).
  - b) For faults requiring error out reaction, clear the fault after the pin has continued to be asserted for a longer duration (for example  $2 \cdot \text{duration } x$ ). This will artificially create a long pulse on EOUT.
  - c) For faults which do not require error out reaction, clear the fault within duration  $x$ . This will artificially create a short pulse on EOUT.
  - d) External device should ignore short pulse of duration  $x$  while recognizing longer pulses as valid reaction.
  - e) While clearing the fault, the associated software shall check the pending faults.

## ERR008341: FlexCAN: Entering Freeze Mode or Low Power Mode from Normal Mode can cause the FlexCAN module to stop operating.

### Description

In the Flexible Controller Area Network (FlexCAN) module, if the Freeze Enable bit (FRZ) in the Module Configuration Register (MCR) is asserted and the Freeze Mode is requested by asserting the Halt bit (HALT) in MCR, in some cases, the Freeze Mode Acknowledge bit (FRZACK) in the MCR may never be asserted.

In addition, the Low-Power Mode Acknowledge bit (LPMACK) in the MCR may never be asserted in some cases when the Low-Power Mode is requested.

Under the two scenarios described above, the loss of ACK assertion (FRZACK, LPMACK) causes a lock condition. A soft reset action is required in order to remove the lock condition.

The change from Normal Mode to Low-Power Mode cannot be done directly. Instead, first change mode from Normal to Freeze Mode, and then from Freeze to Low-Power Mode.

## Workaround

To avoid the lock condition, the following procedures must be used:

A) Procedure to enter in Freeze Mode:

1. Set both the Freeze Enable bit (FRZ) and the Halt bit (HALT) in the Module Control Register (MCR).
2. Check if the Module Disable bit (MDIS) in MCR register is set. If yes, clear the MDIS bit.
3. Poll the MCR register until the Freeze Mode Acknowledge bit (FRZACK) in MCR is set or the timeout is reached (see NOTE below).
4. If the Freeze Mode Acknowledge bit (FRZACK) is set, no further action is required. Skip steps 5 to 8.
5. If the timeout is reached because the Freeze Mode Acknowledge bit (FRZACK) is still cleared, then set the Soft Reset bit (SOFTRST) in MCR.
6. Poll the MCR register until the Soft Reset bit (SOFTRST) bit is cleared.
7. Reconfigure the Module Control Register (MCR)
8. Reconfigure all the Interrupt Mask Registers (IMASKn).

After Step 8, the module will be in Freeze Mode.

NOTE: The minimum timeout duration must be equivalent to:

- a) 730 CAN bits if the CAN FD Operation Enable bit (FDEN) in MCR is set (CAN bits calculated at arbitration bit rate),
- b) 180 CAN bits if the FDEN bit is cleared.

B) Procedure to enter in Low-Power Mode:

1. Enter in Freeze Mode (execute the procedure A).
2. Request the Low-Power Mode.
3. Poll the MCR register until the Low-Power Mode Acknowledge (LPMACK) bit in MCR is set.

## ERR009797: eSCI: Unable to send next frame after timeout in LIN mode

### Description

When generating a Local Interconnect Network (LIN) Transmit (Tx) and Receiver (Rx) frame, the Enhanced Serial Communication Interface (eSCI) module should first send the Header as per the LIN protocol. However, after the Slave Timeout Interrupt Flag (STO) in the Interrupt Flag and Status Register 2 (eSCI\_IFSR2) for the previous LIN Rx Frame is asserted (eSCI\_IFSR2[STO]=1), the eSCI module is not able to generate the next Header, it remains in a suspended state.

### Workaround

Perform the following actions in this order:

- (1) Set the LIN Protocol Engine Stop and Reset (LRES) control bit to '1' in the LIN Control Register 1 (eSCI\_LCR1).
- (2) Wait until the status bits DACT, WACT, LACT, TACT, and RACT in the Interrupt Flag and Status Register (eSCI\_IFSR1) are cleared to '0'.
- (3) Clear LRES in eSCI\_LCR1 to '0'.
- (4) Begin transmission of the LIN Header for the next frame.

## ERR007425: SENT: Unexpected NUM\_EDGES\_ERR error in certain conditions when message has a pause pulse

### Description

When the Single Edge Nibble Transmission (SENT) Receiver (SRX) is configured to receive a pause pulse (Channel 'n' Configuration Register - CHn\_CONFIG[PAUSE\_EN] = 1) the NUM\_EDGES error can get asserted spuriously (Channel 'n' Status Register - CHn\_STATUS[NUM\_EDGES\_ERR] = 1) when there is any diagnostic error (other than number of expected edges error) or overflow in the incoming messages from the sensor.

### Workaround

Software can distinguish a spurious NUM\_EDGES\_ERR error from a real one by monitoring other error bits. The following tables will help distinguish between a false and real assertion of NUM\_EDGES\_ERR error and other errors. Software should handle the first error detected as per application needs and other bits can be evaluated based on these tables. The additional error may appear in the very next SENT frame. Table 1 contains information due to erratum behavior. Table 2 contains clarification of normal NUM\_EDGES\_ERR behavior.

**Table 1. Erratum behavior of NUM\_EDGES\_ERR**

Table:

First Error Detected	Other error bits asserted	Cause for extra error bits getting asserted	Action
NIB_VAL_ERR	NUM_EDGES_ERR asserted twice	Upon detection of the first error, the state machine goes into a state where it waits for a calibration pulse, the first NUM_EDGES_ERR error is for the current message as the state machine does not detect an end of message. The second error comes when both the Pause pulse and the Calibration pulse are seen as back to back calibration pulses and no edges in between.	Ignore both NUM_EDGES_ERR error
FMSG_CRC_ERR	NUM_EDGES_ERR asserted twice	Same as NIB_VAL_ERR.	Ignore both NUM_EDGES_ERR errors
CAL_LEN_ERR	NUM_EDGES_ERR asserted once	Since the calibration pulse is not detected as a valid calibration pulse, the internal edges counter does not detect the end of one message and start of bad message (which has CAL_LEN_ERR); hence the NUM_EDGES_ERR gets asserted.	Ignore NUM_EDGES_ERR error
FMSG_OFLW	NUM_EDGES_ERR asserted once (random occurrence)	A message buffer overflow may lead the state machine	Ignore NUM_EDGES_ERR error

		to enter a state where it waits for a calibration pulse (behavior also seen in ERR007404). When in this state, the state machine can detect both a Pause pulse and a Calibration pulse as back to back calibration pulses and no edges in between. Then, the NUM_EDGES_ERR can get asserted. Since entry into this state is random, the error can be seen occasionally.	
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**Table 2. Expected behavior, clarification of NUM\_EDGES\_ERR cases**

Table:

First Error Detected	Other error bits asserted	Cause for extra error bits getting asserted	Action
NUM_EDGES_ERR (when edges are less than expected)	NIB_VAL_ERR is asserted	When the actual number of edges in the message are less than expected, then a pause pulse gets detected as a nibble since the state machine expects nibbles when actually there is a pause pulse present. This generates NIB_VAL_ERR.	Ignore the NIB_VAL_ERR
NUM_EDGES_ERR (when edges are more than expected)	NIB_VAL_ERR and PP_DIAG_ERR are asserted	When the actual number of edges in a message are more than expected, then after receiving the programmed number of data nibbles, the state machine expects a pause pulse. However, the pause pulse comes later and gets detected as a nibble and hence NIB_VAL_ERR is asserted. Since the message length is not correct, PP_DIAG_ERR is also asserted.	Ignore NIB_VAL_ERR and PP_DIAG_ERR

### ERR011469: M\_CAN: Message transmitted with wrong arbitration and control fields

#### Description

Under the following conditions, the Modular Controller Area Network (M\_CAN) module may transmit a message with wrong ID, format fields, and Data Length Code (DLC):

- M\_CAN is in state "Receiver" (M\_CAN\_PSR[ACT] = 10), with no pending transmission

- A new transmission is requested before the 3rd bit of Intermission is reached
- The CAN bus is sampled dominant at the third bit of Intermission, which is treated as Start of Frame (SoF) (see: ISO11898-1:2015 Section 10.4.2.2). This dominant level at the 3rd bit of Intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

Under the conditions listed above, the following can occur:

- The shift register is not loaded with ID, format fields, and DLC of the requested message
- The M\_CAN will start arbitration with wrong ID, format fields, and DLC on the next bit
- In case the ID wins arbitration, a CAN message with wrong ID, format fields, and DLC is transmitted, however this message will have a valid Cyclic Redundancy Check (CRC) and therefore will appear to the receiver as a valid frame with no errors. The incorrect format fields and/or DLC may cause the data field to be truncated or padded, but the CRC will be computed after these changes and will be valid for the transmitted frame.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus. No error is detected by the transmitting M\_CAN
- If the message loses arbitration or is disturbed by an error, it is re-transmitted with correct arbitration and control fields.

### Workaround

If another transmission is already pending or the M\_CAN is not in state "Receiver" (i.e. When M\_CAN\_PSR[ACT] != 10), a new transmission may be requested without causing this issue.

If no transmission is pending and the M\_CAN is in state "Receiver" (M\_CAN\_PSR[ACT] = 10) then the application must avoid requesting the new transmission during the critical time window between the sample points of the 2nd and 3rd bit of Intermission.

To accomplish this, the application software can evaluate the Rx Interrupt flags M\_CAN\_IR[DRX], M\_CAN\_IR[RF0N], and M\_CAN\_IR[RF1N] which are set at the last bit of End of Frame (EoF) when a received and accepted message is validated. The last bit of EoF is followed by three bits of Intermission. Therefore the critical time window has safely terminated three bit times after the Rx interrupt. Now a transmission may be requested by writing to M\_CAN\_TXBAR.

After the interrupt, the application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

If the application cannot reliably avoid the critical time interval described above, another option is to implement additional application-defined protocol checks within the data payload of each message. This protocol can be used by the receiving node to detect messages that have been corrupted by this issue, discard them, and request retransmission. Such a protocol is already recommended for safety-relevant communication as described in the Safety Manual for this device (See sub-section "Fault-tolerant communication protocol" in the Software Requirements chapter).

## ERR050312: M\_CAN: Debug message handling state machine not reset to Idle state when CCCR.INIT is set.

### Description

In case bit CCCR.INIT is set by the Host by writing to register CCCR or when the M\_CAN enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Setting CCCR.CCE does not change RXF1S.DMS.

### Workaround

In case the debug message handling state machine has stopped while RXF1S.DMS="01" or RXF1S.DMS="10" it can be reset to Idle state by hardware reset or by reception of debug messages after CCCR.INIT is reset to zero.

In case the debug message handling state machine has stopped while RXF1S.DMS="11"

with a DMA request active, it can be reset to Idle state by hardware reset or by the completion of the DMA request.

## **ERR008340: NPC: EVTO\_B toggles instead of remaining asserted when used by the DTS if Nexus is not enabled**

### **Description**

When the Development Trigger Semaphore (DTS) module asserts its trigger output on the Event Out (EVTO\_B) pin, the EVTO\_B pin will toggle instead of remaining asserted low if the Nexus Port Controller (NPC) Port Configuration Register MCKO Enable (NPC PCR[MCKO\_EN]) bit is set to 0. If the NPC PCR[MCKO\_EN] bit is set to 1, the EVTO\_B pin behaves as expected and remains asserted low as long as the DTS asserts its trigger output.

### **Workaround**

Always set the MCKO\_EN bit to 1 when using the DTS trigger out function.

## **ERR007204: SENT: Number of Expected Edges Error status flag spuriously set when operating with Option 1 of the Successive Calibration Check method**

### **Description**

When configuring the Single Edge Nibble Transmission (SENT) Receiver (SRX) to receive message with the Option 1 of the successive calibration pulse check method (CHn\_CONFIG[SUCC\_CAL\_CHK] = 1), the number of expected edges error (CHn\_STATUS[NUM[EDGES\_ERR]) gets randomly asserted. Option 2 is not affected as the number of expected edges are not checked in this mode.

The error occurs randomly when the channel input (on the MCU pin) goes from idle to toggling of the calibration pulse.

Note: The Successive Calibration Pulse Check Method Option 1 and Option 2 are defined as follows:

Option 2 : Low Latency Option per SAE specification

Option 1 : Preferred but High Latency Option per SAE specification

### **Workaround**

To avoid getting the error, the sensor should be enabled first (by the MCU software) and when it starts sending messages, the SENT module should be enabled in the SENT Global Control register (by making GBL\_CTRL[SENT\_EN] = 1). The delay in start of the two can be controlled by counting a fixed delay in software between enabling the sensor and enabling the SENT module. The first message will not be received but subsequent messages will get received and there will be no false assertions of the number of expected edges error status bit (CHn\_STATUS[NUM[EDGES\_ERR]).

Alternatively, software can count the period from SENT enable (GBL\_CTRL[SENT\_EN] = 1) to the first expected calibration pulse. If the number of expected edges error status bit (CHn\_STATUS[NUM[EDGES\_ERR]) is asserted, software can simply clear it as there have no messages which have been completely received.

Alternatively, the software can clear this bit at the start and move ahead. When pause pulse is enabled, then NUM\_EDGES will not assert spuriously for subsequent messages which do not have errors in them or cause overflows.

## **ERR009664: DSPI: Frame transfer does not restart in case of DSI parity error in master mode**

### **Description**

In the Serial Peripheral Interface module, in the scenario when:

1. Master/slave mode select bit of module configuration register is set (MCR[MSTR]=0b1) to configure the module in master mode
2. Deserial Serial Interface (DSI) communication is selected via DSPI Configuration field (DCONF) in MCR (MCR[DCONF] = 0b01)

3. Parity reception check on received DSI frame is enabled by setting Parity Enable bit (PE) of DSI configuration register 0 (DSICR0[PE]=0b1)
4. Parity Error Stop (PES) bit of DSI configuration register0 is set (DSICR0[PES]=0b1) which stops DSI frame transfer in case of parity error
5. Parity error is detected on received frame

Then the next frame transfer is stopped, DSI parity error flag bit of status register is set (SR[DPEF] =0b1) and the corresponding DSI parity error interrupt is asserted. Even after the interrupt is serviced and SR [DPEF] is reset, the frame transfer does not restart.

#### Workaround

DSI frame transfer stop in case of parity error detection should be disabled. For this, keep the parity error stop bit of DSI configuration register0 de-asserted (DSICR0 [PES]=0b0).

### ERR007001: EBI: External TA and TEA do not operate properly when internal master does burst aborts to EBI

#### Description

Internal masters such as the e200 cores (with cache enabled), the Enhanced Direct Memory Access modules (eDMAs), and the Fast Ethernet Controller (FEC), can, under certain circumstances, abort a burst access in progress. If this occurs on an EBI access that is using external Transfer Acknowledge (TA) or Transfer Error Acknowledge (TEA), it can cause protocol violations and possibly hang the external bus.

#### Workaround

Do not use external TA, the TEA pin, or non-chip-select accesses with the e200 cores (with cache enabled for EBI address space), the eDMAs, or the FEC. External TA can be disabled for chip-select accesses by clearing the Select External Transfer Acknowledge (SETA) bit in the corresponding EBI Calibration Base Register (EBI\_CAL\_BRn) for that chip select.



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