LS2085_88ARDBE

LS2085A/LS2088A Reference Design Board Errata

Rev. 3 — 28 May 2021 Errata

This document lists and describes all known errata for the LS2085A/LS2088ARDB. It also describes the available workaround for each errata and their detailed explanation, where necessary.

The table below lists the revision history of this document.

Table 1. Revision history

Revision	Date	Description
Rev. 3	28 May 2021	Added new erratum E-00018
Rev. 2	31 August 2017	Updated errata E-00014 and E-00017
Rev. 1	30 April 2017	Updated erratum E-00014
Rev. 0	31 March 2017	Initial public release

This table summarizes all known errata and their workaround for the LS2085A/LS2088ARDB.

Table 2. LS2085A/LS2088ARDB errata summary

Erratum	Found on board revisions	Fixed on board revisions
E-00001: JTAG voltage translator U37 is not required	Rev. B	Rev. B and later
E-00002: COM1 (UART 1/3) port is not working	Rev. B	Rev. C and later
E-00003: CPLD requires 1.8 V standby power for programming	Rev. B	Rev. C and later
E-00004: DDR4 connector U6 has a conflicting I2C address with connector U7	Rev. B and Rev. C	Rev. D and later
E-00005: DDR4 connector U6 signals D2_MCLK1P and D2_MCLK1N are reversed	Rev. B and Rev. C	Rev. B and later
E-00006: Clocks are not generated properly to PCIe slots	Rev. B and Rev. C	Rev. B and later
E-00007: CFG_TESTSEL_B cannot be driven low	Rev. B and Rev. C	Rev. B and later
E-00008: Only two 10 Gbit Ethernet copper ports can operate at a time	Rev. B and Rev. C	Rev. D and later
E-00009: DDR rate is limited to 1866 MT/s when a single DIMM is installed	Rev. B, Rev. C, and Rev. D	Rev. E and later
E-00010: SATA Gen3 speed (6 Gbit/s) is fully functional, but exhibits a high error rate	Rev. B, Rev. C, and Rev. D	Rev. E and later
E-00011: USB 3.0 SuperSpeed devices train only to USB 2.0 (high speed) mode	Rev. B, Rev. C, and Rev. D	Rev. E and later
E-00012: Certain USB 2.0 flash devices do not enumerate at USB port 1	Rev. B, Rev. C, and Rev. D	Rev. D and later

Table continues on the next page...

Table 2. LS2085A/LS2088ARDB errata summary (continued)

Erratum	Found on board revisions	Fixed on board revisions
E-00013: I2C1 and I2C3 buses are missing pull-up	Rev. B, Rev. C, and Rev. D	Rev. E and later
E-00014: Unable to boot from SDHC port due to SDHC voltage/ speed limitation	All revisions	No fix is planned
E-00015: Main clocking source frequency out of tolerance	Rev. B, Rev. C, Rev. D, and Rev. E	Rev. F and later
E-00016: Unable to access AQR405 through EMI2 bus (MDC/ MDIO)	Rev. E	Rev. E and later
E-00017: CPU rotation error detect circuit not functional	All revisions	No fix is planned
E-00018: PCIe Gen3 is not working on PCIe x8 and x4 ports of LS2088ARDB	All revisions	No fix is planned

E-00001: JTAG voltage translator U37 is not required

Description

The U37 voltage translator impacts the signal integrity of the JTAG bus.

Impact

The CodeWarrior TAP device does not work with the U37 voltage translator installed on the board.

Workaround

Remove the U37 voltage regulator and R309 resistor and solder the wires as listed below.

- R310 pin 1 to R309 pin 1
- U37 pin 2 to U37 pin 13
- U37 pin 3 to U37 pin 12
- U37 pin 4 to U37 pin 11
- U37 pin 5 to U37 pin 10

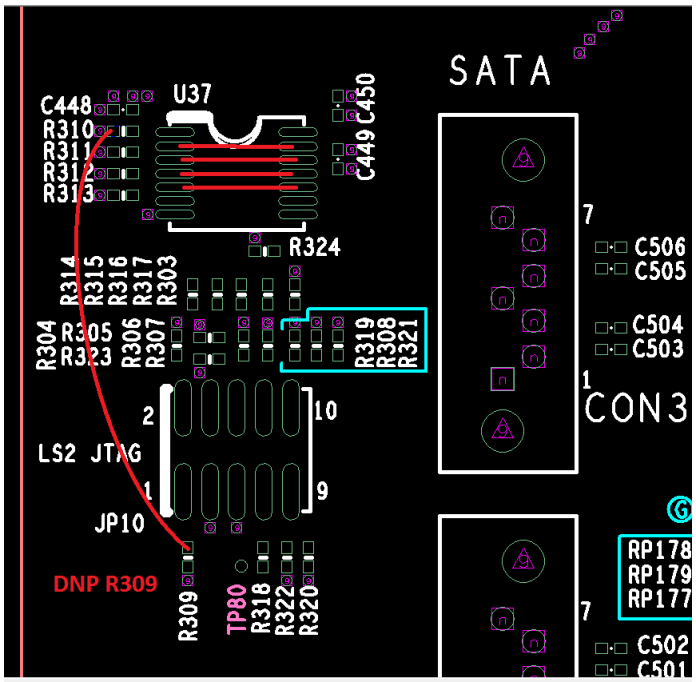

Figure 1. E-00001 workaround

Fix plan

The above mentioned rework has been implemented on all Rev B boards. The permanent fix will be available on Rev. C boards.

E-00002: COM1 (UART 1/3) port is not working

Description

The bottom port UART 1/3 is not working. It is wired incorrectly.

Impact

User cannot use the bottom port, UART 1/3.

Workaround

Use the UART 2/4 top port.

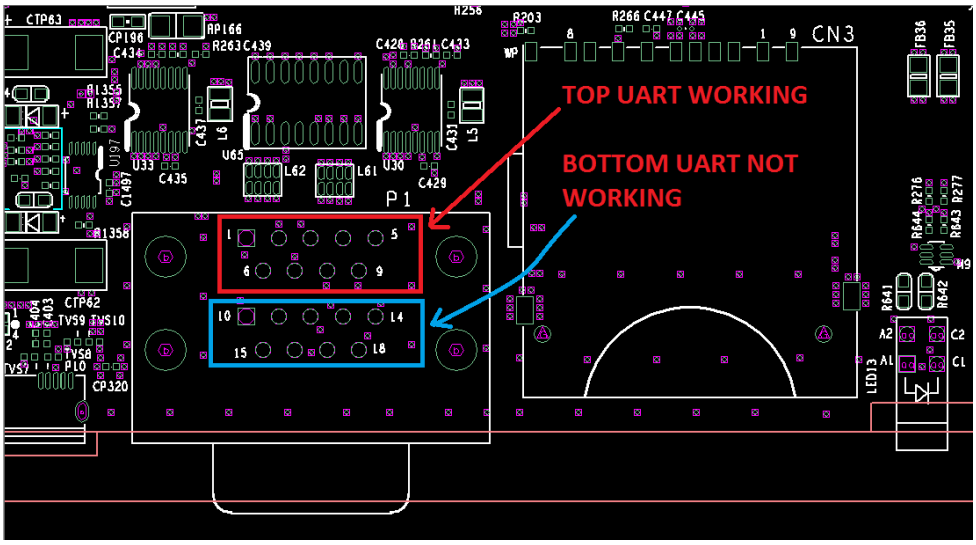

Figure 2. E-00002 workaround

Fix plan

The issue will be fixed on Rev. C boards.

E-00003: CPLD requires 1.8 V standby power for programming

Description

The CPLD requires both 3.3 V and 1.8 V standby voltages for the CPLD programming to work. The 1.8 V power supplied to CPLD on Rev. B board is not on standby.

Impact

Impacts the Rev A. boards. The Rev B boards works when a non standby 1.8 V power is supplied through the OVDD regulator.

Workaround

Use the OVDD regulator to supply the 1.8 V power on the Rev B boards.

Fix plan

The issue will be fixed on Rev. C boards with a regulator supplying 1.8 V power on standby to the CPLD.

E-00004: DDR4 connector U6 has a conflicting I^2C address with connector U7

Description

Both DDR4 connectors U6 and U7 have same I^2C address (0x54).

Impact

Only one DIMM slot can be used for the DDR controller 2. It impacts Rev. B and Rev. C boards.

Workaround

Use only one DIMM slot for the DDR controller 2. You can install the DDR4 DIMM either on slot U6 or slot U7. The preferred slot is U6.

Fix plan

The issue will be fixed on Rev. D boards.

E-00005: DDR4 connector U6 signals D2_MCLK1P and D2_MCLK1N are reversed

Description

The D2_MCLK1P and D2_MCLK1N signals are mistakenly reversed in the schematic and in the layout.

Impact

The DDR controller 2 will not work. The errata impacts Rev. B and Rev. C boards.

Workaround

Remove the R93 and R94 resistors and solder jumpers as listed below.

- R93 Pin1 to R94 Pin2 (need posted insulating tape)
- R94 Pin1 to R93 Pin2

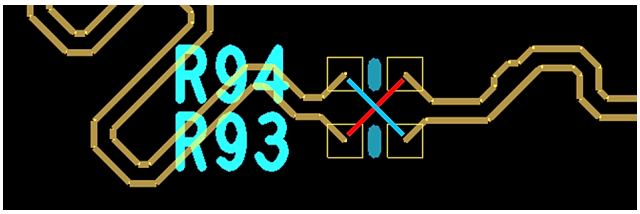

Figure 3. E-00005 workaround

Fix plan

All Rev B and Rev C boards will have this rework implemented before shipping. Therefore, no visible impact to the end user. The permanent fix will be implemented on Rev. D boards.

E-00006: Clocks are not generated properly to PCIe slots

Description

The 100 MHz clocks are not generated properly to the PCIe slots.

Impact

The x8 and x4 PCIe slots are not operational.

Workaround

Remove the R399 and R394 resistors.

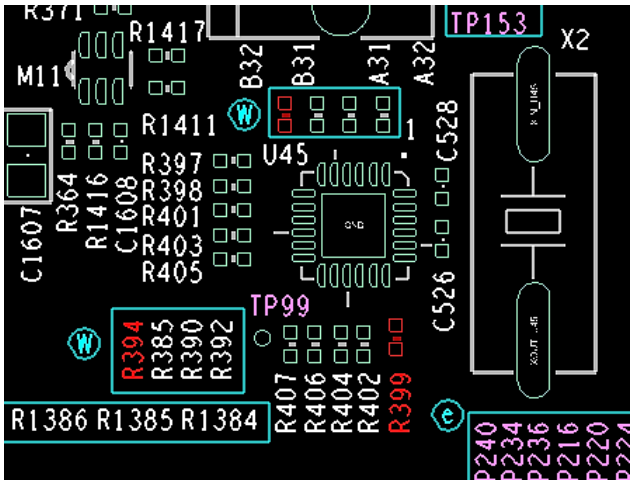

Figure 4. E-00006 workaround

Fix plan

All Rev. B and Rev. C boards will have this fix implemented before shipping. Therefore, no visible impact to the end user. The permanent fix will be implemented on Rev. D boards.

E-00007: CFG_TESTSEL_B cannot be driven low

Description

CFG_TESTSEL_B has both, a weak pulldown and a stronger pull-up. The SW8[5] switch cannot affect the TESTSEL level.

Impact

The alternate LS2085A/LS2088A personalities cannot be selected.

Workaround

Rev. B/C: Remove the R271 resistor from the bottom of the board as shown in the image below.

Rev. D and later: Use CPLD v1.18 or later. The R271 resistor does not need to be removed.

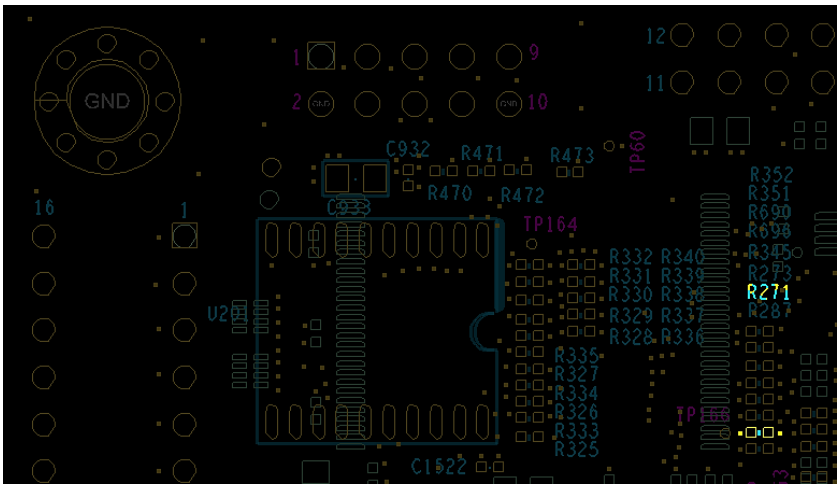

Figure 5. E-00007 workaround

Fix plan

Rev. B/C: Remove the R271 resistor from the bottom of the board as shown in the image above.

Rev. D and later: Use CPLD v1.18 or later. The R271 resistor does not need to be removed.

E-00008: Only two 10 Gbit Ethernet copper ports can operate at a time

Description

The power supply to the Aquantia 10 Gbit Ethernet PHY is inadequate on Rev. B and Rev. C boards. As a result, only two 10 Gbit Ethernet copper ports can be enabled at a time instead of all four copper ports.

NOTE

This two port restriction only applies to the 10 Gbit Ethernet copper ports and does not apply to the 10 Gbit Ethernet optical ports.

Impact

Any two 10 Gbit Ethernet copper ports can be used or enabled under this restriction. The LS2085A/LS2088ARDB software enables the ETH0 (DPNI7) and the ETH2 (DPNI9) copper ports by default.

Workaround

No viable workaround to enable all four Ethernet ports. User is restricted to use only two 10 Gbit copper ports at a time. Currently, the software enables the ETH0 (DPNI7) and ETH2 (DPNI9) ports by default.

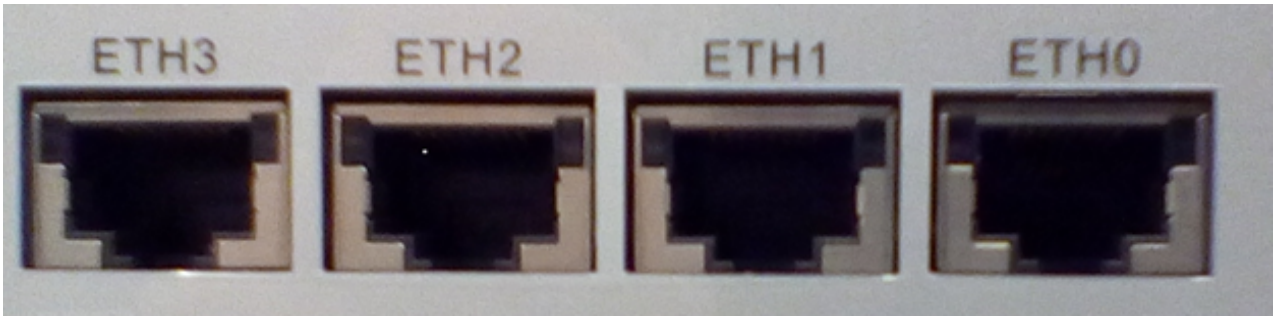

Figure 6. E-00008 workaround

Fix plan

The power supply is fixed on Rev. D and later boards. Therefore, all four 10 Gbit Ethernet copper ports can be used on Rev. D and later boards with no port restrictions.

E-00009: DDR rate is limited to 1866 MT/s when a single DIMM is installed

Description

The DDR only operates at a 1866 MT/s maximum rate when a single DIMM is installed (for each controller). Rev. C and earlier boards do not support two DIMMs per controller due to the erratum E-00004.

Impact

For Rev. C boards and earlier: For each DDR controller, the maximum DDR rate is 1866 MT/s when one DIMM is installed.

For Rev. D boards: for each DDR controller, the maximum DDR rate is 1866 MT/s when either one or two DIMMs per controller are installed.

For Rev. E boards and later: for each DDR controller, the maximum DDR rate is 2133 MT/s when one DIMM is installed. When configured with two DIMMs (per controller), DDR rate on Rev. E and later boards is 1866 MT/s.

Workaround

For Rev. C and earlier boards: No workaround. The boards are limited to work on one DIMM per controller at a maximum rate of 1866 MHz.

For Rev. D boards: No workaround. Either one or two DIMMs per controller is supported; DDR rate is 1866 MT/s.

For Rev. E and later boards: Two DIMMs per controller is supported; DDR rate is 1866 MT/s. One DIMM per controller is supported; DDR rate is 2133 MT/s.

NOTE

On Rev. E and later boards, U4 location is swapped with U5 location. Similarly, U6 location is swapped with U7 location. The figure below shows the swapped locations.

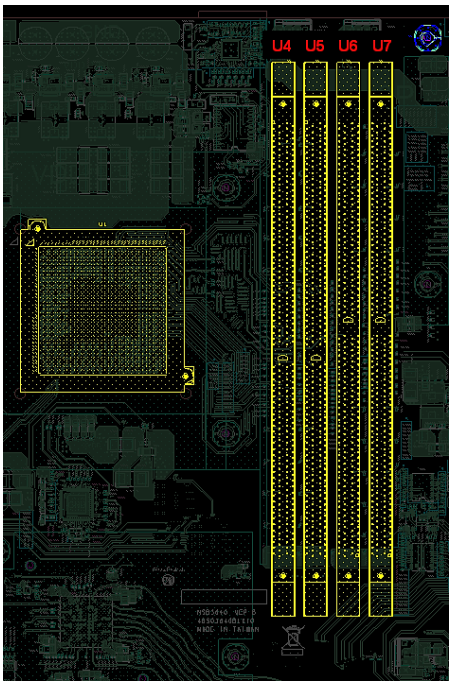

Figure 7. E-00009 workaround

Fix plan

On Rev. E boards, DDR operation at 2133 MT/s requires the removal of DIMM at U5 (for DDR controller 1) and U7 (for DDR controller 2). The DDR DIMMs are relocated and rewired on Rev. E and later boards to provide optimal DIMM location signaling. The Figure below shows the changes in the DDR DIMM locations for Rev. E and later boards. Basically, U4 – U7 have been repositioned to provide optimal signal integrity when only one DIMM is installed. When installing one DIMM per controller to achieve 2133 MT/s speed, the DIMM should be installed at location U4 (for DDR controller 1), and at U6 (for DDR controller 2).

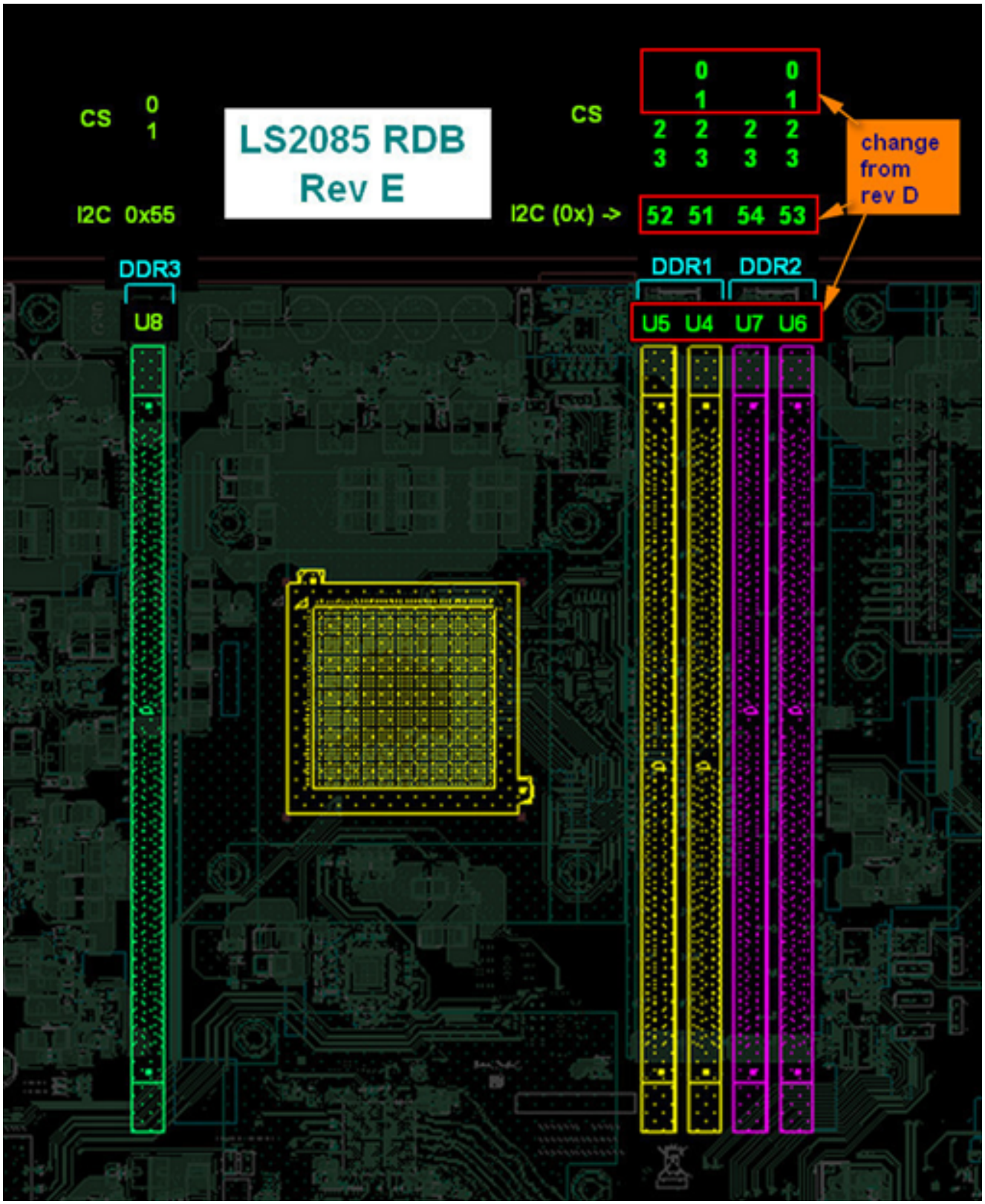

Figure 8. Rev. E and later boards: DDR DIMMs

E-00010: SATA Gen3 speed (6 Gbit/s) is fully functional, but exhibits a high error rate

Description

The SATA ports (COM2 and COM3) are fully functional at the Gen 1/2/3 speeds. Both SATA ports exhibit high read data error rate when a SATA Gen3 compatible drive is installed and runs at a 6 Gbit/s rate. However, the error rate is within the SATA specifications. The solid-state type hard drives are much more susceptible to errors.

Impact

The read data errors at 6 Gbit/s causes system software to perform retries for the read data operations.

Workaround

None required. If performance needs to be optimized at a Gen3 speed, then it is important to implement all SoC errata related to the SATA and/or SerDes operation. Contact your local NXP field applications engineer (FAE) or sales representative to get the complete list of LS2085A/LS2088A SoC errata.

Alternatively, you can program the SATA control register and SPD field to limit the interface negotiation to the Gen2 speed as the highest allowed speed.

Fix plan

Implement all SoC Errata related to the SATA and/or SerDes operation(s) to optimize the performance. Rev. E and later boards will have the hardware channel modifications to improve the error rate for the Gen3 speed.

E-00011: USB 3.0 SuperSpeed devices train only to USB 2.0 (high speed) mode

Description

On both USB ports, the USB 3.0 devices (SuperSpeed devices) detects in a USB 2.0 (high speed) mode. SuperSpeed = 5 Gbit/s, high speed = 480 Mbit/s. The ESD protection devices (AZ4012-01F) have excessive loading capacitance (40-50 pF).

Impact

The USB 3.0 devices will not train at the SuperSpeed mode (5 Gbit/s) and fall back to 480 Mbit/s.

Workaround

Remove the ESD protection devices, TVS2 to TVS5 and TVS7 to TVS10. This solution is required for Rev. C and earlier boards. No change is required on Rev. D boards as these ESD protection devices have already been removed from the board during the assembly process before shipping.

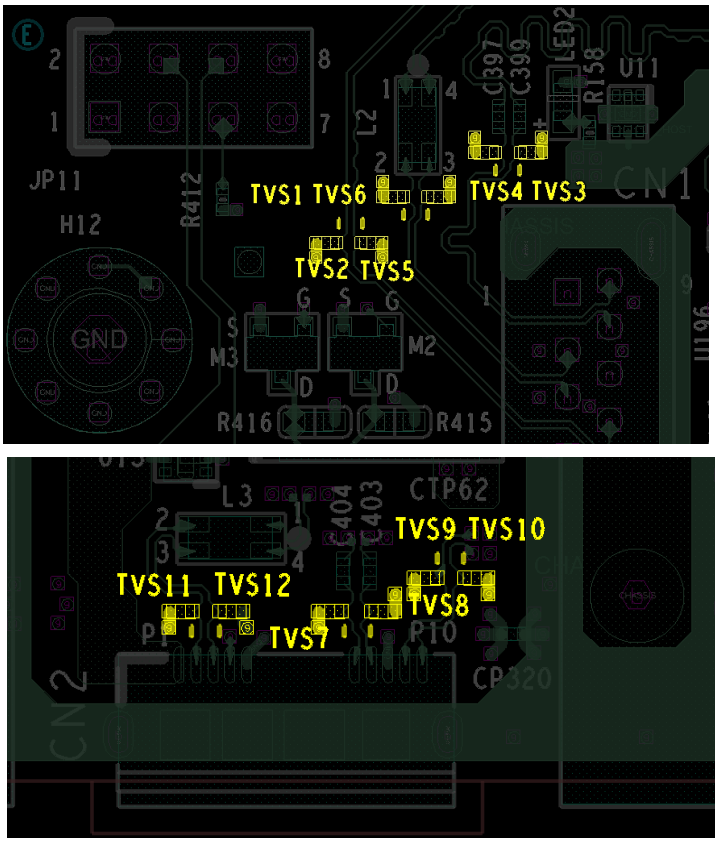

Figure 9. E-00011 workaround

Fix plan

For Rev. C and earlier boards, remove the ESD protection devices, TVS2 to TVS5 and TVS7 to TVS10. For Rev. D boards, these ESD protection devices have already been removed. The permanent fix will be implemented on Rev. E and later boards as listed below.

- Replace all ESD protection diodes TVS1 to TVS13 on the USB interface, with the lower load capacitance diodes (0.2 pF).

Rev. E and later boards have NXP PUSB3FR6Z ESD protection diodes at location U22 and U37 as shown in below figure:

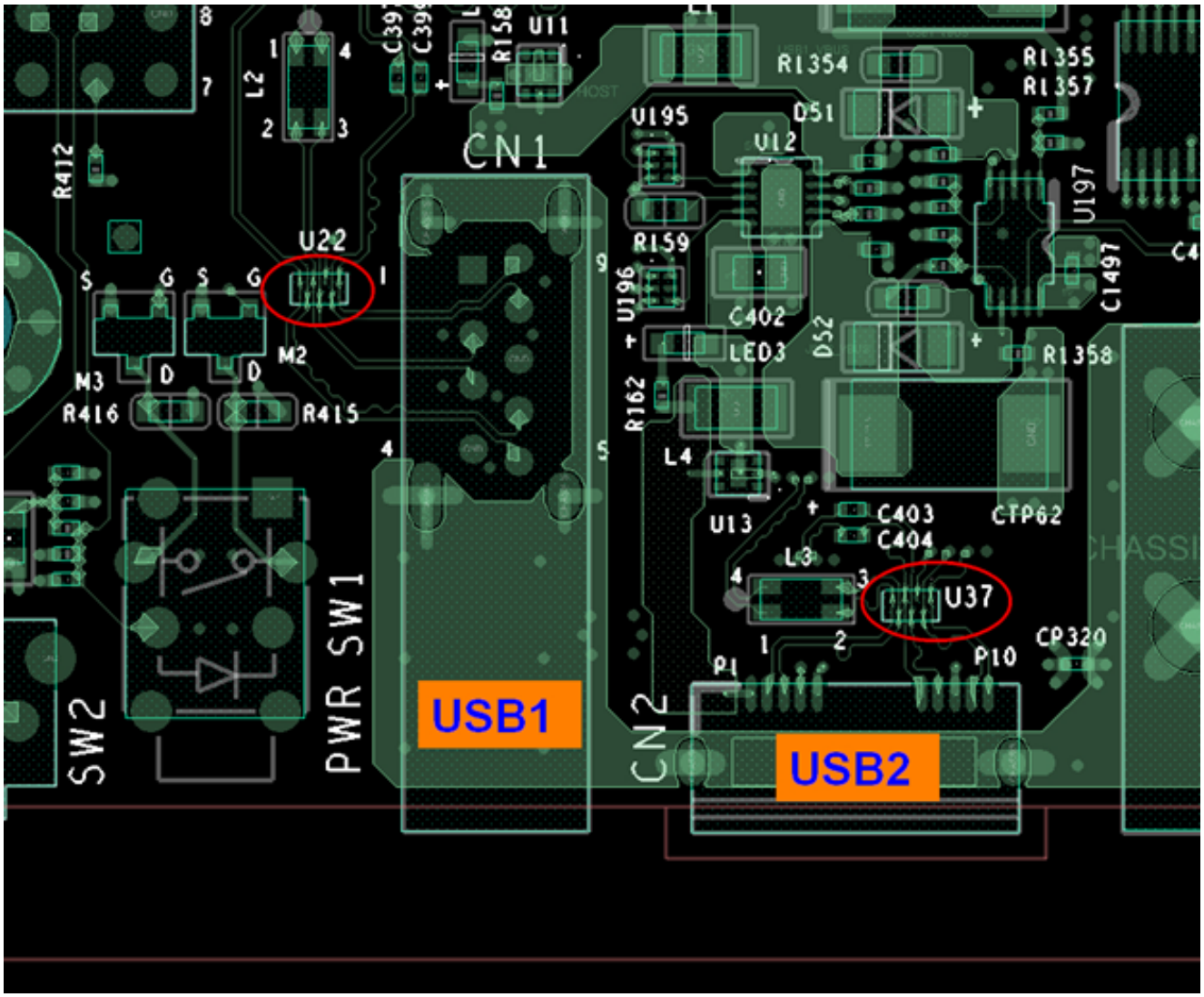

Figure 10. LS2085A/LS2088ARDB Rev. E and later boards: USB protection diodes

E-00012: Certain USB 2.0 flash devices do not enumerate at USB port 1

Description

Rev. D and earlier boards: On USB port 1, certain USB 2.0 flash devices (HP) do not enumerate properly. Uboot software reports that no device has found on USB Port 1.

Impact

Certain USB 2.0 flash devices do not enumerate properly. Flash device is not recognized by the system.

Workaround

Replace USB connector at USB Port 1 (CN1) with higher quality connector, such as Molex part number 48404-0003.

Fix plan

Replace USB connector at USB Port 1 (CN1) with higher quality connector, such as Molex part number 48404-0003.

E-00013: I2C1 and I2C3 buses are missing pull-up

Description

Rev. D and earlier boards: The pull-ups for I2C1 and I2C3 do not populate (DNP) between the LS2 device and the PCA954x device on the board.

Impact

When the PCA954x device is tri-stated, the I2C bus will float. This makes the I2C bus and its associated downstream devices inaccessible.

Workaround

Two potential workarounds are as follows:

- Hardware fix - Populate resistors R189 and R190 for I2C1 and resistors R228 and R229 for I2C3.
- Software fix - Remove the tri-state option from the PCA954x driver. These patches have been successfully proven by NXP.

NOTE

The software patches are not up-streamable for Linux.

Fix plan

Long term fix - Populate resistors R189, R190, R228, and R229. These resistors are populated in Rev. E and later boards.

E-00014: Unable to boot from SDHC port due to SDHC voltage/speed limitation

Description

Boot from the SDHC interface is not supported. Smart Voltage Translator (U36) requires special control signals such as CMD_DIR, DATA_DIR from the LS2085A/LS2088A device to function. These signals cannot be enabled from the LS2085A/LS2088A device during boot time, therefore, the SDHC interface cannot be used during the boot time.

On some Rev. F boards, U36 is removed from the board. The voltage translators U205 and U208 provide required voltage translation to support Uboot and Legacy SDHC at 3.3 V only (1.8 V IO at SD Card is not supported).

Impact

Boot from SD is not supported. The SDHC interface is useable only after booting.

Since, some revision boards do not support 1.8 V translation, software has been updated so that it supports only Legacy SDHC 3.3 V modes. Although, the LS2080A/LS2088A device is capable of supporting the SD modes as listed below, the LS2085A/LS2088ARDB is limited to DS and HS modes only.

- DS - Default speed up to 25 MHz 3.3 V signaling
- HS - High speed up to 50 MHz 3.3 V signaling
- SDR12 - SDR up to 25 MHz 1.8 V signaling
- SDR25 - SDR up to 50 MHz 1.8 V signaling
- SDR50 - SDR up to 100 MHz 1.8 V signaling
- SDR104 - SDR up to 208 MHz 1.8 V signaling
- DDR50 - DDR up to 50 MHz 1.8 V signaling

Workaround

None.

Fix plan

No fix is planned.

E-00015: Main clocking source frequency out of tolerance

Description

Board layout issue has excessive capacitance on crystal X1 pin 3 (net XB_Si5341B). Due to excess capacitance, the frequency tolerance of all clock outputs from U44 is slightly out of specification (too slow at approx. -100 ppm).

Impact

Ethernet traffic may exhibit some bit errors on some boards.

Workaround

Cut three traces as shown in the figure below and add a wire from U44 pin 9 to crystal X1 pin 3.

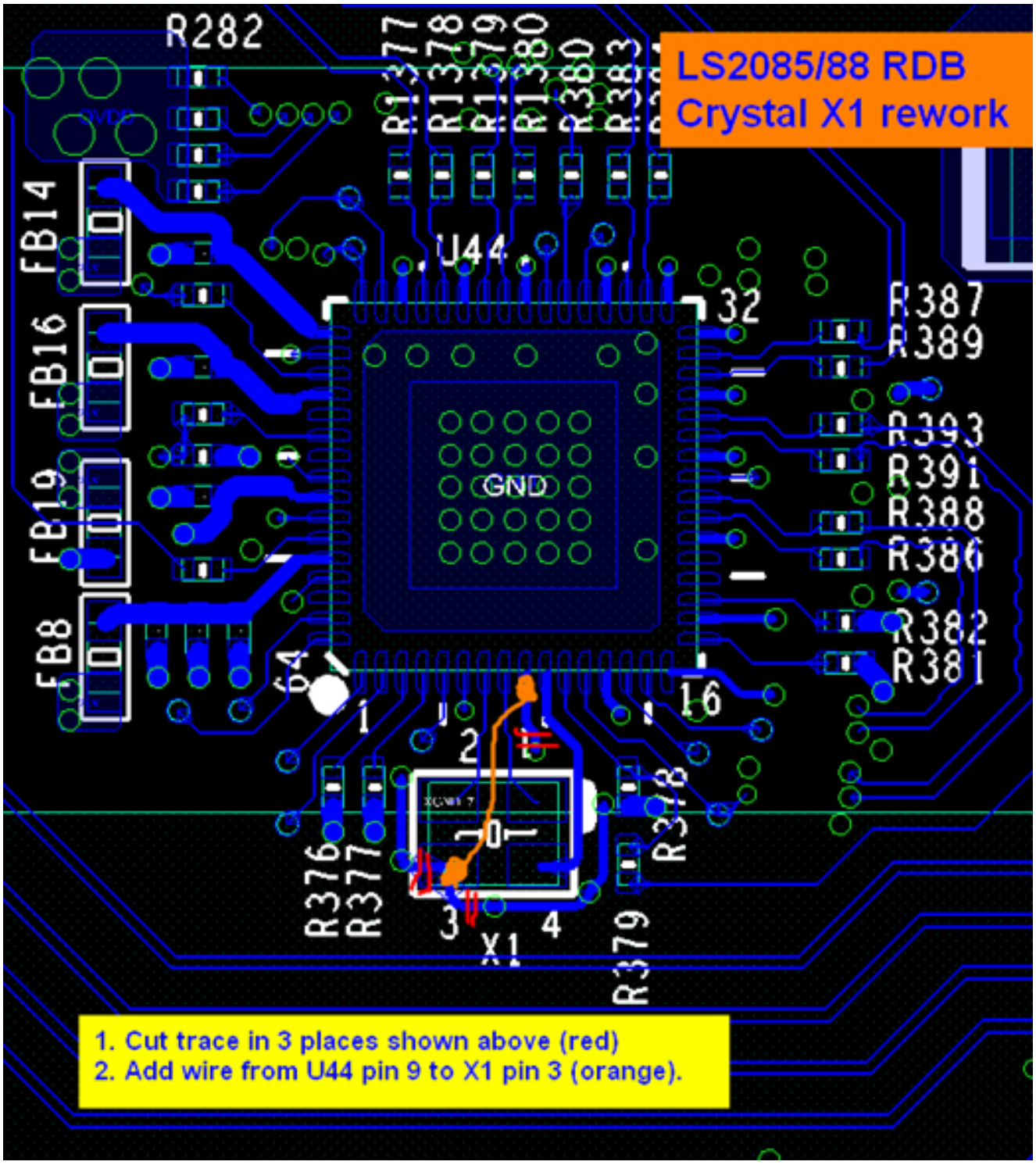

Figure 11. E-00015 workaround

Fix plan

Rev. F and later boards have correct layout to remove excess capacitance. No other correction is required.

E-00016: Unable to access AQR405 through EMI2 bus (MDC/MDIO)

Description

Rev. E boards only: The voltage signaling interface on the EMI2 (MDC/MDIO) bus has been changed from 1.2 V to 2.5 V on Rev. E boards. This change was requested by Aquantia for the AQR405 device. The change to 2.5 V levels requires flipping the voltage translator U28 backwards, which is not done in Rev. E board. The U28 voltage translator does not not work with the new 2.5 V levels unless it is reversed.

Impact

Software cannot access and configure the AQR405 (10GBase-T) PHY over the EMI2 bus, unless board is reworked to reverse U28.

Workaround

Remove U28 from the PCB pads and re-wire as described below:

LS2085A/LS2088ARDB Rev. E modification for AQR405 EMI2 (MDC and MDIO) connection:

Remove U28 and flip chip and re-wire the pins as shown in the figures below. This is required because VL must be equal to or lower than VCC.

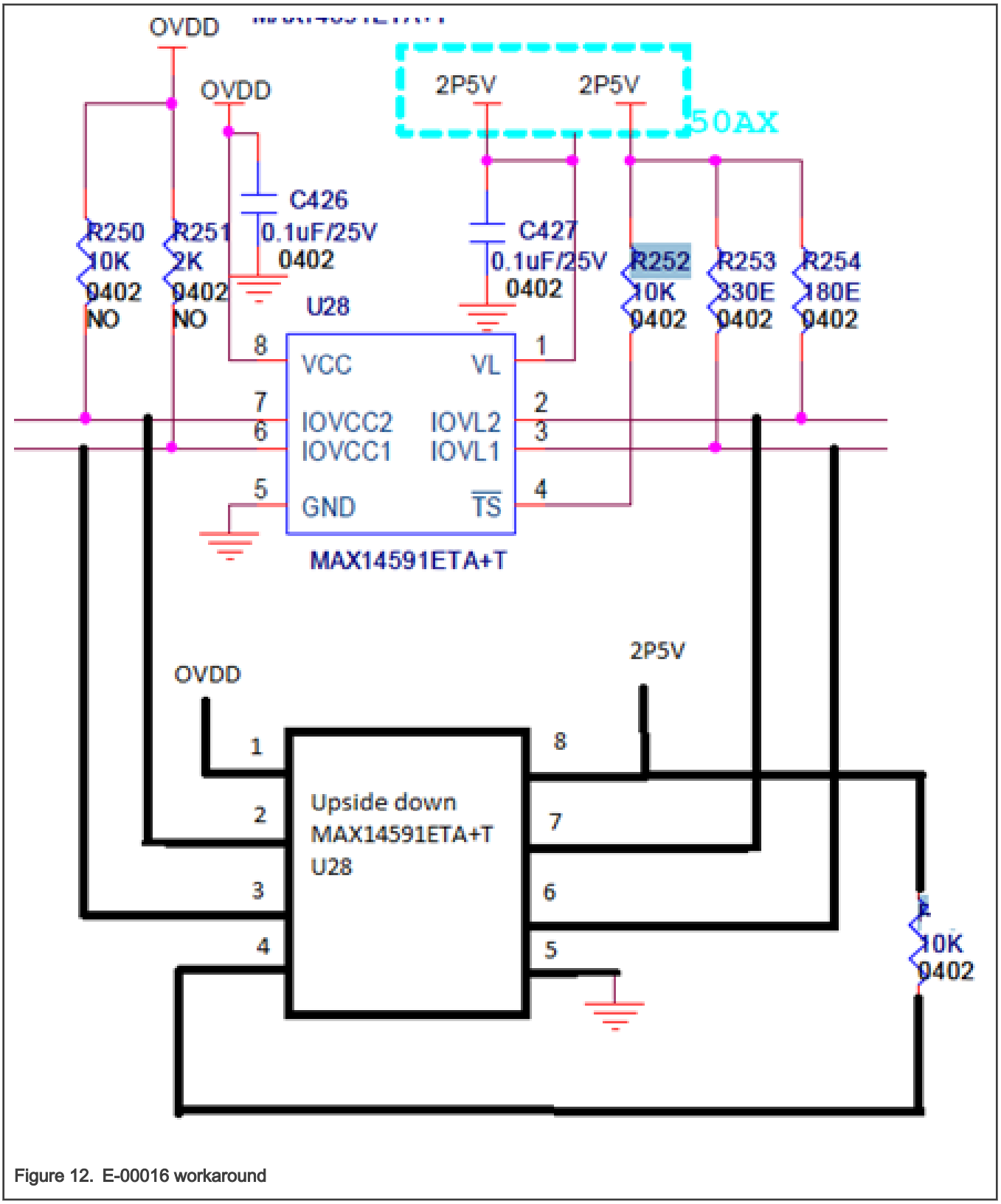

Figure 12. E-00016 workaround

Adding a 10K ohm resistor to pin 4 makes the connection simple. The white material under the chip is double-sided tape to keep the chip in place.

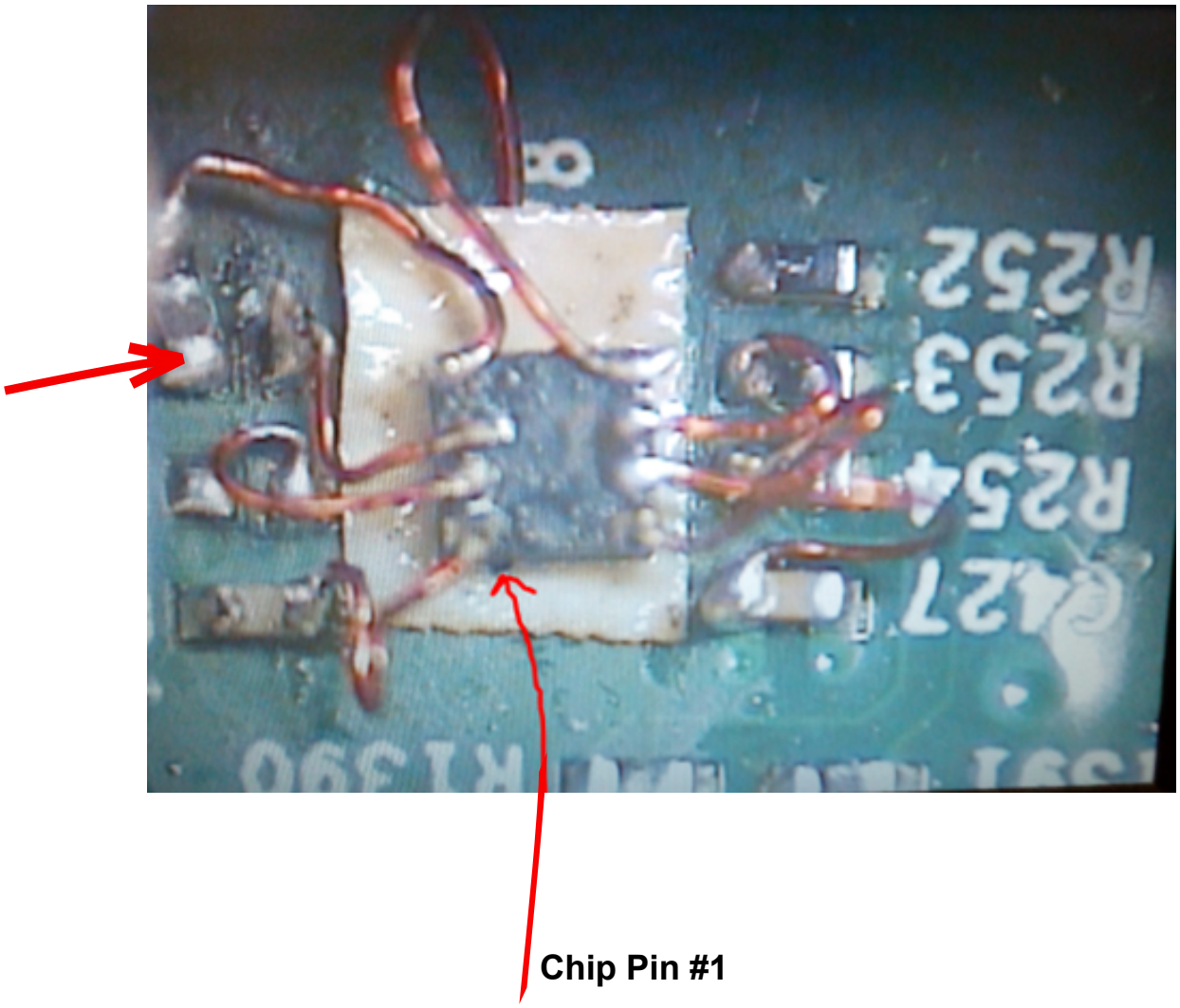

Figure 13. E-00016 workaround

Fix plan

Rev. F and later boards have U28 wired as shown in the diagram above. No other correction is required.

E-00017: CPU rotation error detect circuit not functional

Description

The CPU rotation error detection circuit does not signal an error when the CPU is disoriented in the CPU socket.

Impact

If the CPU is inserted incorrectly into the CPU socket, the ROT_ERR LED does not illuminate, and the board is allowed to power on. Powering up the CPU while it is misaligned in the socket can cause damage to the CPU device, socket, and PCB.

Workaround

None.

Fix plan

No fix is planned for this platform, since the CPU device has to be soldered down in Rev. F and later boards. However, this circuit needs to be corrected in future platforms with the following solution:

An NC pin (with pull-up) is used to sense the CPU orientation, and the GND/Power pins are located in the other three device pinout quadrants in such a manner that a disoriented CPU will effectively ground the rotation error signal.

E-00018: PCIe Gen3 is not working on PCIe x8 and x4 ports of LS2088ARDB

Description

Due to signal integrity issues on the LS2088ARDB circuit board, the PCIe link may frequently experience (depending on what type of endpoint card is plugged in) the correctable receiver error, which causes Linux kernel to cycle between normal operation and recovery operation when running either PCIe x8 or PCIe x4 port at Gen3 speed (8 GHz). The issue has been confirmed in IBIS simulations performed by NXP. The simulation results showed that the eye diagram was not sufficiently open for correct Gen3 operation. PCIe Gen2 (5 GHz) and Gen1 (2.5 GHz) speeds work fine. This is a board-level issue, not a silicon issue, as confirmed during silicon validation. No customer has reported such an issue on their own boards.

Impact

This reduces the performance on the PCIe link and a flood of correctable errors may be reported by the Linux kernel, potentially crashing it.

Workaround

Use one of the following workarounds:

- Operate at Gen2 speed
- Suppress error reporting to kernel to prevent the recoverable error from crashing the kernel. The error recoveries will still take place. Use one of the following methods to suppress error reporting:
  - Set the RXEM Receiver Error Mask bit of PCI Express Correctable Error Mask Register (offset 114h) to 1. This will prevent the error from being reported to the kernel.
  - Compile the kernel without Advanced Error Reporting (AER). This error (and others) will not be reported.

Fix plan

No fix is planned.

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