NXP Semiconductors
Application Note

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MPC5746R Hardware Design Guide

by: NXP Semiconductors

1 Introduction

MPC5746R is a multi-core 32-bit microcontroller intended for automotive powertrain applications. It is based upon e200z4 Power® Architecture cores running at up to 200 MHz.

Throughout this application note, MPC5746R refers to the family of devices: MPC5743R, MPC5745R, and MPC5746R.

This application note details the options of MPC5746R power supplies and the correct external circuitry required for each supply, including digital, analog, and SRAM standby. It also discusses configuration options for clock, reset, and ADCs, as well as recommended debug and peripheral communication connections, and other major external hardware required for the device.

Please note that information from the MPC5746R Reference Manual, Data Sheet, and/or Errata report may be repeated in this application note for the convenience

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of the reader. The Reference Manual, Data Sheet and Errata report are the official specifications for MPC5746R and should be reviewed for the most up-to-date information available for this device.

2 MPC5746R Package Options Overview

The MPC5746R is available in four different package options; three of these are intended for production and one is intended to provide additional features to support debug and calibration.

Table 1. MPC5746R Package Options

Package	Target	Description
144 LQFP	Production	Provides access to the primary features of the device. Packages with additional pins provide additional features and/or additional GPIO. No Nexus High Speed Aurora Trace interface is provided on any production package, only JTAG.
176 LQFP		
252 MAPBGA		
292 MAPBGA	Development	Provides access to primary features of device, plus Nexus High Speed Aurora Trace and overlay/trace memory that can be used for calibration. This package is designed for debug and calibration development use and is typically provided mounted to an interposer/adapter system to connect to either a 144LQFP, 176 LQFP or 252 MAPBGA footprint. The Aurora debug interface connector is provided on this adapter board, eliminating the need for the customer to route the high speed Aurora differential pairs and allowing use on the customer PCB.

The package selection should be based on the number of input/output pins required for the application and the area available for the target system. The following table shows the sizes of different packages. See the MPC5746R Data Sheet for complete package dimensions and ball placement. Drawings are also available on the NXP web site; search for the case outline number shown in Table 2.

Table 2. Package Sizes

Package	Physical Size (mm)	Case Outline Number
144 LQFP	20 x 20	98ASS23177W
176 LQFP	24 x 24	98ASS23479W
252 MAPBGA	17 x 17	98ASA00468D
292 MAPBGA[1]	17 x 17	98ASA00261D

1 Only for development purpose and not intended for production.

3 Power Supply

MPC5746R provides several options for providing power supply voltages. The main power supplies required are 1.25 V, 5 V and 3.3 V depending on the requirements of the application. The on-chip flash memory supply is generated internally. The SRAM has a separate supply input for data retention features, if they are required.

In addition the MPC5746R microcontroller includes a robust power management infrastructure that enables applications to select among various user modes and to monitor internal voltages for high- and

low-voltage conditions. The monitoring capability is also used to ensure supply voltages and internal voltages are within the required ranges before the microcontroller can exit reset. The MPC5746R MCU supports three different input voltages:

- 1.25 V (required) for the internal logic. This supply may be provided externally or generated from either the 3.3 V or 5.0 V supply using an external NPN Bipolar Junction Transistor (BJT) ballast transistor and the internal 1.25 V regulator control.
- 5 V (required) for the Power Management controller, I/O, Debug, ADCs and external communication interfaces
- 3.3 V (optional) for I/O, Debug and external communication interfaces

The 3.3 V supply required for the flash memory is generated by an on-chip regulator. This regulator requires an external decoupling capacitor on VDD_HV_FLA.

3.1 Power Supply Signals and Pins

Table 3 lists all power domains with corresponding pin names.

Table 3. MCU Supply Pins

Domain Name	Supply Voltage[1]	Description
VDD_LV[2]	1.25 V	Core Logic Low Voltage Supply
VDD_HV_IO_MAIN	5.0 V	Main I/O Voltage Supply
VDD_HV_ADV_SAR	5.0 V	SAR ADC Voltage Supply
VDD_HV_ADR_SAR	5.0 V	SAR ADC Voltage Reference
VDD_HV_ADV_SD	5.0 V	Sigma-Delta ADC Voltage Supply
VDD_HV_ADR_SD	5.0 V	Sigma-Delta ADC Voltage Reference
VDD_HV_IO_JTAG	3.3 V or 5.0 V	Production Device JTAG I/O and External Oscillator Voltage Supply
VDD_HV_IO_FEC	3.3 V or 5.0 V	Ethernet I/O Supply
VDD_HV_IO_MSC	3.3 V or 5.0 V	Microsecond Channel I/O Supply
VDD_HV_PMC	5.0 V	Power Management Controller Supply
VDD_HV_FLA[3]	3.3 V	PMC Flash Regulator Bypass Capacitor
VDD_LV_BD[4]	1.25 V	Emulation Device Core Logic Low Voltage Supply
VDD_HV_IO_BD[4]	3.3 V or 5.0 V	Emulation Device Main I/O Voltage Supply
VDDSTBY[5]	1.3 V–5.9 V	Standby RAM Supply Input

1 Nominal voltage, see MPC5746R Data Sheet for actual voltage specifications.

2 This supply may be optionally provided by the on-chip regulator using a pass transistor. See Section 3.1.2

3 No connection to external supply required, but it does require a bypass capacitor.

4 Only present on the 292 MAPBGA emulation device.

5 Ramp rate must be less than 16.6 kV/s as per limitation for the 0N94H mask set. Refer to the latest MPC5746R Data Sheet for additional requirements.

Some of the supplies can be powered with different supply voltages. In particular, the MCU allows flexibility in the supply of voltages that power selected input and output pins. These supplies are “high” supplies and can be connected to either a nominal 3.3 V or 5.0 V supply. In addition we recommend keeping all supply slew rates below 25 V/ms.

Refer to the MPC5746R Data Sheet to learn what voltages can be connected to the power pins. Supply pins/balls differ from package to package. Please refer to section 3.1.1 for package differences.

The following table shows several power supply design schemes. The flexibility of the supply configurations provides the board designer several options for optimizing the design.

Table 4. Power supply schemes

Supply options	Reference
Single 5 V supply	Section 3.1.2
Multi supply with 5 V and 3.3 V	Section 3.1.3
Multi supply with 5 V and 1.25 V	Section 3.1.4

Please refer to the IO description attached to the MPC5746R Reference Manual for more details.

3.1.1 Power supply package differences

There are different numbers of balls/pins available for the power supplies in each of the MPC5746R package options. In addition, for some package options, some power supplies are not available. The table below shows, for each package, the number of balls available for the power supply input to the device. All supply balls that are available on the package should be connected to a supply voltage.

Table 5. Number of power supply balls/pins versus package

Supply Domain	Nominal Voltage	144LQFP	176LQFP	252BGA
VDD_LV[1]	1.25 V	6	6	14
VDD_HV_IO_MAIN	5.0 V	5	5	7
VDD_HV_ADV_SAR	5.0 V	1	1	2
VDD_HV_ADR_SAR	5.0 V	1	1	1
VDD_HV_ADV_SD	5.0 V	1	1	1
VDD_HV_ADR_SD	5.0 V	1	1	1
VDD_HV_IO_JTAG	3.3 V or 5.0 V	1	1	1
VDD_HV_IO_FEC	3.3 V or 5.0 V	1	1	1
VDD_HV_IO_MSC	3.3 V or 5.0 V	1	1	1
VDD_HV_PMC	5.0 V	1	1	1
VDD_HV_FLA[2]	3.3 V	1	1	1
VDD_LV_BD[3]	1.25 V	-	-	-

Table 5. Number of power supply balls/pins versus package

Supply Domain	Nominal Voltage	144LQFP	176LQFP	252BGA
VDD_HV_IO_BD[4]	3.3 V or 5.0 V	-	-	-
VDDSTBY[4]	1.3 V - 5.9 V	1	1	1

1 This supply may be optionally provided by the on-chip regulator using a pass transistor. See Section 3.1.2

2 Except bypass capacitor no connection to external supply required.

3 Only present on the 292 MAPBGA emulation device.

4 Ramp rate must be less than 16.6 kV/s as per limitation for the 0N94H mask set. Refer to the latest MPC5746R Data Sheet for additional requirements.

3.1.2 Single 5 V Supply

This topology uses a single 5 V supply for all I/O, with the internal regulator providing the 1.25 V for the VDD_LV core supply. Note that most Fast Ethernet Controller (FEC) physical layer interfaces require 3.3 V signals, so the FEC would not normally be operational in this configuration.

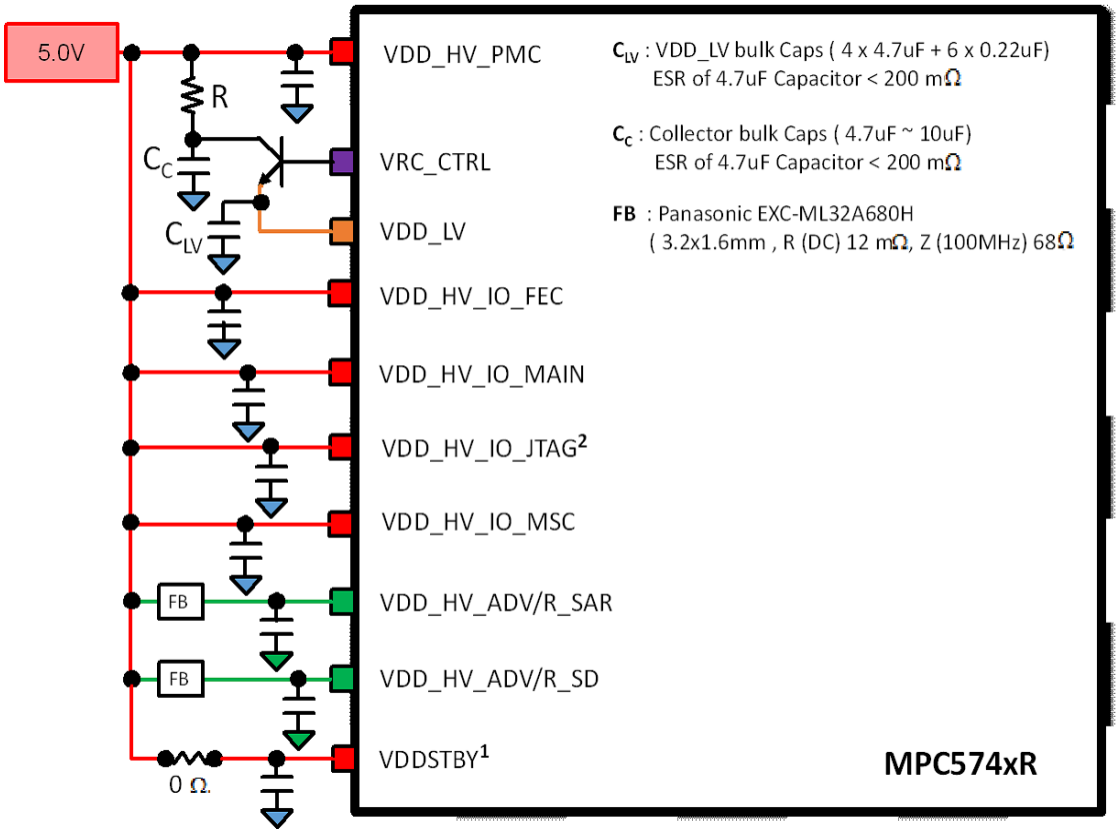


Figure 1. Single 5 V Supply (no Ethernet)

1 VDDSTBY may need to be powered by a separate supply in the case where the standby SRAM data retention feature is required. This figure is intended to illustrate that a single 5 V supply may be used where appropriate for the design.

2 VDD_HV_IO_JTAG is typically powered by a 3.3 V supply for compatibility with many debug tools. However if tools support 5 V or JTAG access is not required, a 5 V supply may be used and the JTAG pins can be used as normal GPIO.

3.1.3 Multi Supply - 5 V and 3.3 V

In this configuration there are dual supply voltages, 5 V and 3.3 V. The 5 V supply provides the I/O supply, the internal regulator provides the 1.25 V core supply and the 3.3 V supply is used to power the FEC subnet.

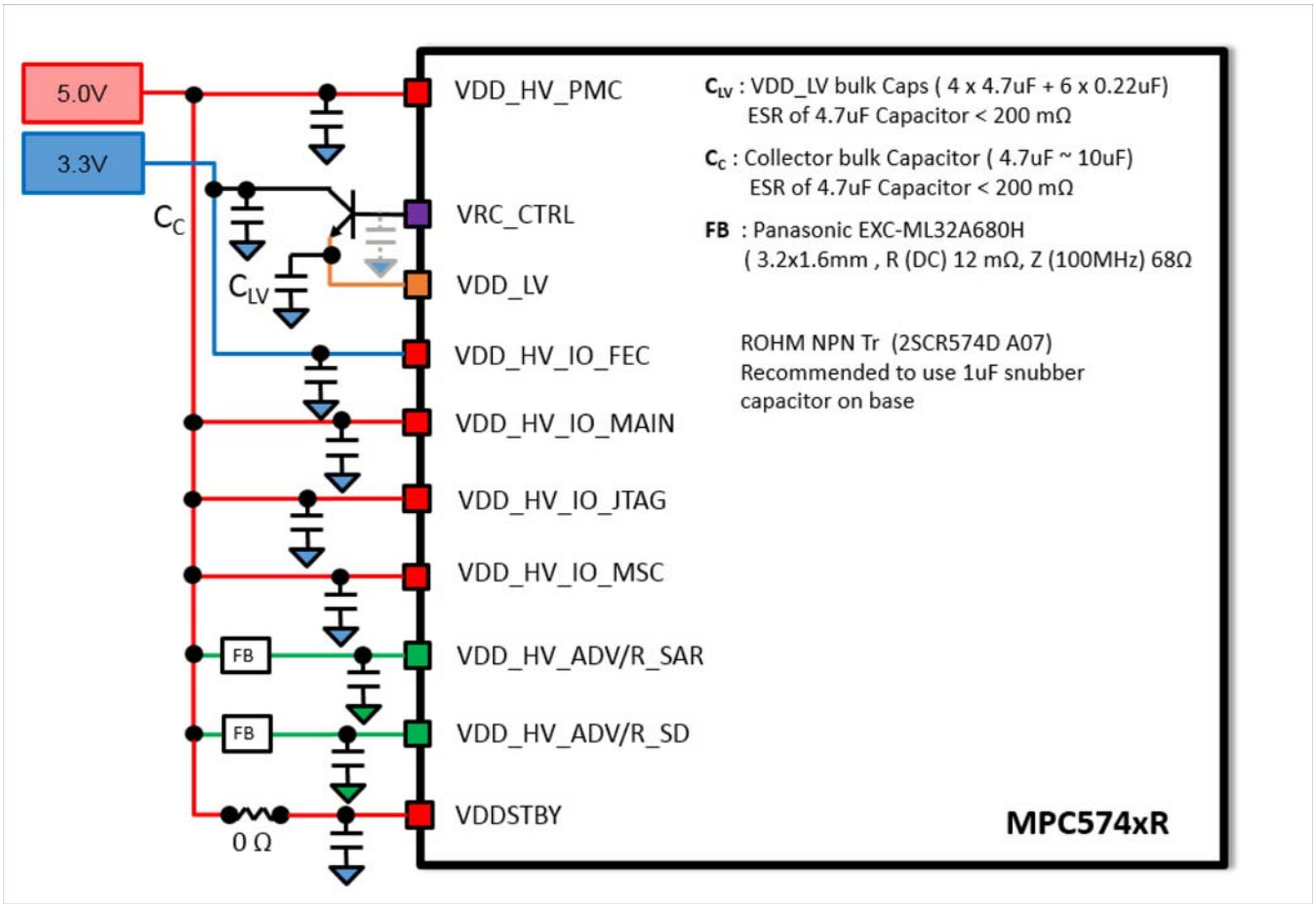


Figure 2. Multi Supply, 5 V and 3.3 V with Ethernet

NOTE

VDD_HV_IO_JTAG and/or VDD_HV_IO_MSC could also be powered by 3.3 V.

3.1.4 Multi Supply: 5.0 V and 1.25 V

In this configuration there are dual supply voltages, 5 V and 1.25 V. I/O is powered by the 5 V supply and the core voltage is powered by the 1.25 V supply. Note that most Fast Ethernet Controller (FEC) physical layer interfaces require 3.3 V signals, so the FEC would not normally be operational in this configuration.

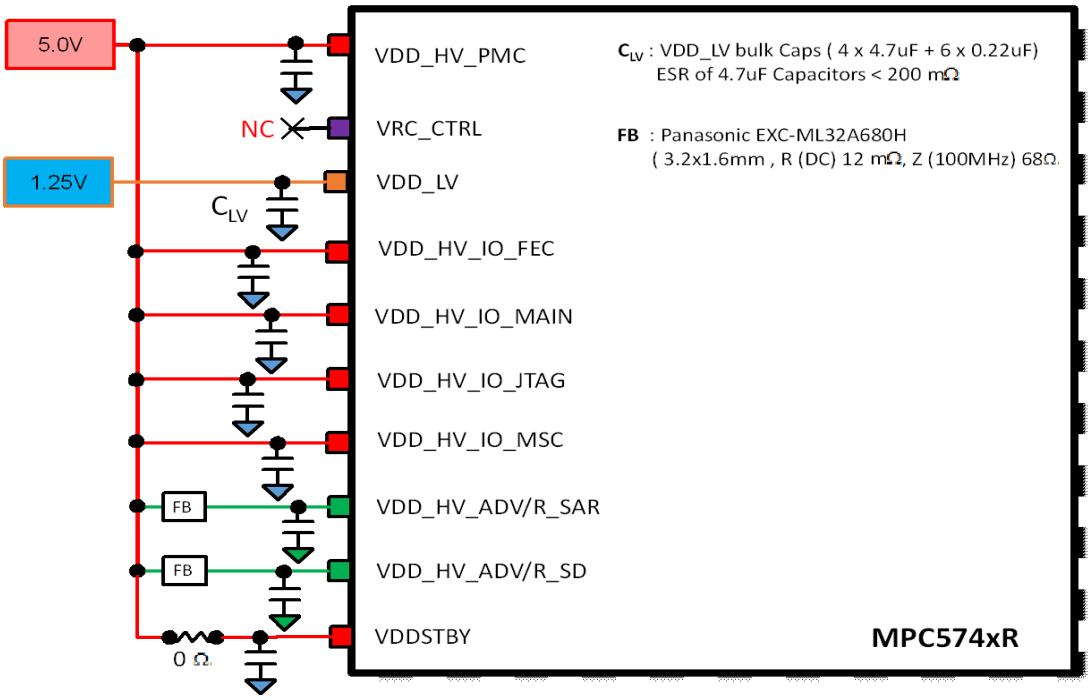


Figure 3. Multi Supply, 5 V and 1.25 V without Ethernet

3.1.5 Decoupling Capacitor Recommendation for supply domains

Table 6 shows all power domains and the suggested decoupling and/or filter capacitors for their corresponding pins. These values are provided as a guideline and will vary depending on the application and capability of the power supplies used.

Table 6. Supply Decoupling Requirements

Domain	Supply Voltage	Bulk	Bypass (each pin)
VDD_LV[1]	1.25 V	4.7 µF[2]	220nF ~ 47 nF
VDD_HV_IO_MAIN	5.0 V	4.7 uF[3]	100nF ~ 10 nF
VDD_HV_ADV_SAR	5.0 V	10 µF	220nF ~ 100 nF
VDD_HV_ADR_SAR	5.0 V	–	220nF ~ 100 nF
VDD_HV_ADV_SD	5.0 V	4.7 µF	220nF ~ 100 nF
VDD_HV_ADR_SD	5.0 V	–	220nF ~ 100 nF
VDD_HV_IO_JTAG	3.3 V or 5.0 V	4.7 µF	220nF ~ 100 nF
VDD_HV_IO_FEC	5.0 V or 3.3 V	4.7 µF	220nF ~ 100 nF
VDD_HV_IO_MSC	5.0 V or 3.3 V	4.7 µF	220nF ~ 100 nF
VDD_HV_PMC	5.0 V	4.7 µF	220nF ~ 47 nF

Table 6. Supply Decoupling Requirements

Domain	Supply Voltage	Bulk	Bypass (each pin)
VDD_HV_FLA[4]	3.3 V	1 µF~2.2 µF	1 nF
VDD_LV_BD[5]	1.25 V	4.7 µF	100 nF
VDD_HV_IO_BD[5]	5.0 V	4.7 µF	100 nF
VDDSTBY	1.3 V–5.9 V	1 µF	100 nF

1 This supply may be optionally provided by the on-chip regulator using a bipolar junction transistor (BJT). See Section 3.1.2.

2 Recommend 4 x 4.7 uF bulk capacitors with lower ESR (each < 200 mΩ) for VDD_LV supply domain.

3 Recommend 5 x 4.7 uF bulk capacitors for VDD_HV_IO_MAIN supply domain.

4 No connection to external supply required.

5 Only present on the 292 MAPBGA emulation device.

3.2 On-chip 1.25 V Regulator

In order to lower system cost, MPC5746R provides an on-chip regulator that can use an external NPN pass transistor to provide the 1.25 V core supply voltage from either a 5.0 V or 3.3 V supply. The recommended external circuits are shown in Figure 4.

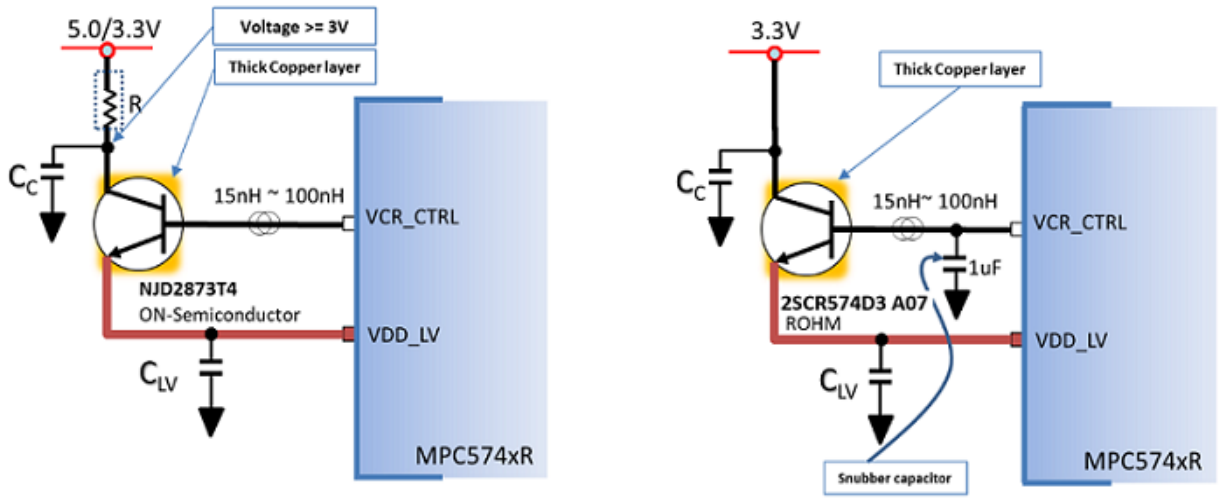


Figure 4. 1.25 V Supply with external pass Transistor

When the 5.0 V supply configuration is in use, the internal regulator regulates the BJT emitter voltage to 1.25[V], which is used as the core supply (VDD_LV). The remaining energy needs to be dissipated via the transistor as heat. The capability of the transistor package to dissipate heat degrades as the temperature increases. To overcome such problems, the user should analyze the thermal capabilities of the transistor and add sufficient heat dissipation options as needed.

There are several options available: 1) use a heat sink 2) populate a copper layer(s) beneath the transistor with thermal VIAS to improve the heat dissipation. NXP recommends consulting the transistor vendor to obtain optimal thermal design.

As another option, an external resistor can be used to minimize the extra heat. The resistor will drop the collector voltage to mitigate the heat dissipation of the pass transistor (BJT). In this case, the collector voltage needs to be maintained at 3 V or above.

NXP recommends a low inductance between the transistor base and the VRC_CTRL pin/pad. This should be less than 100nH. An inductance of 15nH is an optimal value.

The following examples explain how to calculate the power dissipation of the BJT with different resistor (R) values.

Example.1:

Supply voltage is 5.0 V, R=1.8 Ω, Max current consumption at VDD_LV (I_{vdd_lv}) = 700 [mA] and nominal VDD_LV = 1.25 [V]

Voltage drop across the R = 1.8 Ω x 700mA = 1.260 [v], voltage at collector 5 V-1.26 V = 3.74 [V] (> 3 V)

Power dissipation on BJT transistor P (Tr): P (Tr) = (5 - 1.25 - 1.26) x 0.7 = 1.743 [w]

Power dissipation on resistor P(R): P(R)= 1.26 x 0.7 = 0.882 [w]

Example.2:

Supply voltage is 5.0 V, R=2.0 Ω, Max current consumption at VDD_LV (I_{vdd_lv}) = 700 [mA] and nominal VDD_LV = 1.25 [V]

Voltage drop across the R = 2.0 Ω x 700mA = 1.400 [V], voltage at collector 5 V-1.4 V = 3.6 [V] (> 3 V)

Power dissipation on BJT transistor P (Tr) given by: P (Tr) = (5 - 1.25 - 1.40) x 0.7 = 1.645 [w]

Power dissipation on resistor P(R) given by: P(R)= 1.40 x 0.7 = 0.980 [w]

3.2.1 Recommended Pass Transistor

The on-chip 1.25 V regulator requires an external BJT for operation. Refer to the following table for recommended pass transistors. Please refer to the MPC5746R Data Sheet to obtain the requirements for the BJT device.

Table 7. Recommended pass Transistors

Transistor	Collector capacitor (C_C)	Base capacitor	Resistor	Supply options
ON semiconductor NJD2873T4	4.7 uF (min) ESR<200 mΩ	-	2 Ω	5.0 V
ON semiconductor NJD2873T4	4.7 uF (min) ESR<200 mΩ	-	-	3.3 V
ROHM 2SCR574D3 A07	4.7 uF (min) ESR<200 mΩ	1 uF	-	3.3 V

3.3 External 1.25 V Supply

If an external regulator is used for the VDD_LV supply, the pass transistor is not required. In this case, the internal voltage regulator driver should be disabled by setting the REG_SEL bit in the Miscellaneous Device Configuration Format (DCF) client. This is accomplished via a DCF record programmed into the UTEST flash memory. See the DCF Chapter of the MPC5746R Reference Manual for complete information regarding the use of DCF records and UTEST flash memory.

Note that the VRC_CTRL will remain active until the Reset Generation Module (RGM) enters the reset phase 3, where the UTEST configuration is read. When using an external VDD_LV supply, the VRC_CTRL pin should be left floating (no connect). See the RGM chapter of the MPC5746R Reference Manual for more information.

3.4 Input and output pins power supply segmentation

Each I/O pin is associated with one of the power domains. The majority of the I/O pins are powered by the VDD_HV_IO_MAIN. The VDD_HV_IO_JTAG, VDD_HV_IO_FEC, and VDD_HV_IO_MSC domains are primarily intended to allow the JTAG, FEC and MSC interfaces to be operated at a voltage level different from the VDD_HV_IO_MAIN domain if desired. However, they can also be used to power a limited amount of I/O pins at an alternative voltage level.

The voltage level supplied on any I/O domain determines the output voltage level and input transition levels for the I/O pins associated with that domain. Each power domain with corresponding I/O pins is shown in Table 8. Each power domain needs to be maintained below 80 mA. In addition, the sum of all I/O power domains should be maintained below 200mA as described in the MPC5746R Data Sheet. Note that, not all of the listed I/O pins are available on some packages.[1]

Table 8. Power Domains vs. I/O

Power Domain	I/O Pins
VDD_HV_IO_MAIN	PD[0–15] PE[0] PF[0–13] PG[1–7, 9–15] PH[0–15] PI[0–5] PJ[0–15] PK[0–2, 4–5, 7–14] PL[0–1]
VDD_HV_IO_JTAG	PB[0–1]
VDD_HV_IO_FEC	PC[0–13]
VDD_HV_IO_MSC	PA[0–13]
VDD_HV_ADV_SAR	PW[0–3] PX[0–15] PY[0–15]
VDD_HV_ADV_SD	PZ[0–15]

3.5 Decoupling capacitor layout priorities

When trade offs must be made in the layout, it is important to ensure that the highest priority decoupling capacitors are placed as close as possible to the MCU. The list below orders the power supply domains from highest to lowest priority in terms of decoupling capacitor placement.

Table 9. Decoupling Capacitor Layout Priorities

Priority	Domain	Description
1	VDD_HV_ADR_SAR VDD_HV_ADR_SD	ADC references
2	VDD_HV_ADV_SAR VDD_HV_ADV_SD	ADC supplies
3	VDD_HV_IO_JTAG	JTAG debug and XOSC supply
4	VDD_LV	Core(s) supply
5	VDD_HV_PMC	Power Management Controller supply
6	VDD_HV_FLA	Flash memory supply/decouple
7	VDD_HV_IO_MAIN	GPIO supply
8	VDD_HV_IO_MSC	Microsecond channel supply
9	VDDSTBY	SRAM standby voltage

- Highest priority is given to the analog-to-digital converters reference and power supply decoupling: VDD_HV_ADR_SAR, VDD_HV_ADR_SD, VDD_HV_ADV_SAR, and VDD_HV_ADV_SD. Clean supplies are vital to ensure that the highest accuracy is achieved with the ADCs. In addition, linear supplies must be used as analog references. The supply for the oscillator (VDD_HV_IO_JTAG) is also prioritized as this helps to ensure reliable and stable operation from the external oscillator.
- Medium priority is given to VDD_LV, VDD_HV_PMC, and VDD_HV_FLA. VDD_LV is the main supply for the on-chip digital logic, including the cores, and this is prioritized because it affects the largest amount of logic on the device. VDD_HV_PMC powers the flash regulator and VDD_HV_FLA is the output of this regulator. A good supply to the flash memory ensures reliable flash programming and erasing.
- VDD_HV_IO_MAIN, VDD_IO_MSC, and VDDSTBY are given lower priority. Although it is still important that these supplies have a clean power signal, the hardware they power is less affected by noise.

3.6 Supply monitoring

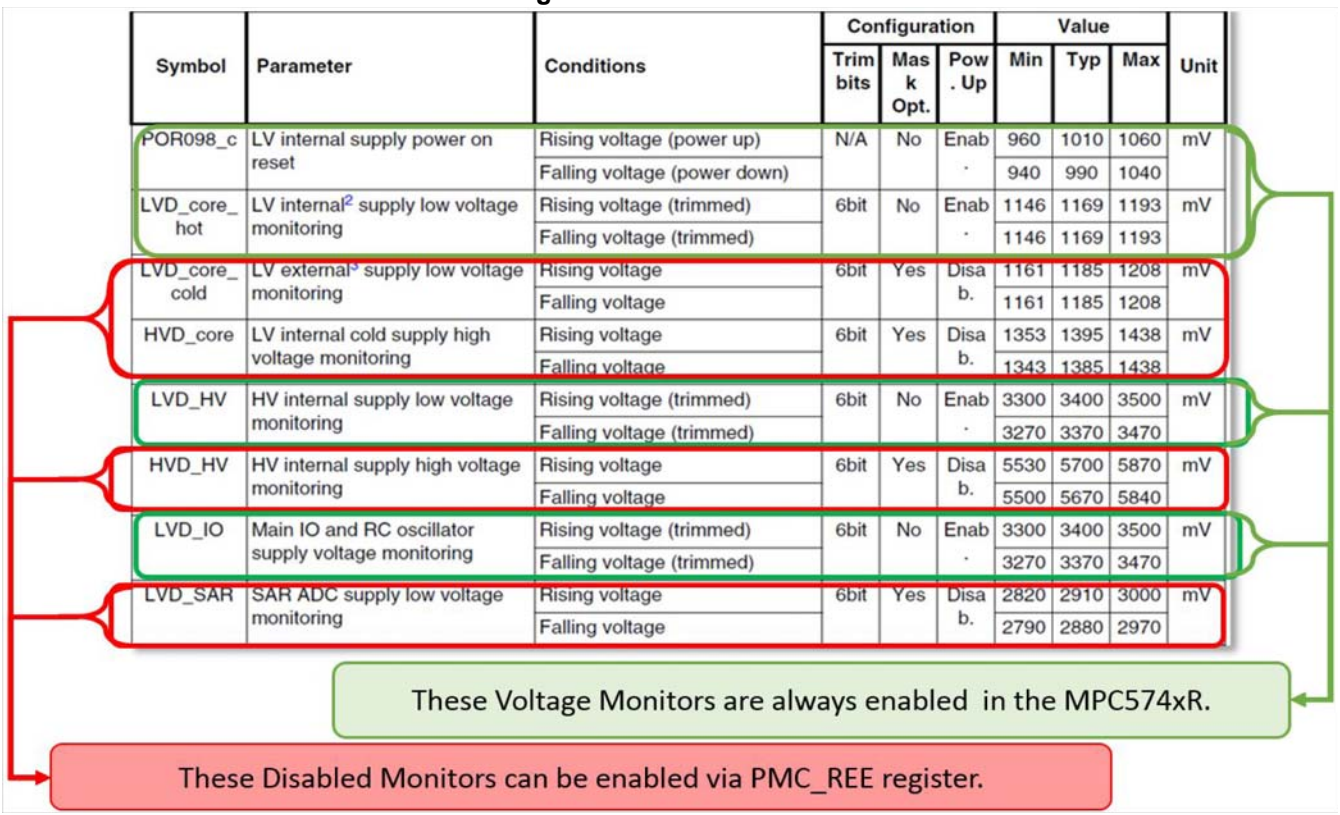
MPC5746R monitors the voltage supplies internally. The function of the power-on reset (POR), low-voltage detect (LVD) and high-voltage detect (HVD) circuits is to hold the device in reset until critical

1.See the MPC5746R Reference Manual for complete information on the power segmentation, input multiplexing and other pin characteristics.

voltages are in specification. LVD/HVD monitor limits are shown in Table 10 for your reference. Use the latest MPC5746R Data Sheet for the final specification values. The device is held in reset regardless of how slow the supply voltage rise is, until the point at which the POR and LVDs are released.

Table 10. Voltage monitor electrical characteristics

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR098_c	LV internal supply power on reset	Rising voltage (power up)	N/A	No	Enab.	960	1010	1060	mV
		Falling voltage (power down)				940	990	1040	
LVD_core_hot	LV internal[2] supply low voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	1146	1169	1193	mV
		Falling voltage (trimmed)				1146	1169	1193	
LVD_core_cold	LV external[3] supply low voltage monitoring	Rising voltage	6bit	Yes	Disab.	1161	1185	1208	mV
		Falling voltage				1161	1185	1208	
HVD_core	LV internal cold supply high voltage monitoring	Rising voltage	6bit	Yes	Disab.	1353	1395	1438	mV
		Falling voltage				1343	1385	1438	
LVD_HV	HV internal supply low voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	3300	3400	3500	mV
		Falling voltage (trimmed)				3270	3370	3470	
HVD_HV	HV internal supply high voltage monitoring	Rising voltage	6bit	Yes	Disab.	5530	5700	5870	mV
		Falling voltage				5500	5670	5840	
LVD_IO	Main IO and RC oscillator supply voltage monitoring	Rising voltage (trimmed)	6bit	No	Enab.	3300	3400	3500	mV
		Falling voltage (trimmed)				3270	3370	3470	
LVD_SAR	SAR ADC supply low voltage monitoring	Rising voltage	6bit	Yes	Disab.	2820	2910	3000	mV
		Falling voltage				2790	2880	2970	



By default VDD_LV internal POR (POR085_c/POR098_c), internal core voltage monitor (LVD_core_hot), VDD_HV_PMC voltage monitor (LVD_HV) and VDD_HV_IO_MAIN voltage monitor (LVD_IO) are enabled. As shown in the mask option field under configuration column of the Table 10, the user can enable/disable the voltage monitors of LVD/HVD by either of following methods.

1. Program the PMC_REE register directly by the application software. But, this method is only valid for LVD_core_cold, HVD_core, HVD_HV and LVD_SAR configurations.
2. Program the PMC_REE_DCF_client DCF record into the UTEST area. With this option, the user can disable the LVD_core_hot, enable the LVD_core_cold, HVD_core, HVD_HV and LVD_SAR configurations. Note that the default configuration will remain active until the RGM enter phase 3, where the UTEST configuration is read.

The POR and LVD circuits function correctly even if the input voltage is non-monotonic. A diagram illustrating the on-chip LVD/HVD circuits is shown in Figure 5. For detailed information on the low-voltage detect (LVD) and high-voltage detect (HVD) circuits, please refer to the MPC5746R Reference Manual and Data Sheet.

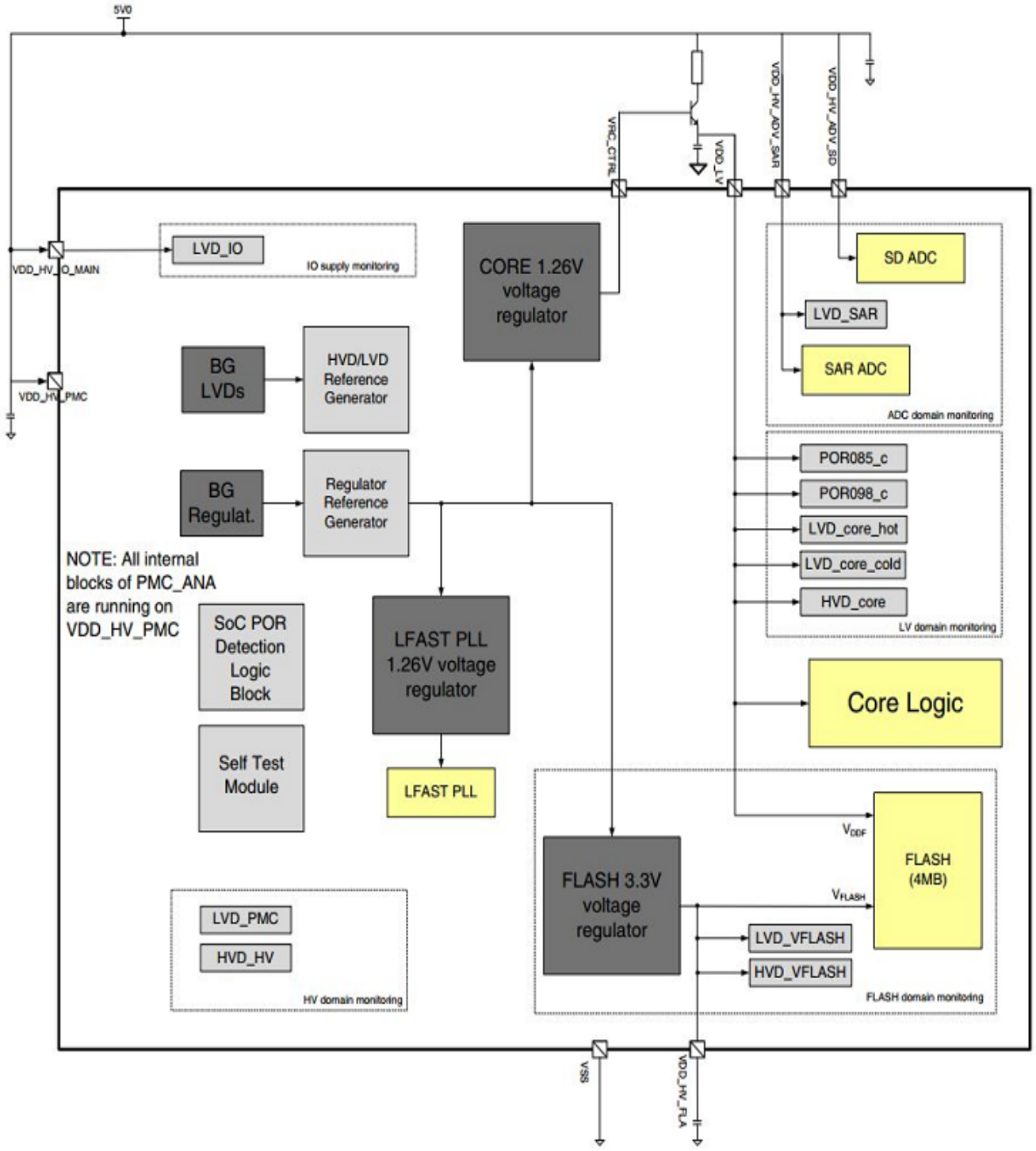


Figure 5. LVD and HVD Implementation

3.6.1 Behavior of LVD / HVD

The internal LVD circuits monitor the voltage on the corresponding supply. If the supply falls below defined values, the LVD asserts either a reset or an interrupt. Figure 6 illustrates how the RESET behaves with different LVD/HVD levels. The LVDs also support hysteresis for the falling and rising trip points.

Although there is an option to disable the LVDs and HVDs following reset, they are capable of being used in a 'monitor' only mode and also capable of generating a safe/interrupt event. The LVDs/HVDs can also be configured after device initialization, preventing a reset when a supply crosses the LVD threshold, providing a higher voltage range. The customer application should monitor and verify that the device voltage supply levels remain in the functional range.

NOTE

VDD_LV internal supply power on reset monitors (POR085_c and POR098_c) cannot be disabled. These trip points are used during the power-up phase and must ensure that an absolute lowest voltage threshold for operation is never crossed. This is not a guarantee that the device will function down to this level. It is rather a guarantee that the device will be reset if this level is crossed.

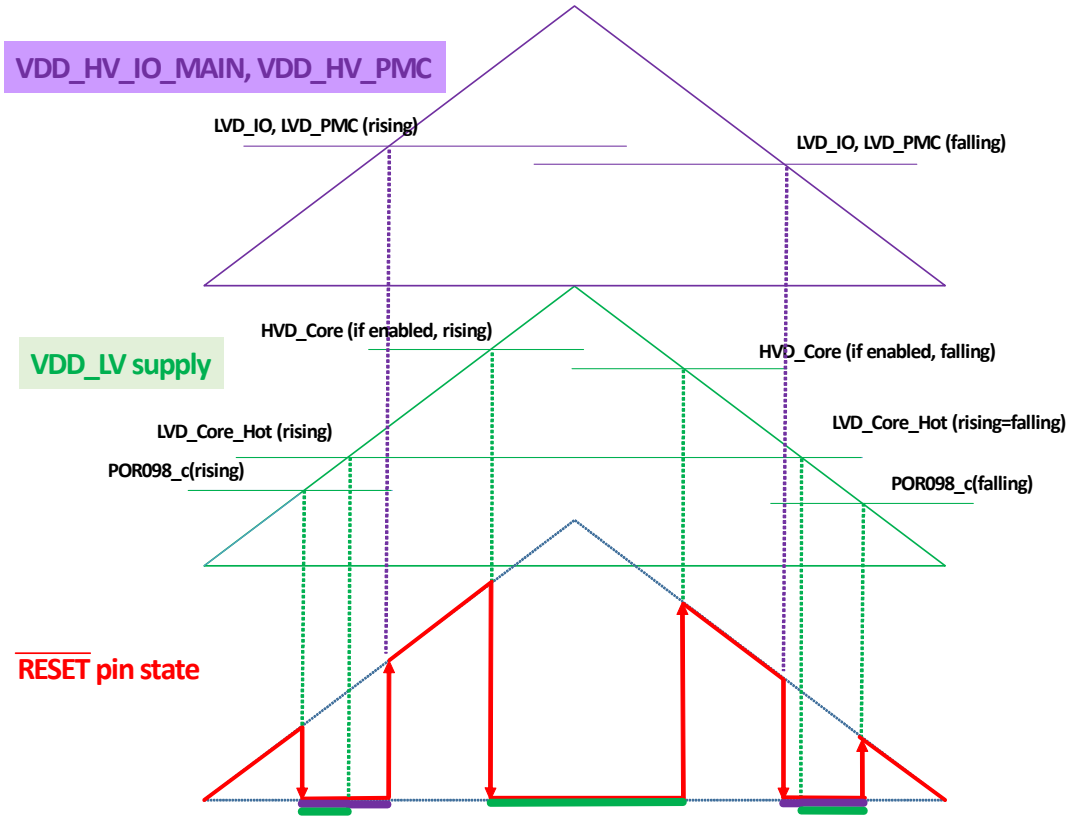


Figure 6. Illustration of LVD/HVD behavior with RESET status

3.6.2 Power-on reset

The power management controller (PMC) controls the Power-On reset (POR) for the MCU. When the critical power supplies are below minimum levels, the MCU is held in the POWER-UP phase of the reset state machine (see the Reset and Boot chapter of the MPC5746R Reference Manual), until the power supplies have reached their specified levels. Power sequencing is not necessary. When the required voltage levels have been reached, the reset generation module (RGM) propagates the device through the next steps of the boot process.

The PMC has three internal power-on reset circuits:

- 1.25 V input supply – This circuit monitors the VDD_LV pin and asserts a reset when the input supply is below defined values.
  - POR085_c monitors the voltage on the 1.25 V input supply on the VDD_LV pin. POR085_c asserts a reset when the input supply is below defined values.
  - POR098_c monitors the voltage on the 1.25 V input supply on the VDD_LV pin. POR098_c asserts a reset when the input supply is below defined values. The POR098_c trip point makes sure that the voltage is high enough for LV logic to initialize and recognize RESET assertion, ensuring the correct logic state. At this point all the LVD circuits become functional.
- 5.0 V input supply – This circuit monitors the VDD_HV_PMC pin and ensures the $\overline{\text{PORST}}$ trip point is high enough to make sure all the LVD circuits are functional.
  - LVD_HV monitors the voltage on the 3.5 - 5.0 V input supply at the VDD_HV_PMC pin, the actual PMC module supply. The POR trip point is high enough to make sure all the LVD circuits are functional i.e. to ensure that the VDD_HV_PMC supply is in range to allow all PMC internal circuits to operate reliably.
- The LVD_VFLASH monitors the flash input voltage and is used to control the power-up sequence, ensuring the flash memory can be accessed prior to the reset phase 0 being completed.

POR085_c2 and POR098_c2 are used for redundancy. Minimum and maximum values and trigger conditions for each LVD and HVD monitor can be found in the MPC5746R Data Sheet. See the Reset chapter in the MPC5746R Reference Manual for $\overline{\text{PORST}}$/$\overline{\text{RESET}}$ pin functionality.

3.6.3 Low-Voltage (LVD) and High-Voltage Detection (HVD)

- All LVDs and HVDs are capable of generating reset.
- All LVDs and HVDs configured for reset generation cause functional or destructive reset. MC_RGM PHASE0 is not exited until all destructive reset conditions are cleared.
- The appropriate bits in the PMC registers are set by LVD and HVD events.
- LVD and HVD control is protected by the System-on-Chip (SoC) wide register protection scheme.
- There are user option bits available to allow degrade of configurable LVDs/HVDs from destructive reset down to functional reset. This is a write once mechanism managed by System Status and Configuration Module (SSCM) during device initialization.
- When the LVD or the HVD is enabled for destructive reset generation, and a trigger event is detected, the external PORST pin is driven low.

3.6.4 Analog module self-test and parameter monitoring

The ADC interface includes connections to the PMC internal voltages for diagnostic purposes. An analog multiplexer and the buffer are inside the PMC. SAR ADC0 converts the selected voltage, which can then be evaluated by the CPU. Voltages in the PMC module can be monitored with the ADC and the ADC does not impact the PMC voltage levels. These signals are used for calibration, diagnostics during test or to allow the application to actively monitor the signal levels. There is a dedicated ADC channel for these monitoring purposes.

Table 11 lists all the internal test signals that can be monitored using SAR ADC0.

Table 11. ADC 0 Mux Interface

PMC_ADC_CS[ADC_CHSE]	ADC Channel Output	Typical Value
6'b000000	ADC Channel Off	
6'b011110	por085_c sense value	1.25 V (CORE supply)
6'b011101	por085_c reference value	0.915 V
6'b011100	por098_c sense value	1.25 V (CORE supply)
6'b011011	por098_c reference value	1.01 V
6'b011010	por085_c2 sense value	1.25 V (CORE supply)
6'b011001	por085_c2 reference value	0.905 V
6'b011000	por098_c2sense value	1.25 V (CORE supply)
6'b010111	por098_c2 reference value	0.993 V
6'b010110	lvd_core_cold sense	1.25 V (CORE supply)
6'b010101	lvd_core_cold_reference	1.24 V
6'b010100	lvd_core_hot_sense	1.25 V (CORE supply)
6'b010011	lvd_core_hot_reference	1.21 V
6'b010010	hvd_core_sense	1.25 V (CORE supply)
6'b010001	hvd_core_reference	1.43 V
6'b010000	por260_c divider tap point	2.55 V
6'b001111	por260_c reference	1.2 V
6'b001110	por260_c2 divider tap point	2.55 V
6'b001101	por260_c2 reference	1.2 V
6'b001100	lvd_pmc divider tap point	1.98 V
6'b001011	lvd_pmc reference	1.2 V
6'b001010	hvd600 divider tap point	1.13 V
6'b001001	hvd600 reference	1.2 V
6'b001000	lvd_flash divider tap point	1.31 V
6'b000111	lvd_flash reference	1.2 V
6'b000110	hvd_flash divider tap point	1.13 V

Table 11. ADC 0 Mux Interface

PMC_ADC_CS[ADC_CHSE]	ADC Channel Output	Typical Value
6’b000101	hvd_flash reference	1.2 V
6’b000100	lvd_io divider tap point	1.97 V
6’b000011	lvd_io reference	1.2 V
6’b000010	Reserved	—
6’b000001	Reserved	—
6’b000000	Reserved	—
6’b1111111	Reserved	—
6’b111110	Reserved	—
6’b111101	Reserved	—
6’b111100	Reserved	—
6’b111011	Reserved	—
6’b111010	lvd_buddy reference	1.05 V
6’b111001	lvd_buddy sense	1.2 V (BD supply)
6’b111000	lvd_sar_adc divider tap point	2.25 V
6’b110111	lvd_sar_adc reference	1.2 V
6’b110110	hvd_sar_adc divider tap point	1.13 V
6’b110101	hvd_sar_adc reference	1.2 V
6’b110100	bandgap voltage with only curve trimming	1.205 V
6’b110011	nwellbias regulator output	1.25 V
6’b110010	nwellbias regulator reference	1.25 V
6’b100100	ioseg3_sense	VDD_HV_IO segment 3
6’b100011	ioseg2_sense	VDD_HV_IO segment 2
6’b100010	vrefh_sd_adc	5 V
6’b100001	vrefh_sd_adc	5 V
6’b100000	vss_sd_adc	0 V

3.7 Power sequence

The following section describes the power sequence and the relationship between the different supplies during power-up and power-down.

The device is considered to be in a power sequence (or POWERUP state) when the power is not supplied or is only partially powered. An internal power-on signal is used to identify the POWERUP state. This signal is released high on exit of the power sequence. The power-on signal is a combination of certain LVDs that are monitoring supplies:

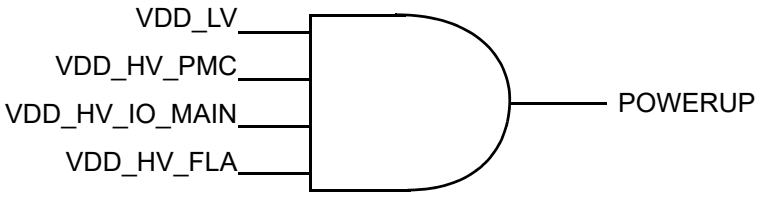


Figure 7. Logical connection between power domains

The actual threshold used for each LVD depends on the configuration of the device. This is configurable by hardware (flash option bit settings) or by software (LVD event configuration through a register interface). Once the power-on signal has been asserted, the device configuration is reset to default power-up configuration; during the initialization phase, the device defaults to a pre-determined state for each of the LVDs, HVDs, and the internal regulators. As the flash memory becomes available, the differential read process allows the trimmed data to be available for trimming the internal LVDs, HVDs, and regulators.

3.7.1 Power-up sequence

In this section, the assumption is made that all supplies are low when entering the power-up sequence. Brown-out and power down sequences are discussed in following sections.

At the beginning of power-up, the internal power-on signal remains low due to the parasitic diodes. As soon as the minimum threshold is reached on VDD_LV, the power-on signal is forced low. It remains low until the power-up LVDs reach their upper (not trimmed) threshold. During power-up, all functional pins are maintained in a known state as described in Table 12.

Table 12. Functional Terminal State - Power-Up and Reset

Pin Type	POWERUP Pad State	During RESET Pad State	Out of RESET Pad State
PORST	strong pull-down	weak pull-down	weak pull-down
RESET	strong pull-down	weak pull-up	weak pull-up
GPIO	high impedance	weak pull-up	weak pull-up
ANALOG	high impedance	high impedance	high impedance
ERROR	high impedance	high impedance	high impedance
JCOMP	high impedance	weak pull-down	weak pull-down
TCK	high impedance	weak pull-down	weak pull-down
TMS	high impedance	weak pull-up	weak pull-up
TDI	high impedance	weak pull-up	weak pull-up
TDO	high impedance	high impedance	high impedance

The power-up sequence is as follows:

1. Digital reset is asserted, ensuring that all module registers are reset to their power-on value.
2. The POWERUP state is exited when both VDD_LV and VDD_HV are above threshold.

3. After both LV, HV and temperature POWERUP exit conditions have been verified, the internal power-on signal is released to all analog modules.
4. The internal RC oscillator module starts initialization and provides a clock to the system. The PMC digital interface reset is released after two RC clock cycles.
5. The device proceeds with the reset sequence through RGM phase PHASE0, PHASE1[DEST], PHASE2[DEST] and PHASE3[DEST].
6. Voltage detector (LVD/HVD) modules are trimmed at the beginning of PHASE3[DEST]. Trimming of the LVDs/HVDs is done by the SSCM at low voltage. After trimming is completed, the SSCM waits for PMC acknowledge to proceed with the reset sequence.
7. The configurable LVD/HVD modules are optionally enabled at the beginning of PHASE3[DEST] by programming the PMC_REE/PMC_RES DCF records. After trimming, the PMC interface monitors all the HVD/LVD outputs that have been enabled by the flash user option bits. When all enabled LVDs/HVDs are released and the analog temporization period has elapsed, LVDs/HVDs are unmasked.
8. When the LVDs are masked, the device relies on the PORST signal to detect a voltage failure during power-up. The device must wait for PORST to be released high before proceeding with power-up sequence. This may increase the amount of time necessary to complete the reset sequence.
9. After all LVDs/HVDs are unmasked the SSCM proceeds with the reset sequence, eventually running full speed accesses to the extended flash option bits required to complete device configuration.
10. The VDD_HV conditions to exit POWERUP are as follows:
    — LVD_HV and LVD_IO upper threshold is crossed
    — LVD_VFLASH is crossed

3.7.2 Power-down sequence

During power down, any time the VDD_HV or the VDD_LV supply crosses the respective LVD threshold, the device enters the POWERUP state. The power-down sequence is entered as soon as the threshold of one of the LVD_HV, LVD_IO, LVD_core_hot, LVD_VFLASH or POR98 is crossed. The device supplies may then proceed to drop down to ground either through device leakage or external pull-down.

3.7.3 Brown-out management

During brown-out, the MPC57xx devices re-enter the POWERUP phase as soon as the LVD/HVD threshold of either VDD_LV or VDD_HV is crossed.

3.7.4 Low voltage during crank

The device is able to continue operation at the minimum input voltage during cranking. In order to proceed with execution during cranking and prevent device reset, it is important to correctly configure the high voltage LVDs. Figure 8 illustrates a typical cranking voltage profile.

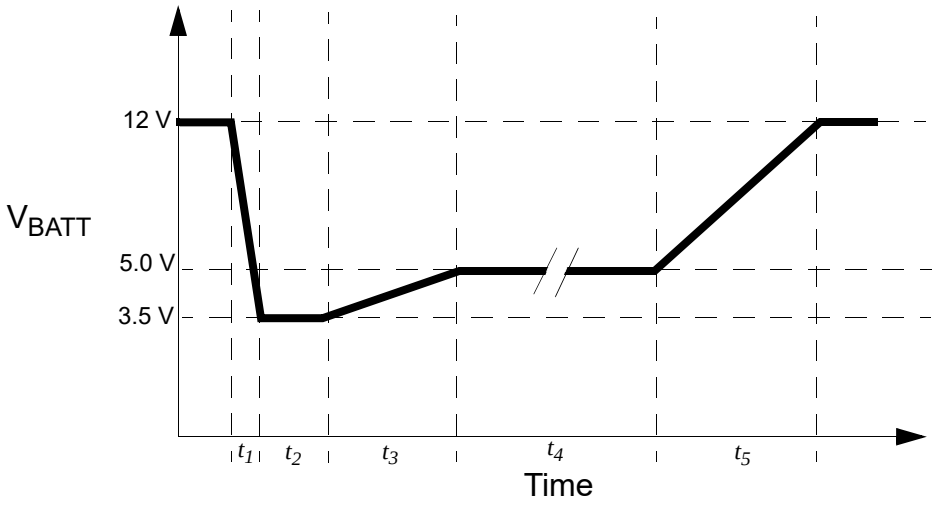


Figure 8. Example Cranking Voltage Profile

The above diagram shows the input voltage falling to 3.5 V at the battery terminals. Several options are available to filter the supply sag.

- DC-DC converters to boost the supply
- Additional capacitance to filter the sag
- External power supply system asserts a reset

4 Clock Circuitry

MPC5746R can use either the internal RC oscillator, an external crystal or an external clock as the reference clock. This reference is qualified by multiple methods before the Phase-Locked Loop (PLL) will begin lock operation. The ‘pre’ Frequency-Modulated Phase-Locked Loop (FMPLL) circuitry consists of an automatic level-controlled amplifier, a comparator, a loss of clock detector, and a pre-divider.

Care must be taken in the layout and design of the circuitry around the crystal and FMPLL power supplies. Any noise in these circuits can affect the accuracy of the clock source to the FMPLL. The PLLs are powered by VDD_LV. The oscillator (OSC) is powered by VDD_HV_IO_JTAG. Noise on either of these supplies can affect the accuracy and jitter performance of the oscillator and PLLs.

In order to minimize any potential noise, connect the capacitors recommended in Table 6 to the VDD_LV and VDD_HV_IO_JTAG supplies.

MPC5746R provides configurable internal load capacitors for the external crystal (Cx and Cy in Figure 9). This feature is intended to simplify the hardware design and reduce the overall system cost by eliminating external components and reducing the printed circuit board (PCB) footprint. If an 8 MHz–16 MHz crystal is used, as shown in Figure 10 external load capacitance must be connected. If the external crystal is to be started during power-up by hardware, the crystal frequency and the selected load capacitance must be specified in the UTEST Miscellaneous DCF Client records field. See the MPC5746R Reference Manual for details.

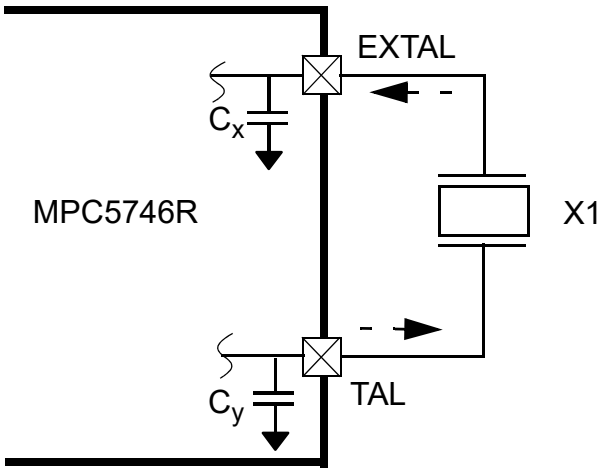


Figure 9. Internal Crystal Load Capacitors and Crystal Connections

Since the layout of the module/board can affect the component values required, customers should have their board characterized by their crystal vendor to recommend values for C_X and C_Y. The values shown in this document should be used as a starting point. These should be re-characterized for any change to the oscillator circuit layout, including routing changes of other circuitry near the crystal circuit.

The crystal should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where ever possible. Do not allow any signals to cross the crystal connections to the device. Absolutely no high current or high speed signals should be run near any of the crystal components.

Other than the connections shown in the figure above, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry.

The following figure illustrates an example circuitry of oscillator with ground routing with external load capacitors.

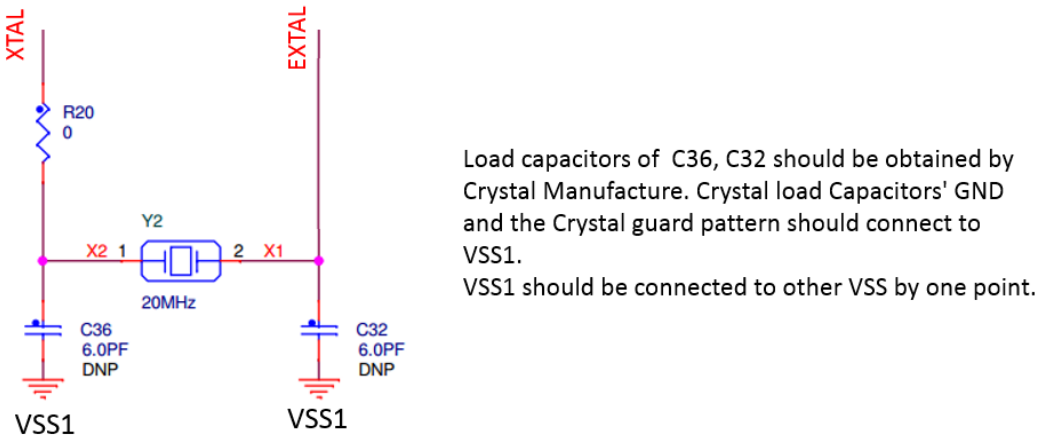


Figure 10. External oscillator circuitry example

The recommendations from the crystal manufacturer will include not only a series resistor value but also the load capacitance required for the crystal (the total crystal load capacitance is usually specified in the crystal Data Sheet). Keep in mind that the load capacitance is the sum of the following:

- Physical capacitors (C_X and C_Y)
- Capacitance of the MCU
- Capacitive loading of the board (C_{PCB})
- Pin capacitance (C_{MCU_PIN}) of the MCU EXTAL and XTAL balls (BGA balls are specified as 7 pF maximum)

The requirement for the crystal vendor to measure the customer board is due to the board capacitance effect on the crystal load capacitors.

Generally, the method to calculate the capacitor values to use for C_X and C_Y is provided by the following formulas:

$$C_A = C_B = 2 \times C_L$$
$$C_A = C_X + C_{MCU\_PIN} + C_{BOARD}$$
$$C_B = C_Y + C_{MCU\_PIN} + C_{BOARD}$$

C_L should come from the crystal specifications (requirements). C_{BOARD} should also include any socket capacitance if a socket is used. C_{MCU_PIN} is listed in the MPC5746R Data Sheet as the discrete load capacitance to connect to EXTAL and XTAL.

If an external clock is being used as clock reference to the MCU, then the XTAL pin should be connected to ground and the clock should be provided to EXTAL as shown in the figure below.

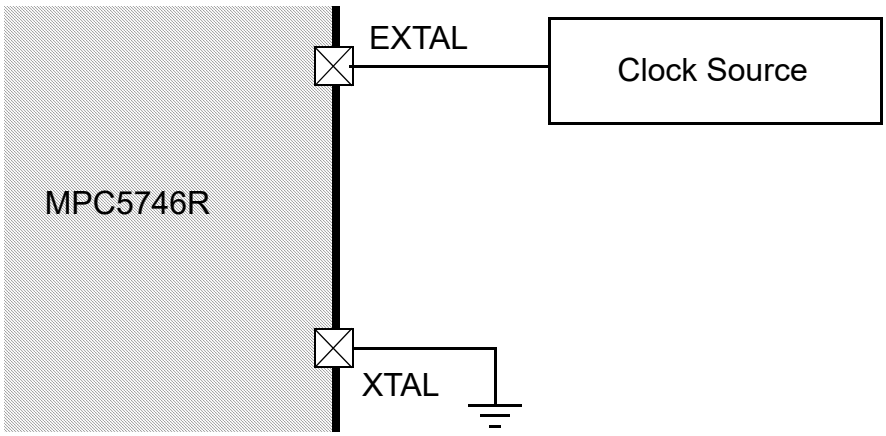


Figure 11. MPC5746R External Clock Connection

5 Device Reset Configuration

MPC5746R does not require external reset circuitry for device configuration. The device is configured during reset based on data in flash memory.

5.1 External reset signals

MPC5746R devices feature two external reset signals:

- Power-on reset ($\overline{\text{PORST}}$)
- External reset ($\overline{\text{RESET}}$)

Both external reset signals are bidirectional and active-low. $\overline{\text{RESET}}$ indicates whether the device is active (high signal) or in reset. It is in a weak pull-up state after the reset sequence has completed. An external 4.7 kΩ pull-up resistor on $\overline{\text{RESET}}$ is required. A falling edge on this pin will trigger a functional reset to the Reset Generation Module (RGM). Holding this pin low will keep the device in the last phase of the reset sequence (Phase3[Functional]).

After reset, $\overline{\text{PORST}}$ is configured as a weak pull-down for safety reasons. In case $\overline{\text{PORST}}$ is disconnected the device will remain in reset. $\overline{\text{PORST}}$ is released when the device leaves the power-up state of the RGM. $\overline{\text{PORST}}$ must be forced high externally so the device will leave the reset state. The internal weak pull-down maximum current of $\overline{\text{PORST}}$ is 100 uA. It is recommended that an external 4.7 kΩ pull-up resistor be used to ensure the $\overline{\text{PORST}}$ voltage level remains safely above the threshold.

Figure 12 illustrates the typical system configuration of $\overline{\text{RESET}}$ and $\overline{\text{PORST}}$ pins with the external components.

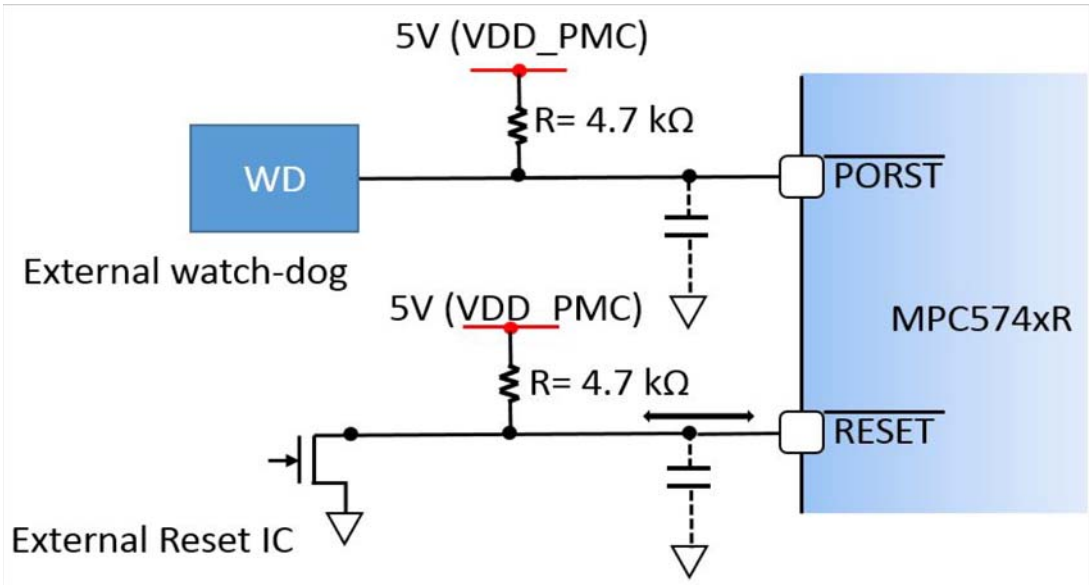


Figure 12. example Circuitry for $\overline{\text{RESET}}$ & $\overline{\text{PORST}}$ pins

5.2 Reset Out ($\overline{\text{RSTOUT}}$)

MPC5746R has an optional Reset out signal which can be used to notify external systems that the MCU has been reset. Pin PJ[5] can be configured to drive the reset out signal (RSTOUT) without generating the internal reset. $\overline{\text{RSTOUT}}$ will follow the $\overline{\text{RESET}}$ pin until reconfigured in software.
In a POR event $\overline{\text{RSTOUT}}$ is internally pull-up then actively drives low during reset PHASE3 and drives

high at the end of reset PHASE3. Please refer the MPC5746R Reference Manual for more information.

6 Input/Output Pins

The I/O pads are distributed across the I/O supply segments. Each I/O supply segment is associated with a VDD_HV_IO/VSS_HV supply pair. In order to ensure device reliability, the total current of the I/O on a single segment should remain below the maximum current per segment value as defined in the data sheet.

If there is a need to source/sink current through some I/Os, care should be taken to spread the amount of current between the segments.

In the MPC5746R family, all of the I/Os have a weak pull up/down feature. In addition, input buffers and the weak-pulls are enabled for all I/Os by default. SD_ADC analog input channels are only multiplexed with digital inputs.

6.1 I/O Pad Block Diagram (GPIO & Module Multiplexer Port)

The following figure illustrates an I/O pad (without analog inputs) internal block diagram and the input/output multiplexer. This also illustrates the internal input/output control, pull-up/pull-down control and module selection. Please refer the system integration unit lite2 (SIUL2) chapter of the MPC5746R Reference Manual for more information

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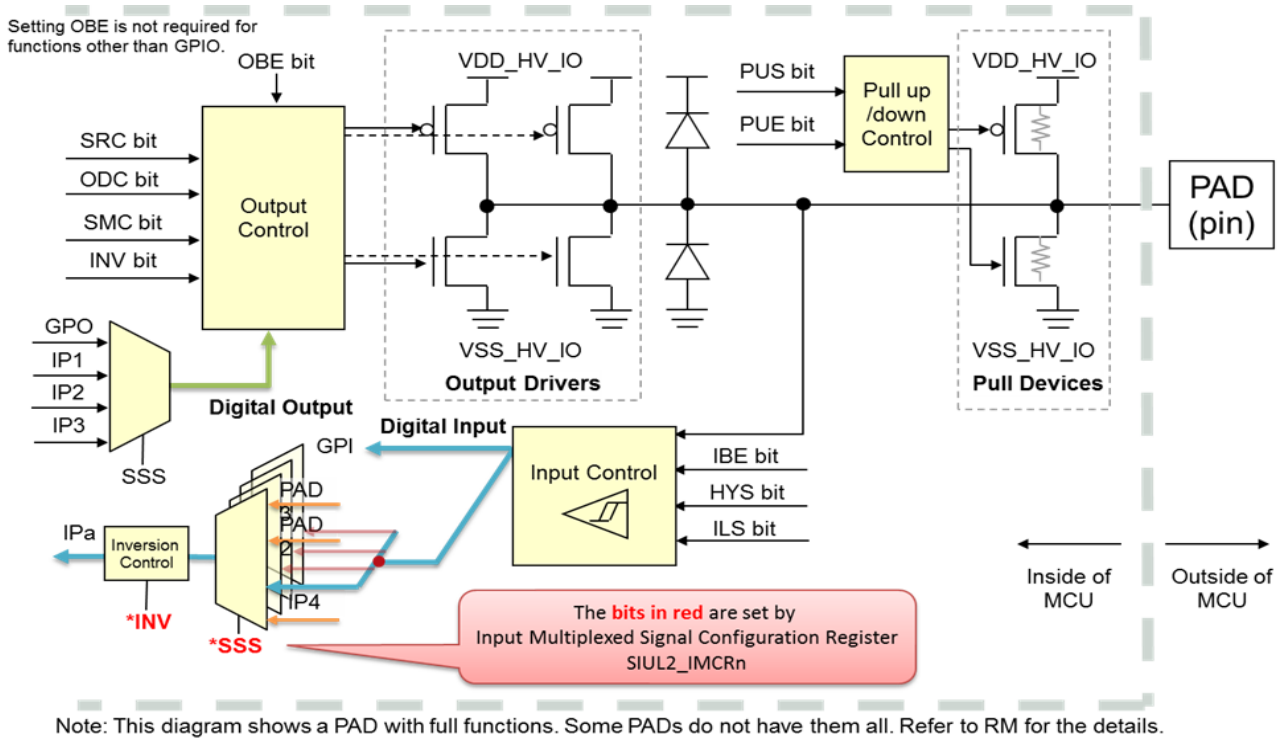
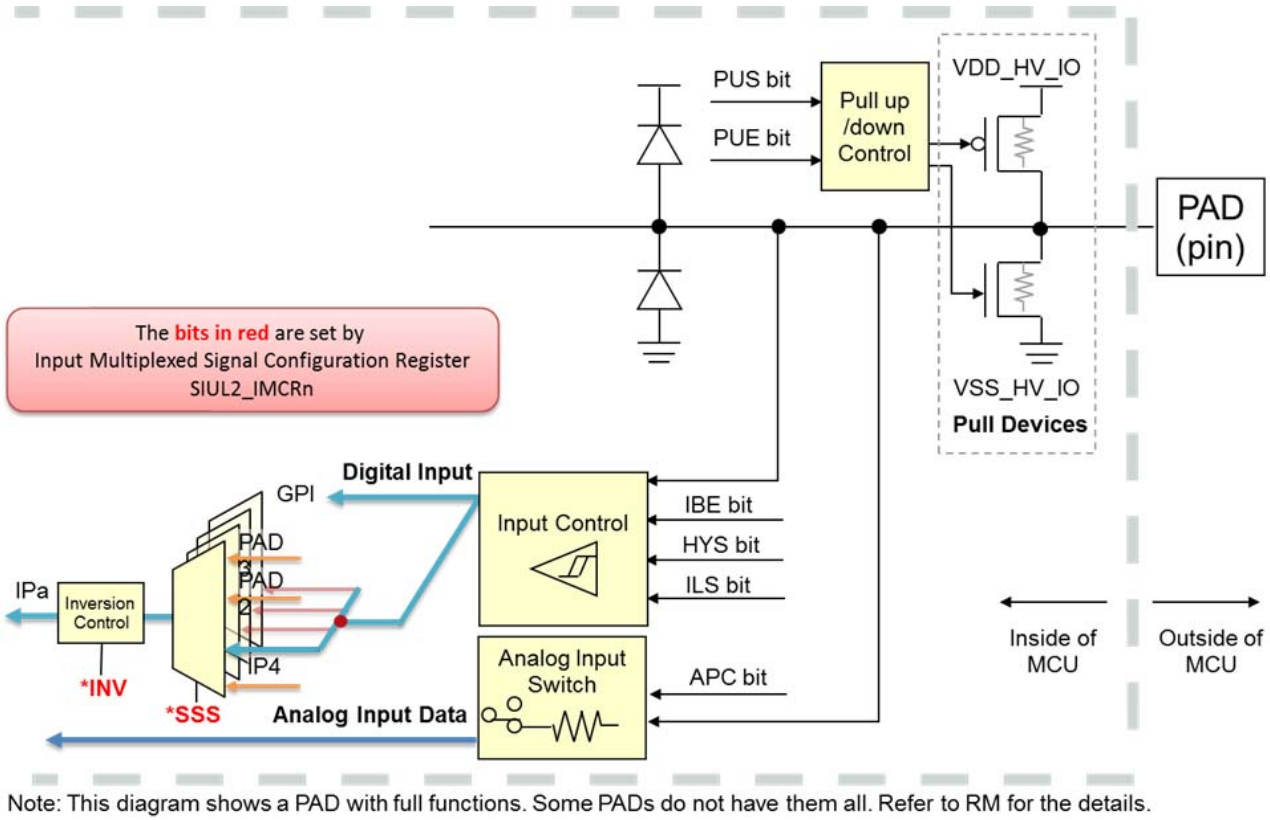


Note: This diagram shows a PAD with full functions. Some Pads do not implement all functions. Refer the MPC5746R reference manual for the details.

Figure 13. I/O pad block diagram without analog inputs

6.2 I/O Pad Block Diagram with analog input (GPIO & Module Multiplexer Port)

The figure below illustrates the I/O pad internal block diagram with analog inputs. This also illustrates the internal digital/analog input control, pull-up/pull-down control and module selection. Please refer to the system integration unit lite2 (SIUL2) chapter of the MPC5746R Reference Manual for more information.



Note: This diagram shows a PAD with full functions. Some Pads do not implement all functions. Refer the MPC5746R reference manual for the details.

Figure 14. I/O pad block diagram with analog inputs

6.3 Unused GPIO Pin Termination

Most microcontrollers are designed to be used in a variety of applications and often a particular application does not use 100% of the MCU resources. To increase EMC performance, unused clocks, counters or I/Os, should never be left floating or unconnected.

Following table describes the termination options that the user should follow for the unused pins.

Table 13. Termination options for unused pins

(1) External pull up or down
(2) Direct connection to VDD source or GND.
(3) Configure as input pin and enable internal weak pull up or down by software
(MSCR Register PUE=1 & PUS=1 or 0)
(4) Configure as output pin and set output to Low or High by software
(MSCR Register OBE=1 & GPDO Register PDO=1 or 0)
(5) No configuration （MSCR Register IBE=0 & OBE=0 as default）

Pin Type	Termination	Note
Pin which is exposed to IO pad on the package.	(1)	Recommended. Benefit of this option is to ensure the termination during Power-On. But this option costs more.
	(2)	Take care for output collision toward external driver due to software mishandling.
	(3)	Recommended. But take care for long wiring to external device without external pull up or down.
	(4)	Recommended. Don't apply for input pin. Take care for output collision toward external driver due to software mishandling.
	(5)	
Pin which is not exposed out of the package	(3)	Recommended.
	(4)	Recommended. Don't apply for input pin.
	(5)	

6.4 Injection Current

The following guidelines should be followed with respect to injection currents.

- Maximum injected input current on any pin during overload condition: +/-3 mA
- Note that the ADC input pad must never exceed its own IO segment supply voltage where the input pad resides. If ADC input pin voltage is higher than IO supply where the pin resides, then this will cause ESD diodes in pads to forward bias.
- Applying signals to pins (~3.3/5.0 V) during power-off (VDD ~0 V) must be considered as an over load condition. Series resistors between signal sources and pins may be needed to limit injection current I_{IC}.
- In general, any over load conditions (positive or negative voltage out of the maximum VIH and the minimum VIL spec applied to the pins) should be avoided.
- Injection current may cause to increase the leakage current on the pins next to the injected pin.

6.5 Internal Weak Pull-Up/Down

The internal weak pull feature is used primarily for device protection. The maximum weak pull current specification is important when the application requires the internal weak pull up to oppose a voltage level caused by an external pull up/down resistor before software changes the internal weak pull configuration. Figure 15 shows an example configuration.

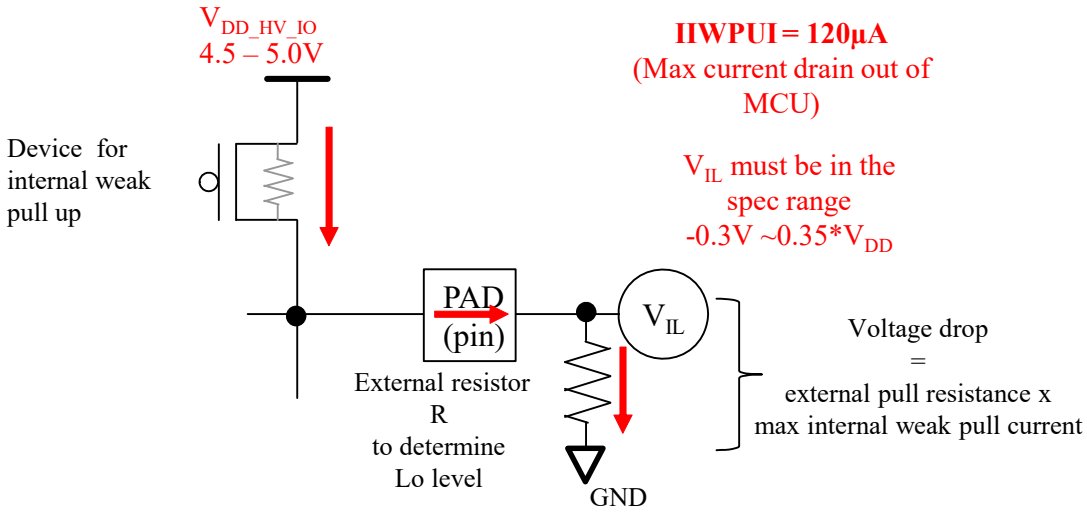


Figure 15. Example Weak pull up/down configuration.

Following example describes how to calculate a suitable pull-up resistor value based on data sheet specifications.

Example:

External resistor R=4.7 kΩ

120 uA max weak pull up current as specified in the data sheet when VDD_HV_IO >= 4.5 V.

Voltage drop (V_{IL})= 4.7 kΩ x 120 µA = 0.56 V

The voltage above pin is less than V_{IL} max= 0.35x4.5 V = 1.575 V at V_{DD}=4.5 V

Therefore R=4.7 kΩ is suitable.

The same principal applies for internal weak pull down scenarios.

7 Debug Options available

The MPC5746R production device (PD) supports a standard 14-pin JTAG connector. A development solution is provided by the 292BGA emulation device (ED). The ED supports a high-speed serial Nexus trace port that utilizes a Xilinx Aurora interface as the transport mechanism. The ED is mounted to a Trace Adapter that allows the customer to install it on production hardware for development support. This ED solution may be ordered through your NXP representative.

NOTE

It is possible that “keep-out” areas may be required by some debug tools. Consult the preferred debug tool vendor to determine any area that must remain clear around the debug connector. Also note that the ED solution may require a small keep out area on the customer PCB to accommodate the adapter and device. Refer to the drawings provided with the MPC5746R ED system.

7.1 MPC5746R JTAG connector

Figure 16 shows the pin-out of the recommended JTAG connector to support MPC5746R device. The recommended connector for the target system is Tyco part number 2514-6002UB.

NOTE:
When using the Emulation Device, VDD_HV_IO_JTAG should be supplied by the VDD_HV_BD supply.

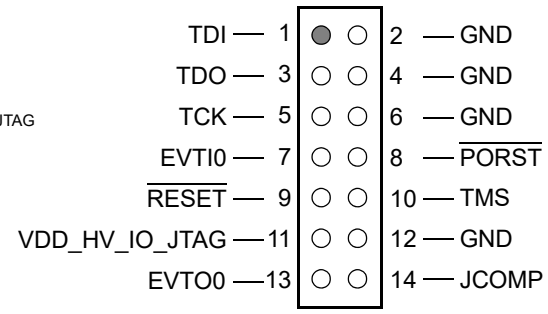


Figure 16. JTAG Connections

7.2 MPC5746R high-speed Nexus serial trace connector

For high speed Nexus Aurora trace applications, the Samtec™ ERF8 Series connector is recommended in the IEEE-ISTO 5001™-2012 standard. For the MPC57xx family, the 17 position (34 pins) connector is recommended. The part number of the Samtec connectors are shown in the following table.

Table 14. Recommended high-speed serial trace connector part numbers

Connector	Part number (Samtec)	Style	Description
HS34	ASP-137973-01	Samtec ERF8 Series, 17 position by 2 row	Vertical mount for MCU module
HS34	ASP-177706-02	Samtec ERF8 Series, 17 position by 2 row	Right Angle mount for MCU

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of seventeen contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity. If at all possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the printed circuit board. Figure is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

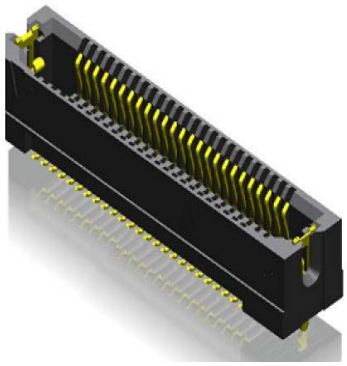


Figure 17. Recommended Nexus connector

Table 15 shows the recommended pin-out for Samtec connector.

Table 15. MPC5746R high-speed serial trace connector

Function	Pin No	Pin No	Function
VSS	GND	GND	VSS
TX0+	1	2	VREF
TX0-	3	4	TCK/TCKC
VSS	5	6	TMS/TMSC
TX1+	7	8	TDI
TX1-	9	10	TDO
VSS	11	12	JCOMP
TX2+	13	14	$\overline{\text{EVTI1}}$
TX2-	15	16	$\overline{\text{EVTI0}}$
VSS	17	18	$\overline{\text{EVTO0}}$
TX3+	19	20	$\overline{\text{PORST}}$
TX3-	21	22	$\overline{\text{RESET}}$
VSS	23	24	VSS
(TX4+)[1]	25	26	CLK+
(TX4-)[1]	27	28	CLK-

Table 15. MPC5746R high-speed serial trace connector

Function	Pin No	Pin No	Function
VSS	29	30	VSS
(TX5+)[1]	31	32	$\overline{\text{EVTO1}}$
(TX5-)[1]	33	34	N/C or WDT
VSS	GND	GND	VSS

[1] TX4-, TX4+, TX5-, and TX5+ these pins are not used on this device.

It is recommended that the "even" side of the connector be mounted closer to the edge of the printed circuit board to facilitate a direct connection to the tool.

7.3 Nexus Aurora Target System Requirements

The Nexus Aurora interface requires termination and AC coupling of the signals between the target system and the tool. The termination resistor for the Aurora clock is located inside the MCU. An external termination resistor is required. The transmit termination resistor must be implemented in the target system; however, it may be implemented internally to the FPGA of the tool.

Figure 18 illustrates the nexus aurora termination and coupling circuit between the tool and the MCU.

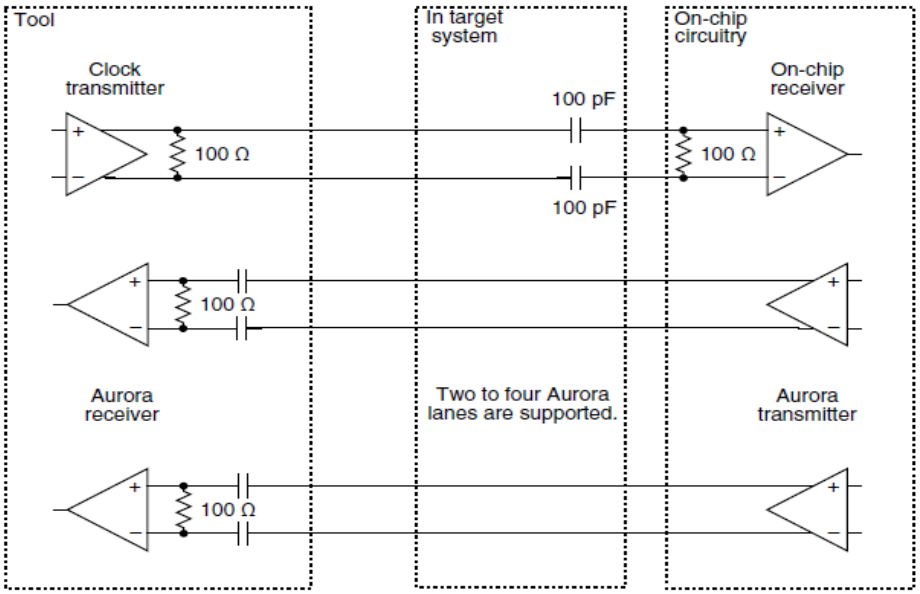


Figure 18. Nexus Aurora termination and coupling circuits

7.4 External circuitry

Additional resistor pull-ups/pull-downs may be required for the JTAG debug circuitry. The MPC5746R device includes internal pull devices that ensure the pins remain in a safe state; however, if there is additional circuitry connected to the JTAG pins, or long traces that could be affected by other signals (due

to crosstalk from high-current or high-speed signals), optional external pull resistors as shown in Table 16 can be added to ensure proper operation under all conditions.

Table 16. Optional External Pull Ups/Pull Downs

JTAG Signal	Component	Description
JCOMP	10 kΩ pull-down resistor	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.
$\overline{\text{PORST}}$	4.7 kΩ pull-up resistor	The $\overline{\text{PORST}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU.
$\overline{\text{RESET}}$	4.7 kΩ pull-up resistor	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU.
$\overline{\text{EVTI}}$	10 kΩ pull-up resistor	A pull-up resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.
TCK[1]	series 0 Ω resistor	A series resistor may be required on TCK to allow the TCK signal in the target system to be disconnected for signal integrity if TCK is connected to multiple connectors.

[1] TCK isolation may be required if using both a JTAG connector and a Nexus Aurora trace connector in the target system to reduce reflections. Selection of TCK to either connector should be supported. On the NXP Trace Adapter board, by default, the debug connectors signals are not connected to the target system and are already isolated.

In addition to the pull-up and pull-down resistors, some systems may want to use buffers between the JTAG connector inputs (JCOMP, TDI, TDO, TMS, EVTI, EVTO, PORST and RESET) and the MCU. This will prevent over-voltage conditions from causing damage to the MCU pins. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit for this application is the Texas Instruments SN74CBTLV38615. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable pin should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

8 Emulation device

The emulation device (ED) is a multi-die MCU that adds additional functionality for calibration and debug during the ECU development. The ED consists of the production die (PD) and a buddy die (BD). The BD JTAG interface replaces the JTAG interface of the PD, but allows access to the PD JTAG interface by passing control from the BD JTAG interface to the PD JTAG interface. Please refer the MPC5746R Reference Manual and AN5181:"Introduction to the MPC5746R Trace Adapter" application note for more information.

It is recommended that customers use the NXP Trace Adapter (TA) for development systems. The TA allows development features with a production ECU board layout. TA solutions are described in Section 8.2. and available at www.NXP.com.

Figure 19 illustrates the LFDBGK46RT4S2A adapter card for MPC5746R 292-pin BGA ED with Aurora interface.

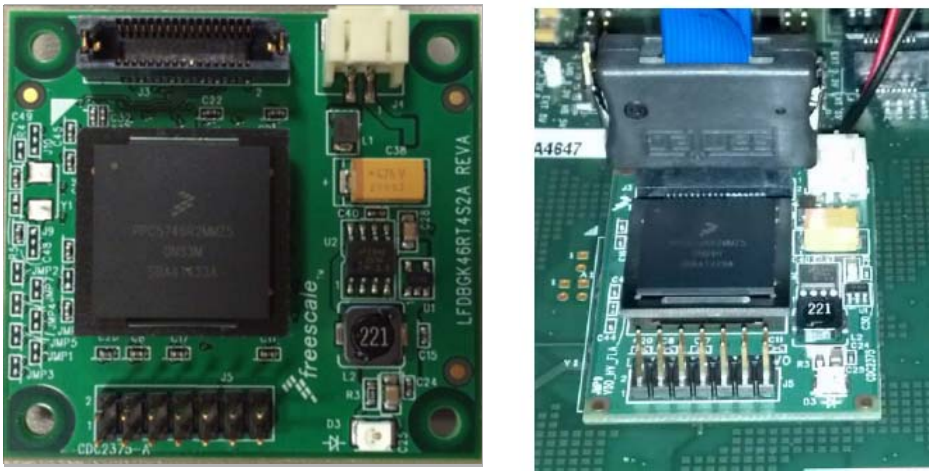


Figure 19. 292 BGA to 252 PGA Adapter card for Emulation and Debug Device

8.1 Emulation device power sequencing

The power supplies to the ED can be sequenced in any of the following orders.

- Power the BD first with 12 V external supply
- Power the PD second
- Or power both BD and PD at same time

8.2 Available ED Trace Adapters

There are two Trace adapters available 1) 292 BGA to 252 PGA and 2) 292 BGA to 208 PGA. The 208 PGA is used to support both 176 LQFP device and the 144 LQFP device. Another adapter is required to adopt the 208 PGA to either the 176 LQFP footprint or the 144 LQFP footprint. Refer to Table 17 for adapter card part numbers.

Table 17. MPC574xR ED Adapter Card types

Pin conversion	Part Number	Description
292BGA to 252PGA	LFDBGK46RT4S2A	292 PIN 0.8MM BGA to 252 0.8MM PGA Adapter with Aurora interface for MPC574xR
292BGA to 176LQFP	LFDBGK46RT4QA LFTAK46MQM2A	292 PIN 0.8MM BGA to 208 1.0MM PGA Adapter with Aurora interface for MPC574xR. 208 pin 1.0mm PGA to 176 pin 0.5mm QFP target Adapter board for MPC574xR
292BGA to 144LQFP	LFDBGK46RT4QA LFTAK46MQLA	292 PIN 0.8MM BGA to 208 1.0MM PGA Adapter with Aurora interface for MPC574xR. 208 pin 1.0mm PGA to 144 pin 0.5mm QFP target Adapter board for MPC574xR

Refer the following illustration for 292 MAPBGA package mapped into a 252BGA footprint.

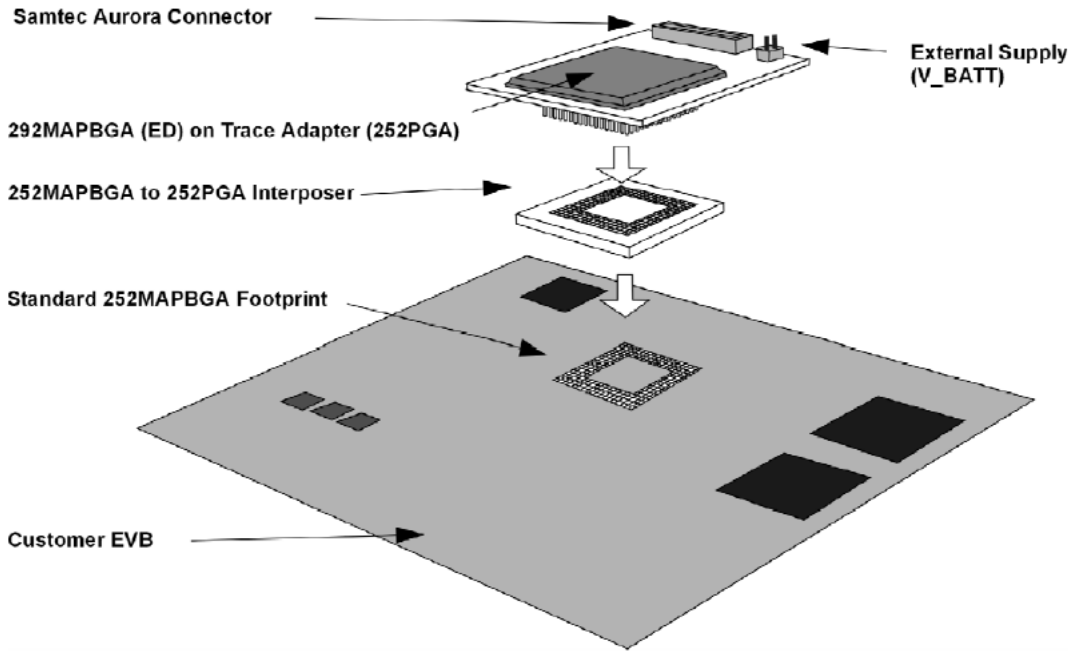


Figure 20. 292MAPBGApackage into a 252BGA footprint

9 ADC and Analog

9.1 Overview

MPC5746R includes seven separate Analog-to-Digital converters (ADC) and associated support modules:

- Four independent 12-bit Successive-Approximation-Register (SAR) ADCs
- Three independent 16-bit Sigma-Delta (SD) ADCs
- Two Decimation Filter blocks
- ADC Cross-Triggering Unit (BCTU)

These ADCs interface a various number of analog input pins depending on whether the 252 MAPBGA, the 176 LQFP package, or the 144 LQFP package is selected for the design. Both the SAR and SD ADCs have their own power supply and references. Please refer to the Power Supply section for information on how to connect these signals and for specific details of the analog pins available in each package.

A diagram of the ADC system in MPC5746R is shown in Figure 21.

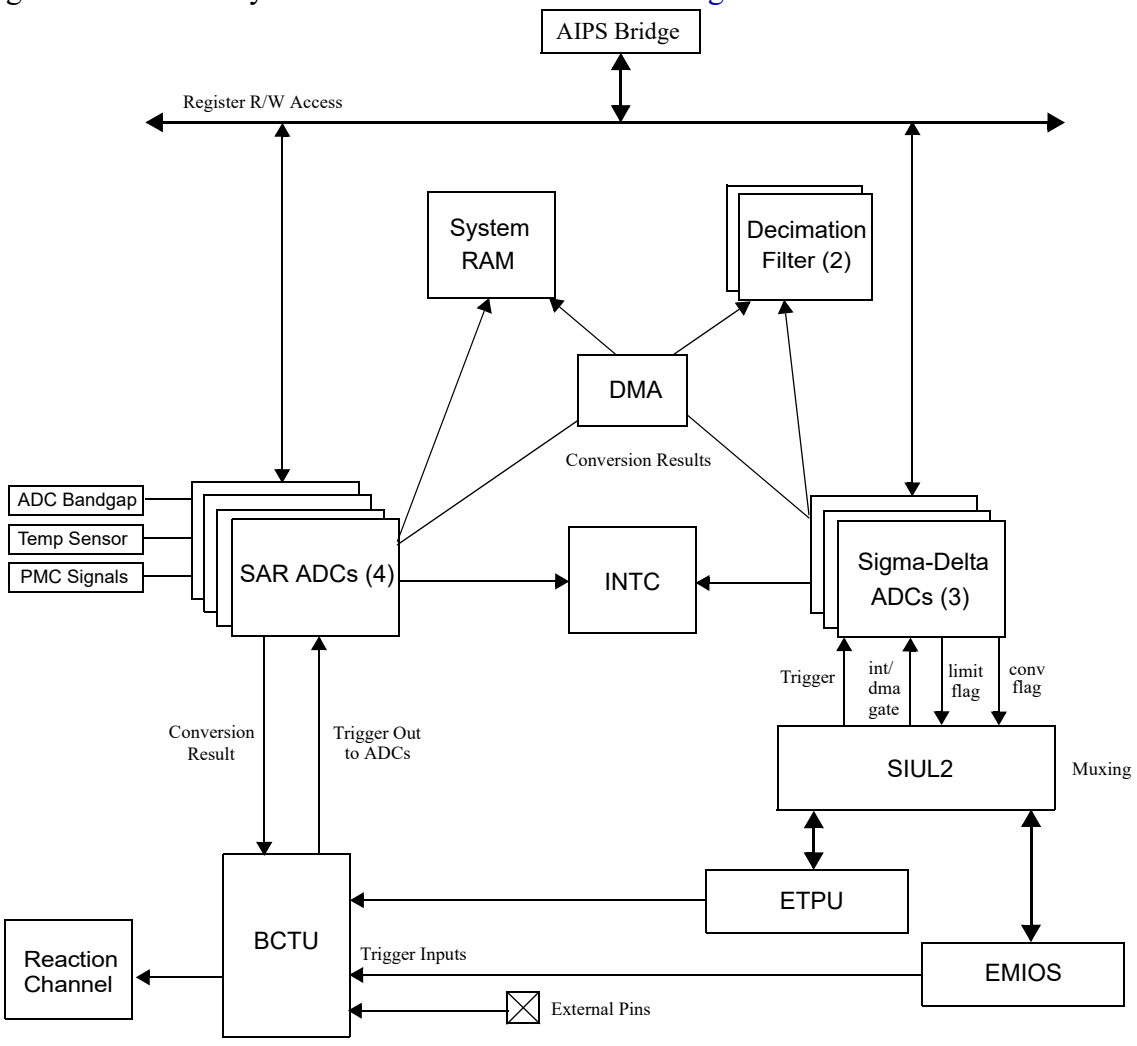


Figure 21. MPC5746R ADC Subsystem

9.2 Analog supply configuration

The following diagram illustrates the full SD/SAR ADC supply configuration with external components.

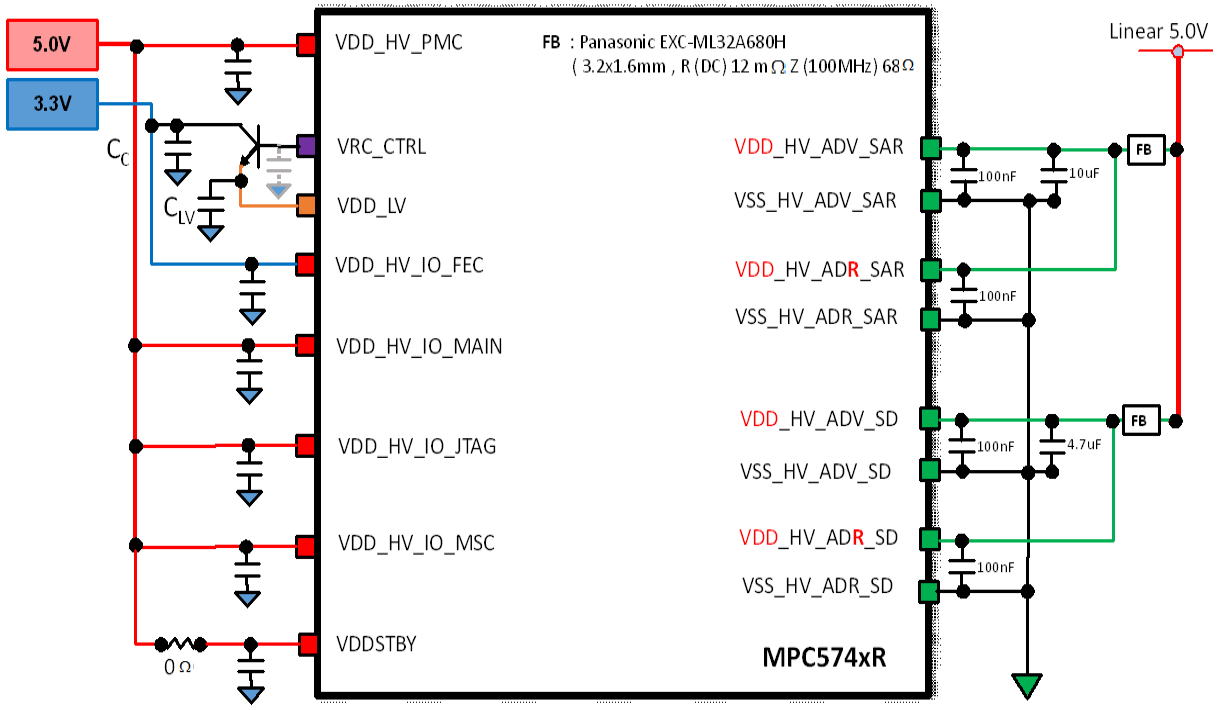


Figure 22. SD/SAR ADC supply configuration

Ferrite beads are used to isolate noise induced from the digital supply domain. Each pair of ADC supplies must have a 100 nF filtering capacitor and should be populated at the pin. NXP recommends a separate linear stable supply for the ADC analog domain to avoid noises from digital supply domain.

The following board schematic and layout guidelines should be followed:

- Isolate the analog power supplies (VDDA) from digital power supplies (see Analog supply configuration)
- Isolate analog traces from digital high-frequency traces
- Incorporate robust bypassing of power supplies (analog and digital supplies) to ensure lowest possible voltage ripple on the power supplies
- Use linear power supplies when possible, or minimize or isolate the switching noise when using a switching power supply
- Incorporate low-pass filter on ADC inputs to remove unwanted higher frequency components as shown in the following sections

User can select either 3.3 V or 5 V for the SD/SAR ADC reference supply. Refer to the MPC5746R Data Sheet for ADC characteristics with different reference supply.

9.3 SAR ADC

This section describes the various features and configurations of the SAR ADC. Refer to “AN4881 - SAR ADC Implementation and Use”, “AN5032 - Ref Circuit Design for SAR ADC” (available at www.nxp.com) and the MPC5746R Reference Manual for additional information.

9.3.1 External circuitry for SAR ADC analog input

Figure 23 shows the typical circuitry for the analog input channel with filtering components. NXP recommends checking the ADC performance on silicon to get optimal R and C values. The SAR ADC supports a maximum sampling frequency of 1 MHz (total conversion time of 1us). The maximum allowed input frequency is 125 kHz. Refer to the MPC5746R Data Sheet for additional information on internal circuitry, minimum sample time and minimum conversion time etc.

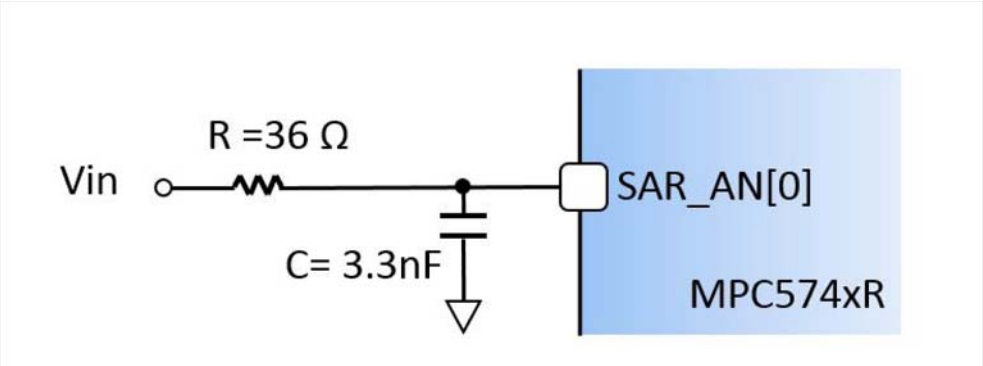


Figure 23. SAR ADC external circuitry example

9.3.2 Input Multiplexing

SAR ADC3 supports 4 external multiplexers, with 8 inputs each. None of the other ADCs support external multiplexers. Table 18 provides the address mapping for the SAR ADC3 multiplexed channels.

Table 18. Channel and External Mux Mapping

Channel	External Mux Input	External Mux Address (binary)
64	PX[5]	000
65		001
66		010
67		011
68		100
69		101
70		110
71		111

Table 18. Channel and External Mux Mapping

Channel	External Mux Input	External Mux Address (binary)
72	PX[6]	000
73		001
74		010
75		011
76		100
77		101
78		110
79		111
80	PX[7]	000
81		001
82		010
83		011
84		100
85		101
86		110
87		111
88	PX[8]	000
89		001
90		010
91		011
92		100
93		101
94		110
95		111

9.4 Sigma Delta ADC

MPC5746R has 3 Sigma Delta Analog-to-Digital Converter (SDADC) modules. The SDADC consists of a cascaded sigma delta modulator coupled to a high pass filter and digital interface to the system bus. Both single ended and differential conversions are supported on a number of input channels. Conversions can be started by software or hardware triggers.

9.4.1 Differential and Single ended operation

Each SD ADC has up to eight inputs that may be configured as single ended channels or as up to four differential channel pairs. The differential pairs are grouped as follows and as shown in Figure 24:

- AN[0] (+) and AN[1] (–)

- AN[2] (+) and AN[3] (–)
- AN[4] (+) and AN[5] (–)
- AN[6] (+) and AN[7] (–)

Refer to the MPC5746R Reference Manual for complete details about configuring the SD ADC external channels.

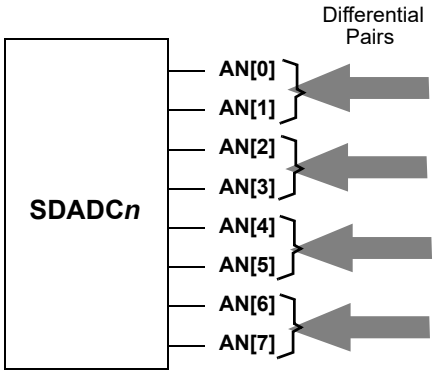


Figure 24. SD ADC Differential/Single Ended Configuration

9.4.2 External circuitry for single ended channel

Figure 25 shows the typical circuitry for a single ended SDADC channel with the filtering components.

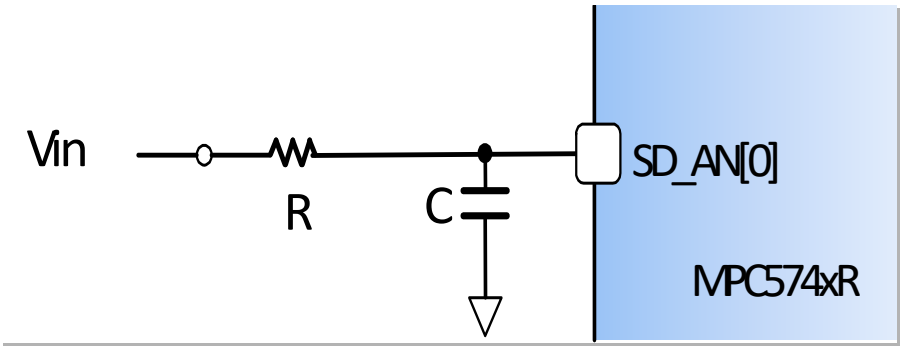


Figure 25. Single ended SDADC external circuitry example

For the anti-aliasing filter, the minimum C is 220 pF and maximum R is 20 KΩ. R & C values should be chosen such that the filter pole (1/(2×π×R×C)) satisfies the following two conditions

- It needs to be placed above the maximum frequency of the input signal (up to 100 KHz) in order to minimize input signal attenuation
- It needs to be placed at or below the SDADC sampling clock frequency minus the input signal bandwidth in order to avoid aliasing (sampling clock is half the SDADC clock, min 4 MHz / 2 = 2 MHz)

Figure 26 shows an example of differential SDADC channels with filtering components. Inputs need to be 180 degrees out of phase and in the 10 Hz - 100 kHz range.

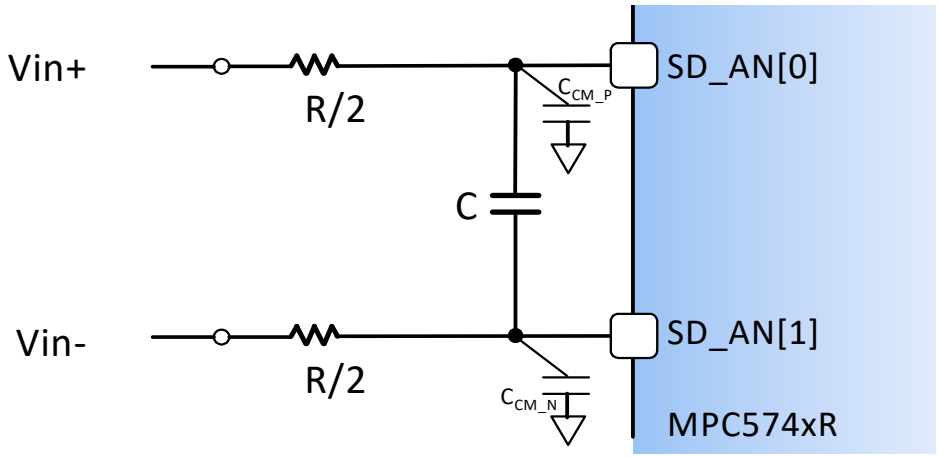


Figure 26. Differential channel SDADC external circuitry example, R=8 kΩ C=250 pF

NOTE

The external common mode voltage of the differential signals should be VDD_HV_ADR_SD/2. Depending on the system noise levels, the user can install C_{CM_P} / C_{CM_N} to improve the external common mode noise. As a rule of thumb, the capacitor value should be less than or equal to the filter capacitor C/10.

The guidelines that need to be followed when designing the external circuitry for the MPC5746R SDADC differential channels

- The internal common-mode voltage for the MPC5746R SD is VDD_HV_ADR/2 and is set by the bias generator.
- External C_{CM_P}/C_{CM_N} capacitors filter external common-mode noise.
- External C_{CM_P}/C_{CM_N} have 2^{nd} order effect on the filter pole. Without external common-mode filter caps, user have to rely on common-mode noise rejection of the ADC.
- External C_{CM_P}/C_{CM_N} should be $1/10^{th}$ or less than the value of C filter.
- External C_{CM_P}/C_{CM_N} is ideally connected to V_{CM} (VDD_HV_ADR/2), but can be connected to ground (VSSA).

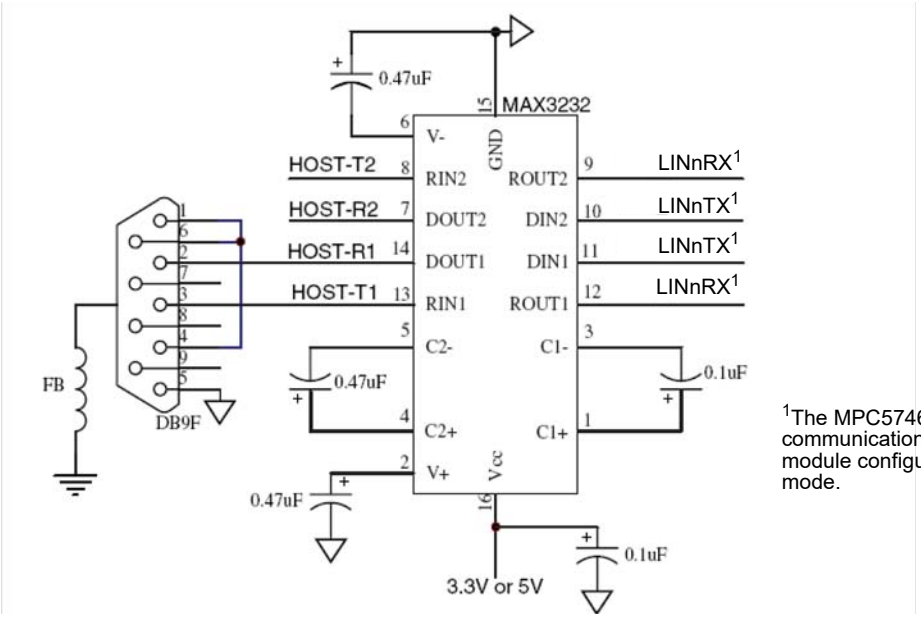
10 Example Communication Peripheral connections

There are a wide range of peripheral pins available on MPC5746R. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, and RS-232 communication interfaces.

10.1 Example RS232 interface

The RS-232 (TIA/EIA-232-F) standard is a common interface once available on most computers. Adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB.

Figure 27 and Table 19 show the typical connections between the serial port of MPC5746R and the MAX3232-EP RS-232D transceiver from Texas Instruments. The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.



[1]The MPC5746R supports RS-232 communication using the LinFLEX module configured to operate in UART mode.

Figure 27. Typical SCI to RS232 Circuit

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature of –40 to +125° C and is not intended for automotive applications. This device should not be used in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore, the commercial device can be used for prototyping purposes. Texas Instruments offers a device option with an operating temperature range of –40 to +85° C and an enhanced version of the device, MAX3232-EP, that is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of –55 to +125° C.

See Table 19 for a list of the typical RS232-D connector pin assignments.

Table 19. Typical RS232-D Connections

Pin	Description
1	Connect to pin 4 and 6
2	RS-232 TX (Transmit)
3	RS-232 RX (Receive)
4	Connect to pin 1 and 6
5	GND
6	Connect to pin 1 and 4
7	N/C
8	N/C
9	N/C

NOTE

N/C pins are not connected. The shell of the connector should be connected through a ferrite bead to ground.

10.2 Example LIN interface

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 28 shows a typical interface implemented using the NXP MC33661 LIN transceiver.

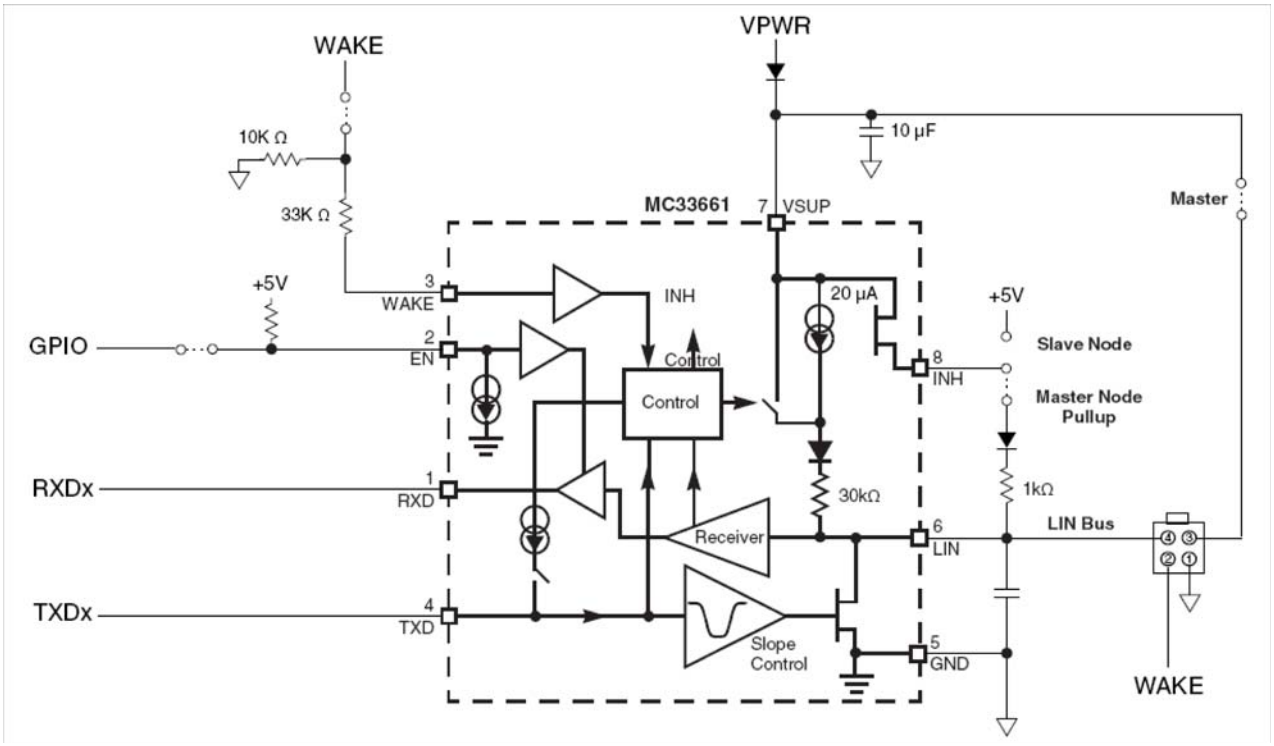


Figure 28. Typical LIN connections

Table 20 below shows the pins of the MC33661 and their typical connections to a MCU.

Table 20. MC33661 Pin Definitions and Example System Connections

Pin Number	Pin Name	Pin Direction	Full Pin Name	MCU or System Connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN receive data output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enable operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Enables the device out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN transmit data input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/Output	LIN Bus	LIN Bus	Bi-directional pin that represents the single-wire transmit and receive.
7	VSUP	Input	Power Supply	Protected Battery Voltage	Device power supply, typically connected to a nominal 12 V supply.

Table 20. MC33661 Pin Definitions and Example System Connections

Pin Number	Pin Name	Pin Direction	Full Pin Name	MCU or System Connection	Description
8	INH	Output	Inhibit Output	LIN Bus (if master)	The inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus or master nodes.

[1] WAKE is an optional signal on the LIN connector, but may come directly from a switch.

There is not a standard industry-defined LIN connector. NXP uses a 4-pin Molex© connector that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. Table 21 shows the NXP pin-out.

Table 21. LIN Connector Pinout Recommendation

Function	Pin Number	Pin Number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN bus – single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- VPWR – can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake – typically used for each individual slave node to enable the LIN physical interface of that node and to consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, to turn on the MCU that controls a function inside the vehicle, such as powering a smart dome light or enabling the controls of a smart seat.
- Ground – ground reference for the module.

Part numbers for the 4-pin Molex connector are shown in Table 22.

Table 22. Recommended Connector Part Numbers

Description	Manufacturer Part Number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-29-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts	39-29-5043

10.3 CAN interface circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

MPC5746R incorporates 4 CAN modules on-chip. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pull-up resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed. The MPC5746R CAN modules conform to CAN protocol specification version 2.0B protocol. The transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 kbit/s to 125 kbit/s) or a high speed (250 kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

NXP includes high speed CAN physical interfaces in some System Basis Chip (SBC) devices that can be used to provide the CAN physical interface and the device power supply. Refer to the MC33908 Data Sheet for more information. Some of these devices include a LIN physical interface. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 23. NXP CAN Transceivers

	Device			
	TJA1050	**TJA1054**	**TJA1040**	**TJA1041**
Bitrate (kbit/s)	1000	125	1000	1000
Modes of Operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

10.3.1 High-speed CAN TJA1050 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

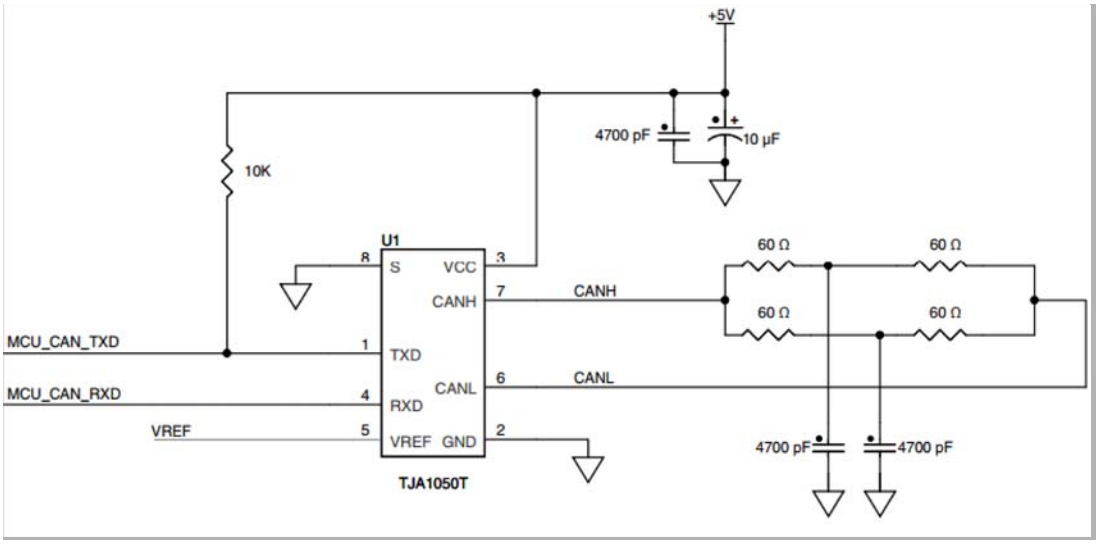


Figure 29. Typical high-speed CAN circuit using TJA1050

NOTE

Decoupling shown as an example only. TXD/RXD pull-up/pull-down may be required, depending on device implementation.

The table below as describes the TJA1050 pin and system connections.

Table 24. TJA1050 Pin Definitions and System Connections

Pin	Name	Direction	Full Pin Name	Connection	Description
1	TXD	Input	Transmit data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VCC	Input	–	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN bus low	CAN bus connector	CAN bus low pin
7	CANH	Input/Output	CAN bus high	CAN bus connector	CAN bus high pin
8	$\overline{S}$	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in the case of an error condition.

10.3.2 Low-speed CAN TJA1054 interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

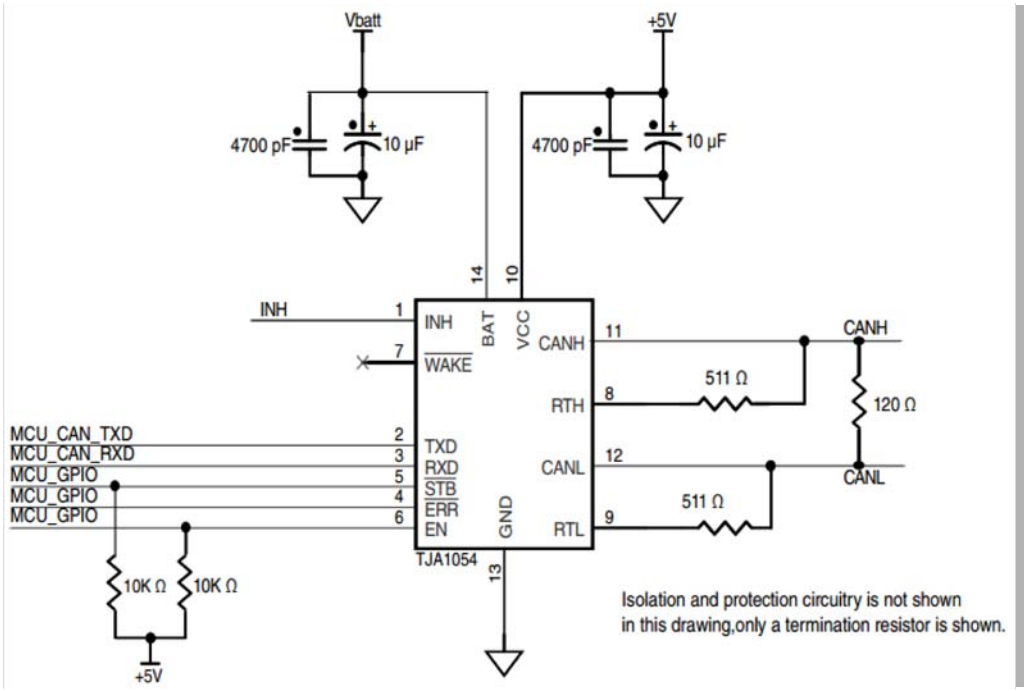


Figure 30. Typical low-speed CAN circuit using TJA1054

NOTE

Decoupling shown as an example only. STB and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 25. TJA1054 Pin Definitions and System Connections

Pin	Name	Direction	Full Pin Name	Connection	Description
1	INH	Input	Inhibit	Typically not connected.	Inhibit output for control for an external power supply regulator if a wake up occurs.
2	TXD	Input	Transmit data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive data	MCU CAN RXD	CAN receive data output to the MCU
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake up is detected in Standby or Sleep modes.

Table 25. TJA1054 Pin Definitions and System Connections

Pin	Name	Direction	Full Pin Name	Connection	Description
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected.	Wake input (active low), both falling and rising edges are detected.
8	RTH	Input	Termination resistor high	Resistor to CANH	Termination resistor for the CAN bus high
9	RTL	Input	Termination resistor low	Resistor to CANL	Termination resistor for the CAN bus low
10	VCC	Input	Voltage supply	5 V	DIgital IO supply voltage, 5 V
11	CANH	Output	CAN bus high	CAN bus connector	CAN bus high pin
12	CANL	Input/output	CAN bus low	CAN bus connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

10.3.3 Recommended CAN connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket (female) is used on the evaluation board and a cable with a connector (male) connects with it.

Figure 31. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 26. DB-9 Signal Mapping

Pin Number	Signal Name
1	N/C
2	CAN_L
3	GND
4	N/C

Table 26. DB-9 Signal Mapping

Pin Number	Signal Name
5	CAN_SHEILD (optional)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (optional)

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

10.4 Zipwire interface

The Zipwire interface is intended to be used to communicate between two nodes implemented on a single board. The interface uses a “low speed” reference clock that is shared between the two nodes. A single-ended 10 to 26[1] MHz reference clock is used to generate the Zipwire high speed operation of approximately 320 MHz. A termination resistor is required at the receiving end of the clock for best performance of the interface. The value of the resistor depends on the board layout and impedance.

The data signals use a low voltage differential signaling (LVDS) that is internally terminated on the MCU.

The following diagram shows the connection between two devices.

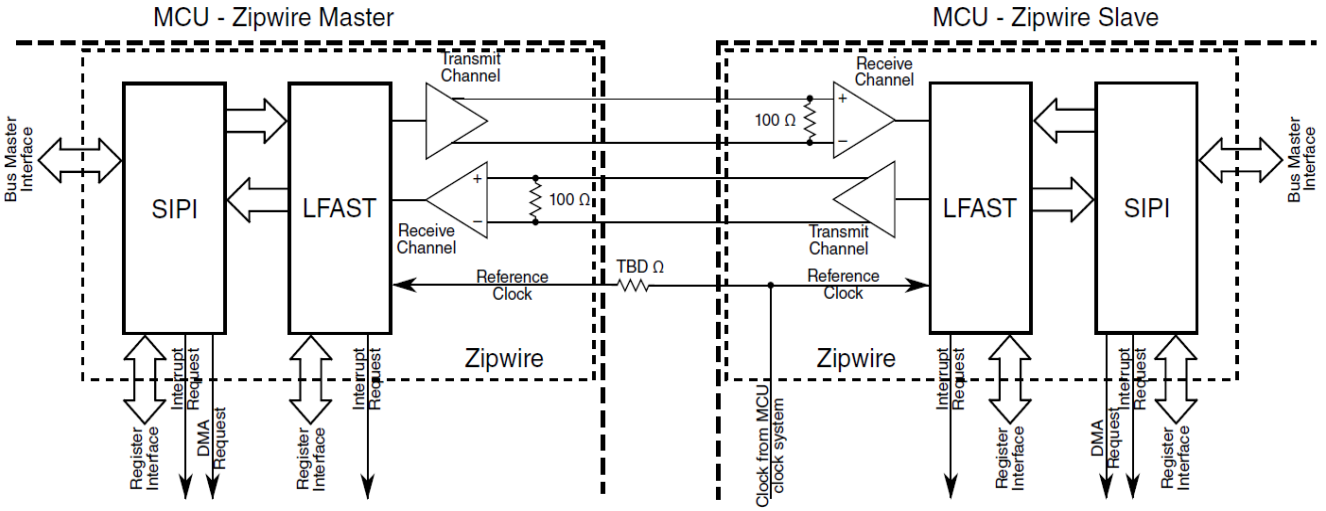


Figure 32. Typical Zipwire hardware interface

The Zipwire interface is a high-speed interface, therefore care should be taken in laying out the signals on a printed circuit board. The following guidelines are suggested.

1. 20 MHz is the most commonly used frequency, 10 MHz can also be used. 26 MHz is not recommended.

- A controlled impedance PCB is required for the LVDS signals.
- The differential LVDS + and – pair should be routed parallel and close to each other. The length of the + and - pairs should be matched to less than 0.1 inches of difference.
- The LVDS transmit pairs length is not required to be same length as the LVDS receiver pair.
- The differential pair should be routed with a maximum of two vias. Ideally, the differential pair should be routed without vias on a single plane of the board preferably on the top or bottom plane of the board. However, due to pin escape issues with the placement of the high speed signals on the surface mounted devices, routing on a single layer is usually not possible.
- Keep necking of the signal to less than 0.01 inch to avoid discontinuities. Some necking is usually required in escaping the signals for the BGA or LQFP signal feeds to other layers on the board.
- The differential pair must be routed on a layer that is one dielectric away from ground.
- A connector is not recommended for the Zipwire interface, but if a connector is used, a high speed connector system, such as the Samtec ERF8 0.8 mm Edge Rate Rugged High Speed Socket, should be used with twin-ax cabling. The odd side of the connector should be placed parallel and nearest to the MCU package on the board to allow direct connection to the package signals.

10.5 Ethernet interface

Ethernet is a communication technology that was originally developed for creating local area networks (LANs) between computers. Over time, it has become the standard wired communications network for the PC and is widely used within telecommunications and industrial applications. In recent years, Ethernet has found its way into automotive electronics with deployment in diagnostic and camera applications.

The Fast Ethernet Controller (FEC) implemented on the MPC5746R devices is a communication controller that supports 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the connection to the physical interface. The figure below shows a typical set up of the complete interface to the network. Here a TJA1100 from NXP is used as the Ethernet physical interface (PHY).

The following figure illustrates the Ethernet configuration of MCU to Ethernet connector.

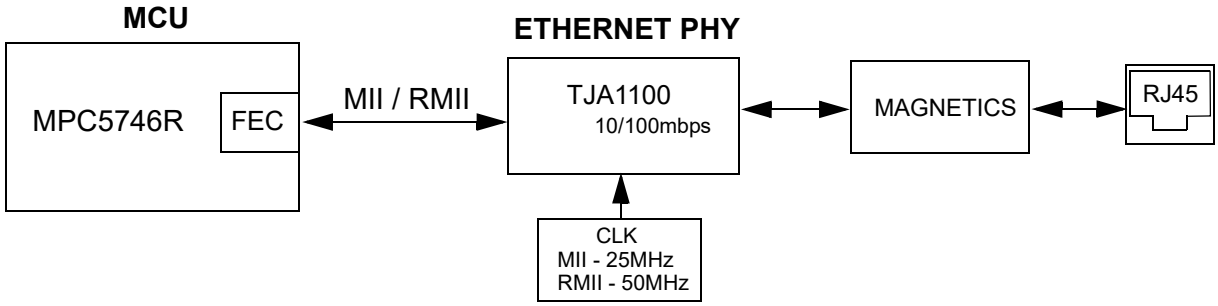


Figure 33. Ethernet application configuration example

NOTE

In MPC5746R, Serial Management Interface FEC_MDIO/FEC_MDC pins are internally tied up to VDD_HV_IO_MAIN supply domain, which is usually 5 V. Therefore the user must use a bidirectional level shifter on the MDIO/MDC pins. Refer the MPC5746R Errata for more information.

As shown in Figure 33, the FEC can interface to a PHY using the 10/100 Mbit/s MII-Lite, RMII or the 10 Mbit/s only 7-wire interface. The FEC signals from the MCU take their voltage level from the VDD_HV_IO_FEC supply domain. Most PHYs require signals in the 3.3 V range, so the VDD_HV_IO_FEC should be set accordingly. The FEC signals are summarized in Table 27 and their use in each interface type is highlighted. Note that the signals required by different PHYs will vary in some cases for each interface option; see the Data Sheet for your selected PHY.

Table 27. FEC Signal Overview

Signal Name	Description	Direction	MII	RMII	7-Wire	Port
FEC_COL[1]	Collision Detection	I	Required	Option	Required	PC[5]
FEC_REF_CLK	RMII Reference Clock Output	O	N/A	Required	N/A	PC[0]
FEC_MDC	Management Data Clock	O	Required	N/A	N/A	PD[8]
FEC_MDIO	Management Data Output	I/O	Required	N/A	N/A	PD[13]
FEC_RXCLK	Receive Clock	I	Required	N/A	Required	PC[12]
FEC_RXDV[2]	Receive Data Valid	I	Required	Required	N/A	PC[13]
	Carrier Sense[1]	I	Required	Required	N/A	
FEC_RXD0	Receive Data 0	I	Required	Required	Required	PC[7]
FEC_RXD1	Receive Data 1	I	Required	Required	N/A	PC[8]
FEC_RXD2	Receive Data 2	I	Required	N/A	N/A	PC[9]
FEC_RXD3	Receive Data 3	I	Required	N/A	N/A	PC[10]
FEC_RXER[1]	Receive Error	I	Option	Option	N/A	PC[11]
FEC_TXCLK	Transmit Clock	I	Required	N/A	Required	PC[1]
FEC_TXD0	Transmit Data 0	O	Required	Required	Required	PC[6]
FEC_TXD1	Transmit Data 1	O	Required	Required	N/A	PC[5]
FEC_TXD2	Transmit Data 2	O	Required	N/A	N/A	PC[4]
FEC_TXD3	Transmit Data 3	O	Required	N/A	N/A	PC[3]
FEC_TXEN	Transmit Enable	O	Required	Required	Required	PC[2]

1 This signal is not available in the MII-Lite interface

2 FEC_RXDV in RMII mode generates RXDV and CRS.

11 References

More information can be found in the documents listed in the table below. All of these documents are available on the NXP web site (http://www.nxp.com).

Document	Title
Data Sheet	MPC5746R Data Sheet Rev 4.
Reference Manual	MPC5746R Reference Manual Rev 6.
Errata	MPC5746R Errata for Mask Set 1N83M Rev2.4
AN4731	Understanding the Injection Current on Freescale Automotive Microcontrollers
AN5134	Introduction to Zipwire Interface
AN5181	Introduction to the MPC5746R Trace Adapter
AN4881	SAR Implementation and Use
AN5032	Ref Circuit Design for SAR ADC

12 Revision History

Table 28. Revision history

Revision	Date	Changes
0	06/2016	Initial release
1	07/2019	Added information related to the change in the name of Transistor from “ROHM 2SCR574D A07“ to “ROHM 2SCR574D3 A07” in Table 7 and Figure 4.

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