A Low Power 1Mbit MRAM based based on 1T1MTJ Bit Cell Integrated with Copper Interconnects

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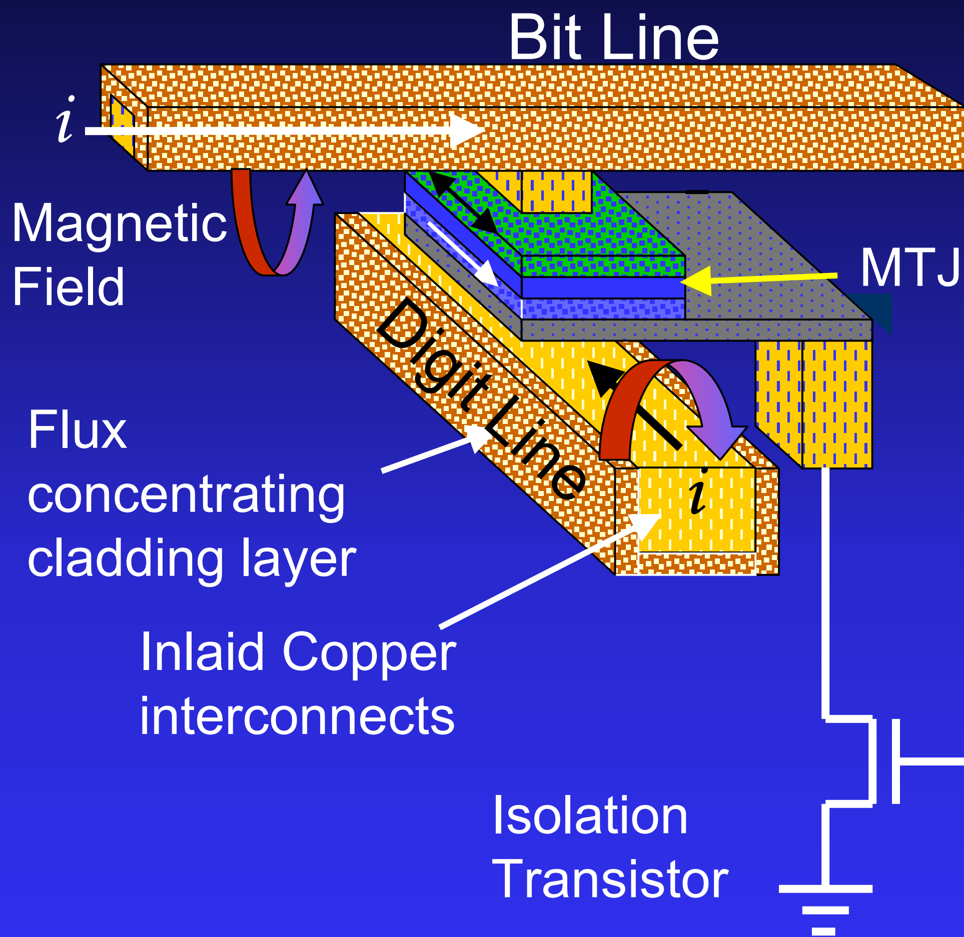
Outline

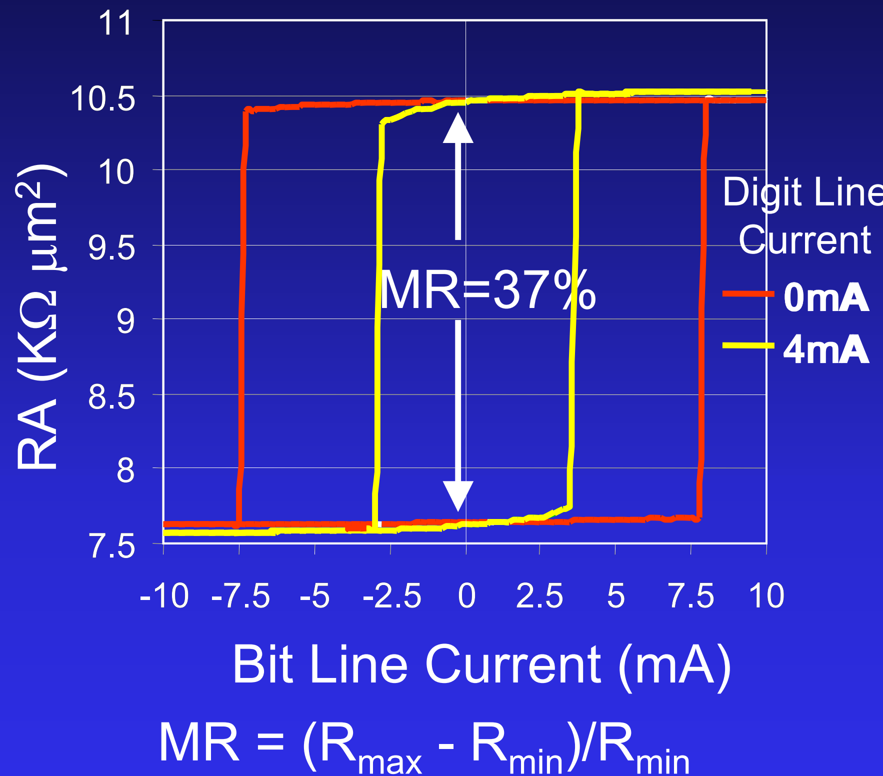
- Overview of MRAM Technology
  - Attributes and operation principle
- 1Mb MRAM process
  - Cu metal interconnect
  - Magnetic Cladding
- 1Mb circuit
  - Memory organization
  - Reference cell
  - Read circuitry
- Summary

MRAM Attributes

- **MRAM** offers multiple memory capabilities that are currently realized by separate memories.
    - **Non-Volatility of Flash** with fast programming, no program endurance limitation, and byte programmable
    - **Density competitive with DRAM** with no refresh refresh
    - **Speed competitive with SRAM** (except the fastest) at fraction of the cell size
    - Nondestructive read
    - Immunity of bits to soft error

Memory Cell - 1Transistor 1Magnetic Tunnel Junction (MTJ)

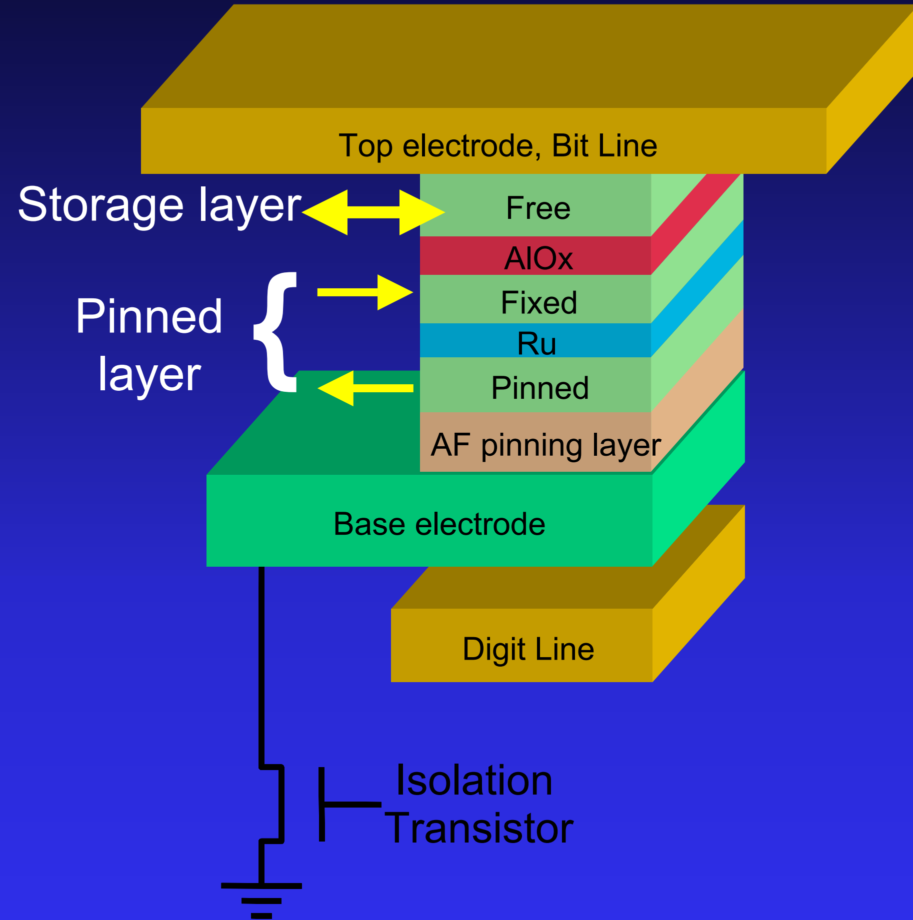




$MR = (R_{max} - R_{min})/R_{min}$

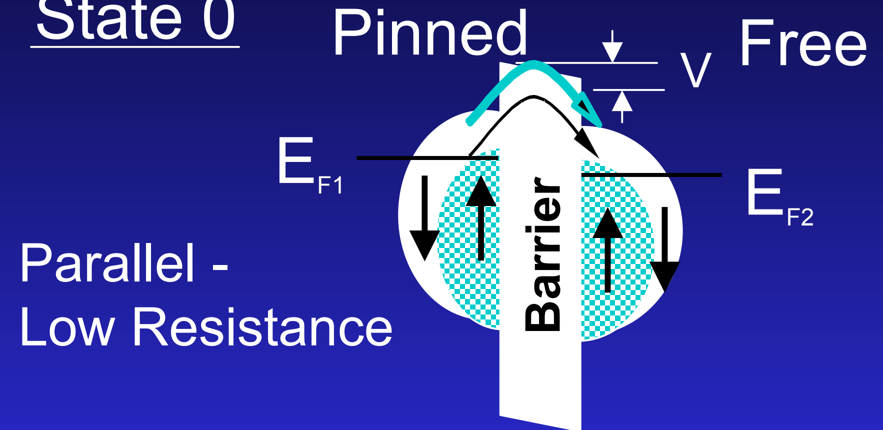
Tunneling Magnetoresistance

MTJ Material Structure



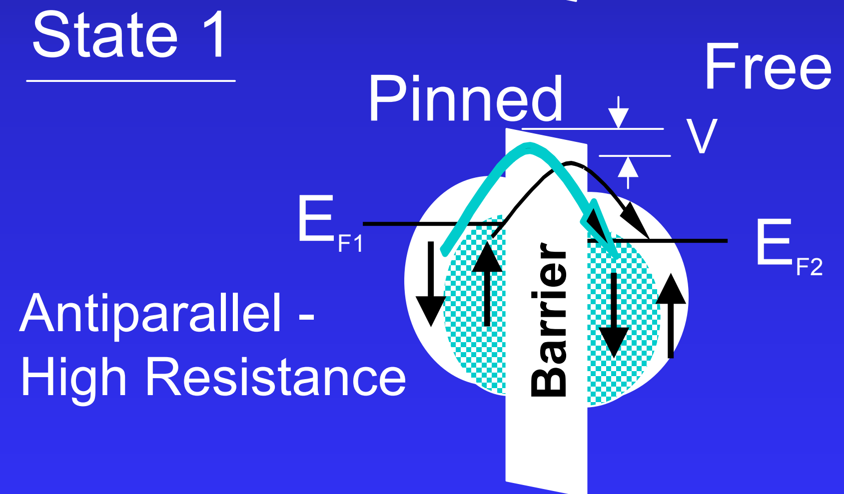
Spin Dependent Tunneling

State 0



Parallel - Low Resistance

State 1



Antiparallel - High Resistance

Tunneling Magnetoresistance

Across wafer uniformity - 200 mm

	11.3	11.0	10.5	10.5	10.9	12.3	
11.7	10.3	9.74	9.88	9.65	9.80	10.2	11.5
10.3	9.54	10.9	10.6		10.3	9.74	10.5
10.1	9.68	10.4	10.8	10.8	10.7	9.85	10.7
	9.80	10.9	10.5	10.8	10.5	9.86	10.2
10.3	9.45	10.1	10.4	10.6	9.87	9.62	10.9
	10.2	9.52	9.43	9.56	9.59	10.2	
		11.2	10.2	10.4	11.0		

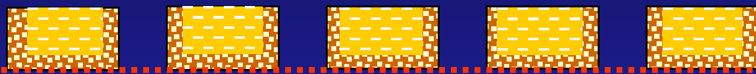
RA=10.4 kΩ-μm^2, σ=6%

	43.9	44.5	44.6	44.8	44.5	43.1	
44.4	45.0	45.2	46.0	45.8	46.0	44.6	43.1
44.1	45.4	42.9	45.6		45.6	45.8	44.5
44.5	46.1	44.3	45.1	45.5	45.8	46.0	45.0
44.5	45.8	43.4	45.4	45.9	45.7	45.9	44.7
44.2	45.3	45.7	45.5	43.9	45.8	45.4	44.0
	44.1	45.3	45.9	45.6	45.0	44.7	
		43.4	44.0	44.8	44.1		

MR=45%, σ=2%

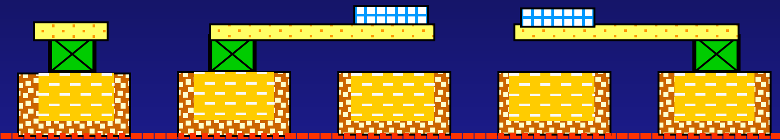
Process Flow

1st MRAM Module Flow



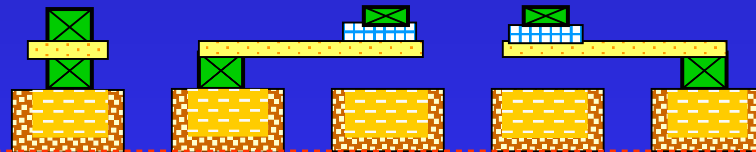
Pattern inlaid copper program lines with permeable cladding.

2nd MRAM Module Flow



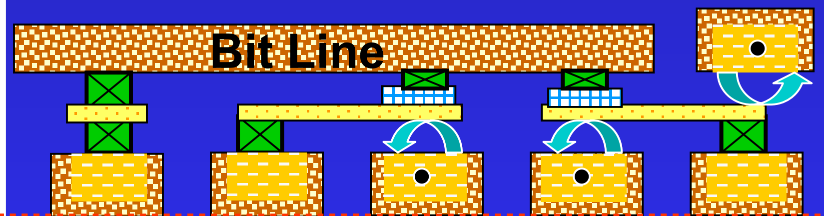
Deposit ILD, form via connection to bottom electrode, deposit, and and pattern MTJ stack.

3rd MRAM Module Flow



Deposit ILD, pattern via for connection to top electrode

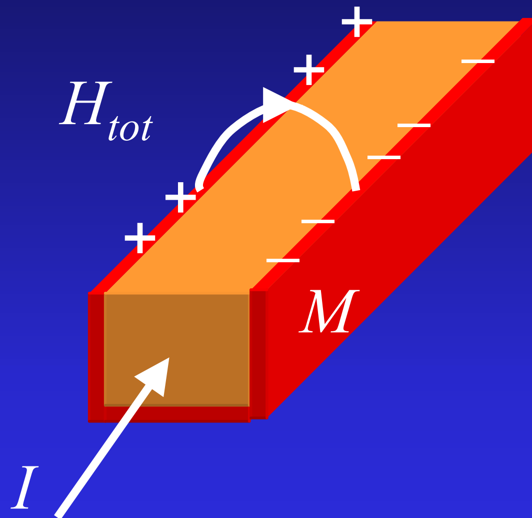
4th

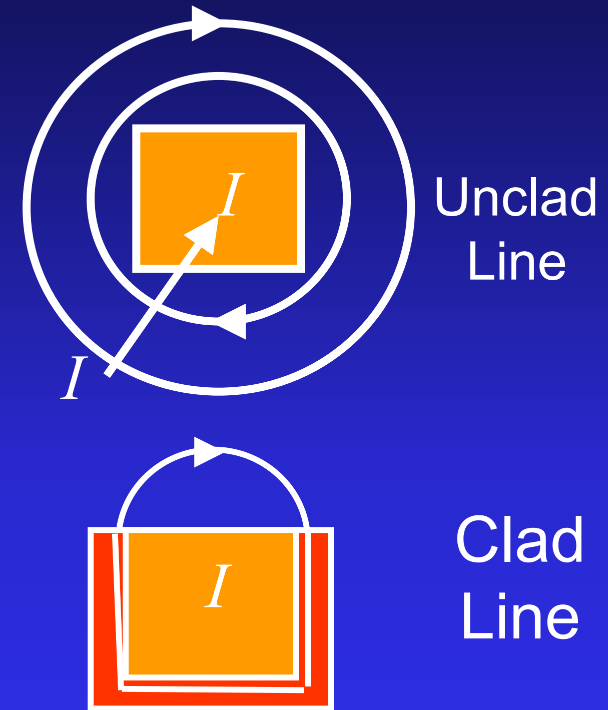


Pattern inlaid copper program line with permeable cladding.

Field Enhancement from Magnetic Cladding

• Magnetic film surrounding conductor doubles field *H* for a given current *I*.

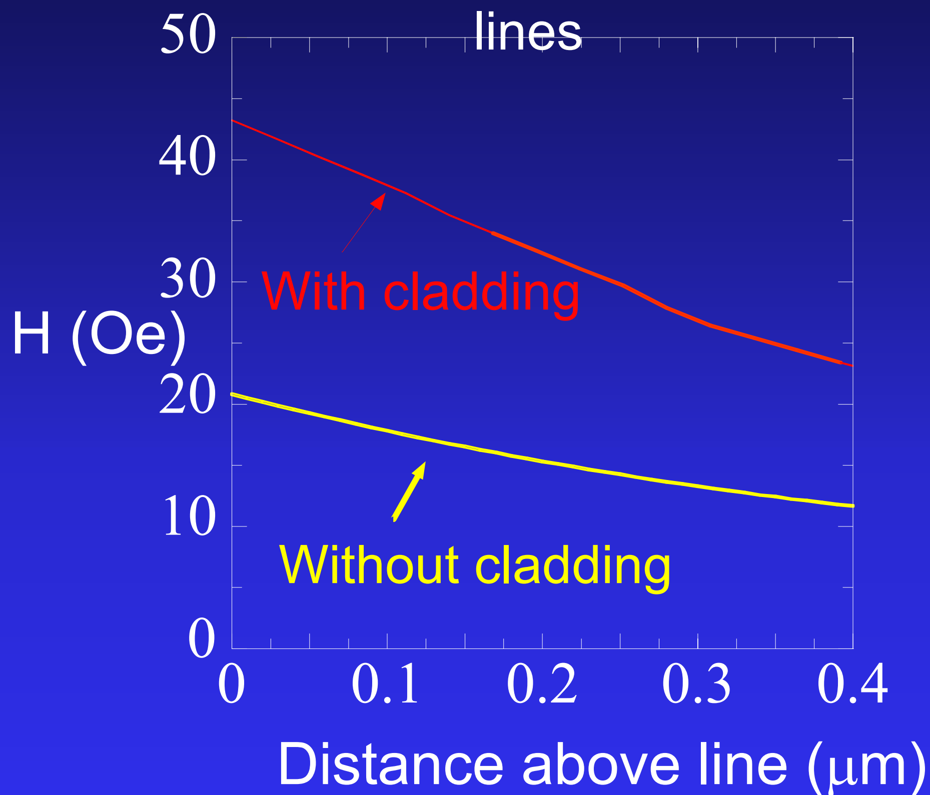


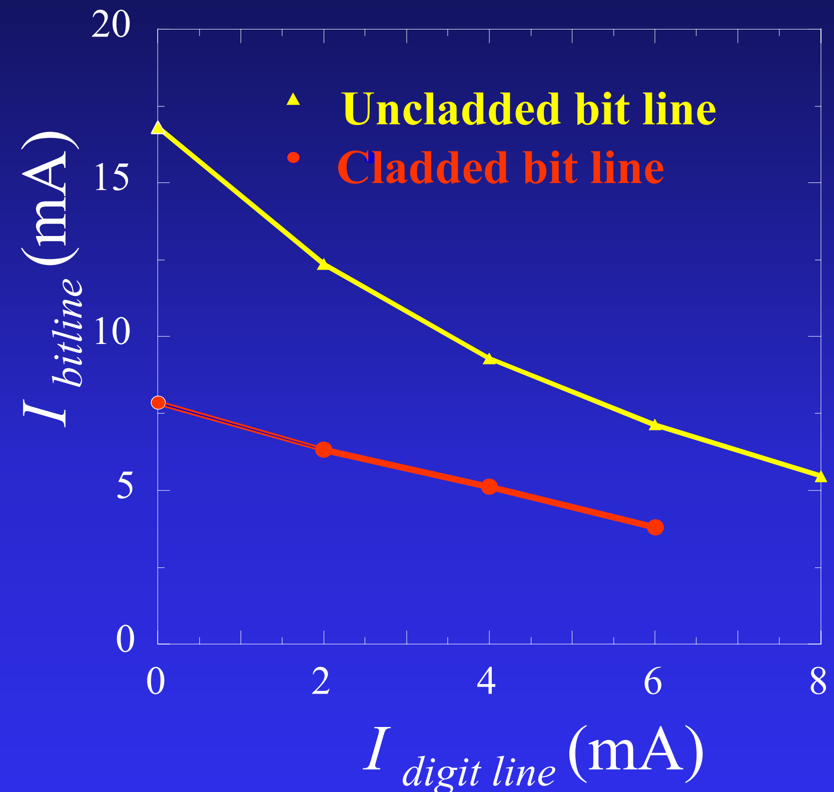


$$H_{unclad} \approx \frac{I}{2w} \qquad H_{clad} \approx \frac{I}{w}$$

• Cladding concentrates field to top of digit line

Field enhancement from cladding cladding





- Factor of 2 field enhancement calculated and observed

1Mb MRAM Architecture

Current/Source or Sink
16
Current Switch
BL 0-511

Row Pre-Decode

Current/Source or Sink
16
Current Switch
BL 511-0

Ground Switch
GL0
GL511
Current Sink
DL0
DL1023

MRAM Array
512 columns
1024 Rows
16 Ref. Columns

0 0
Digit Line Row Select
1023 1023

MRAM Array
512 columns
1024 Rows
16 Ref. Columns

DL0
DL1023
Current Sink
GL0
GL511
Ground Switch

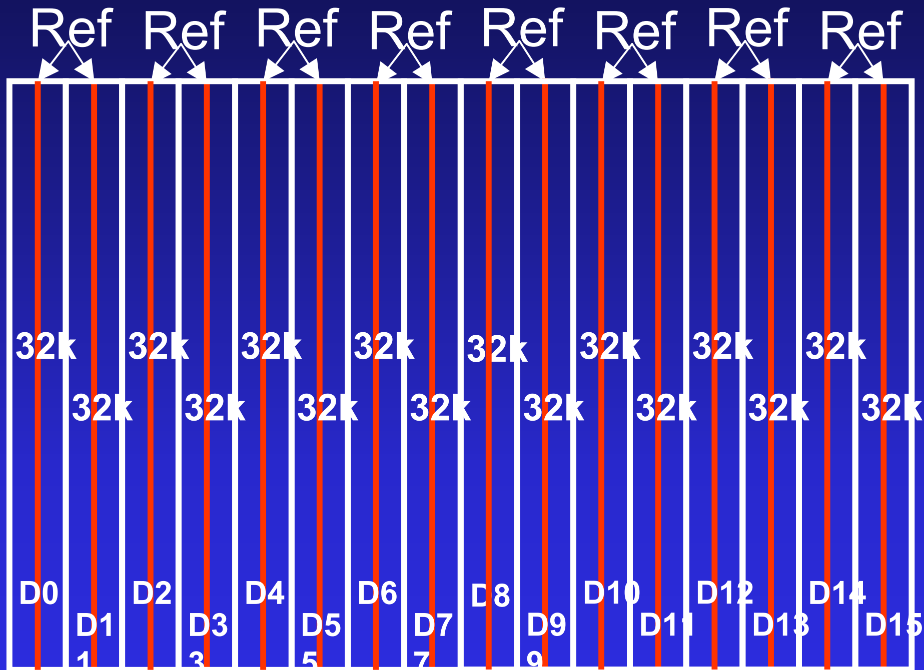
Column Select
16
Current/Source or Sink
16
Read Circuit
dq0 dq15

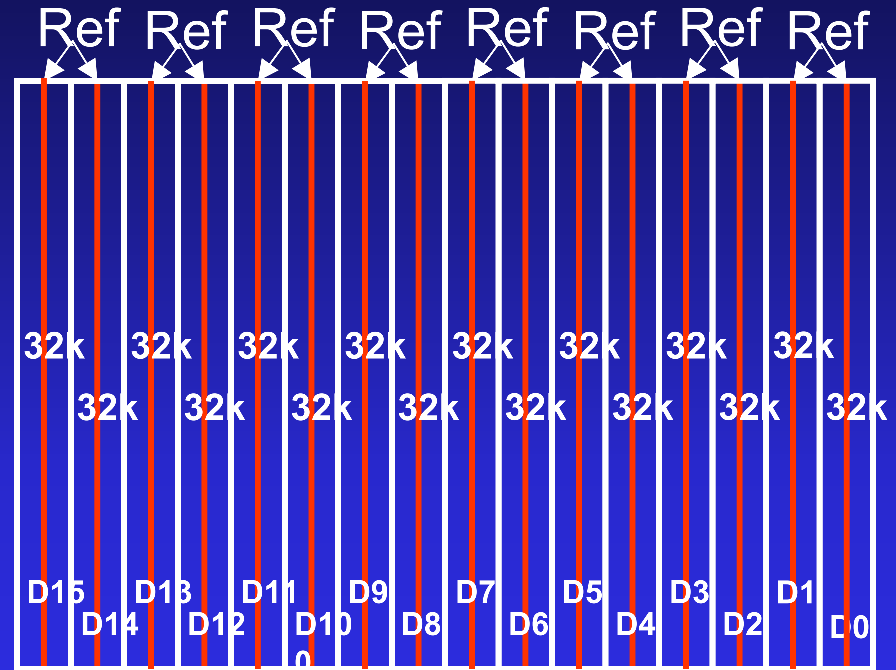
Current Source A

Column Select
16
Current/Source or Sink
16
Read Circuit
dq15 dq0

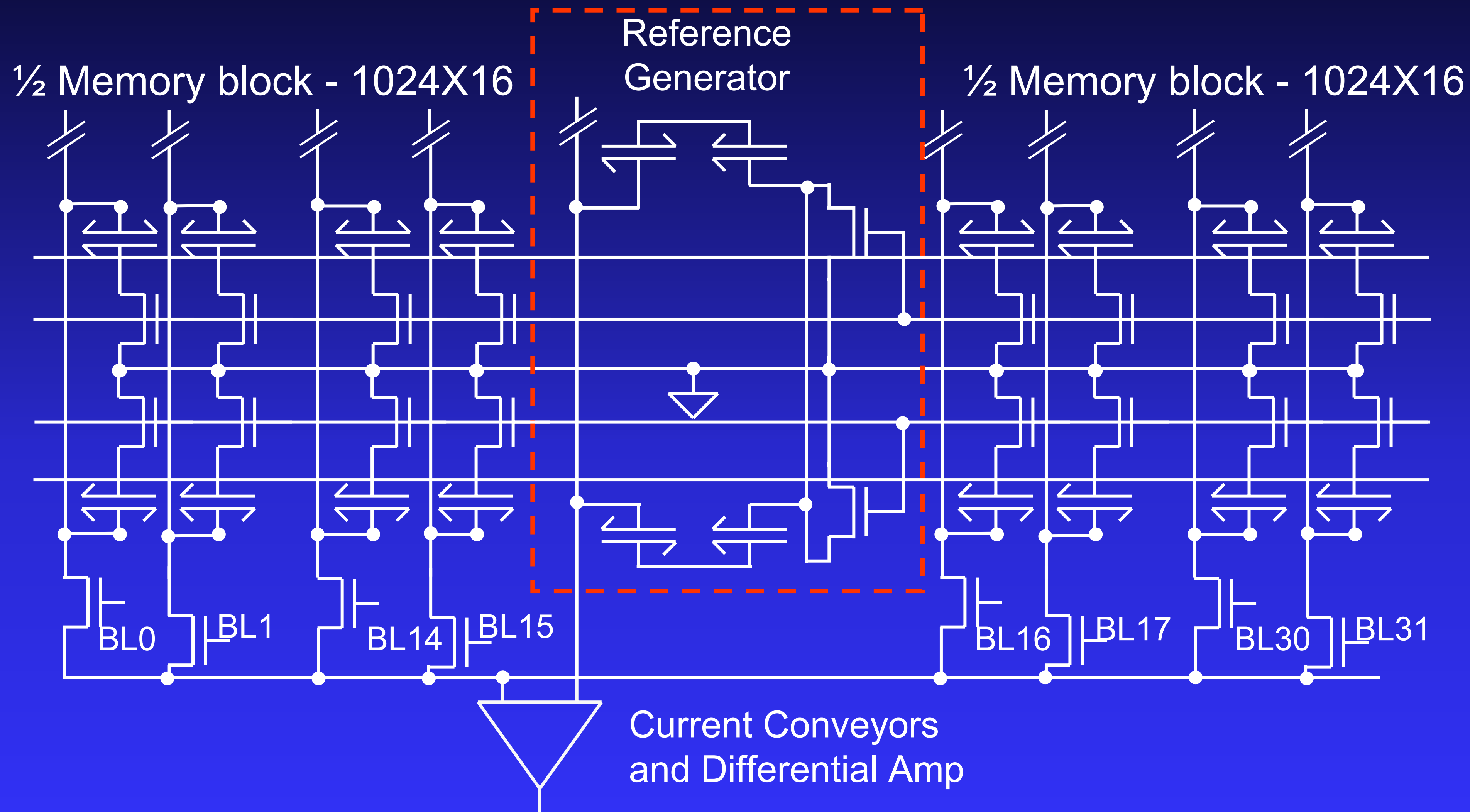
32 Current Conveyors
16 Comparators
16 Regenerators

Array Architecture

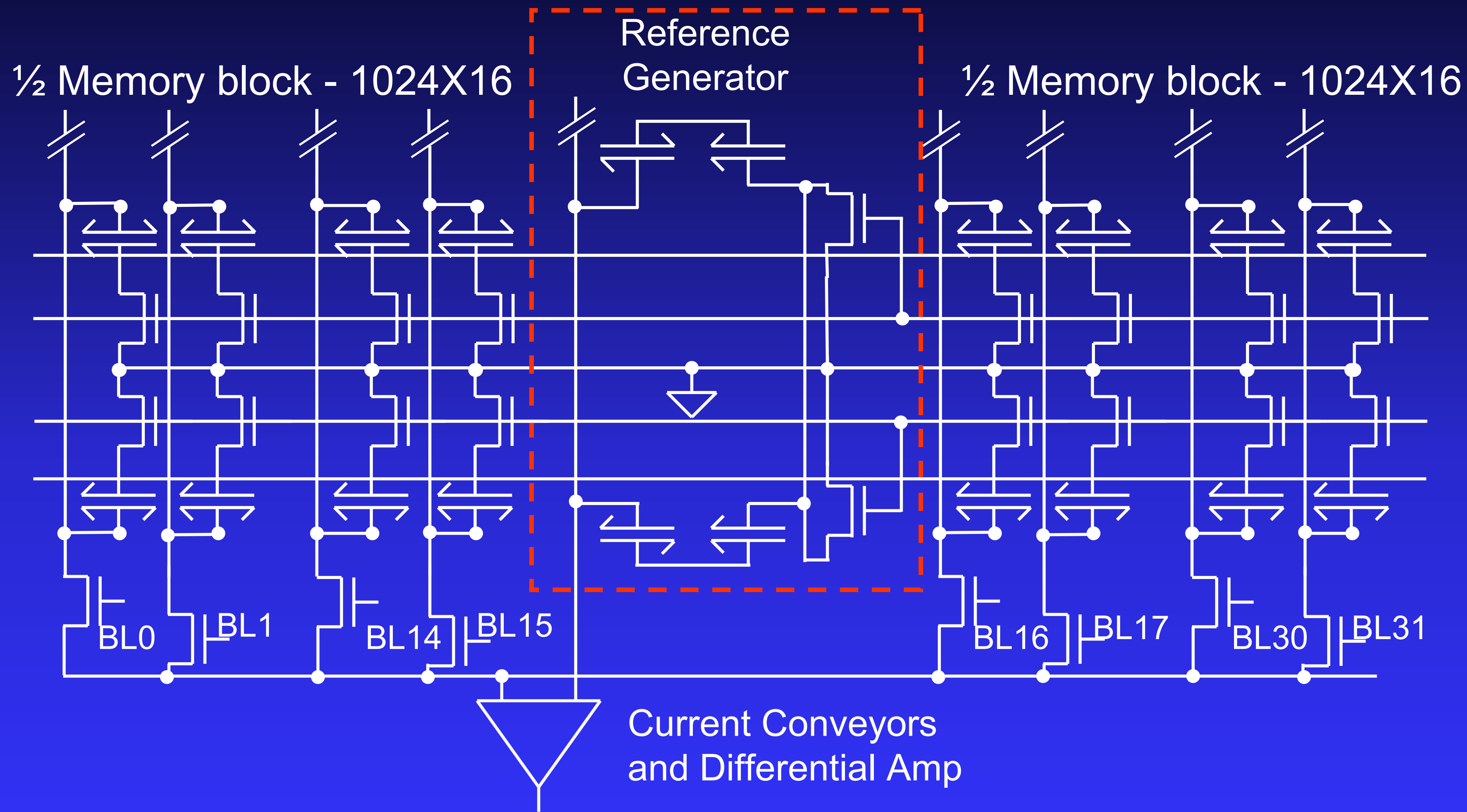




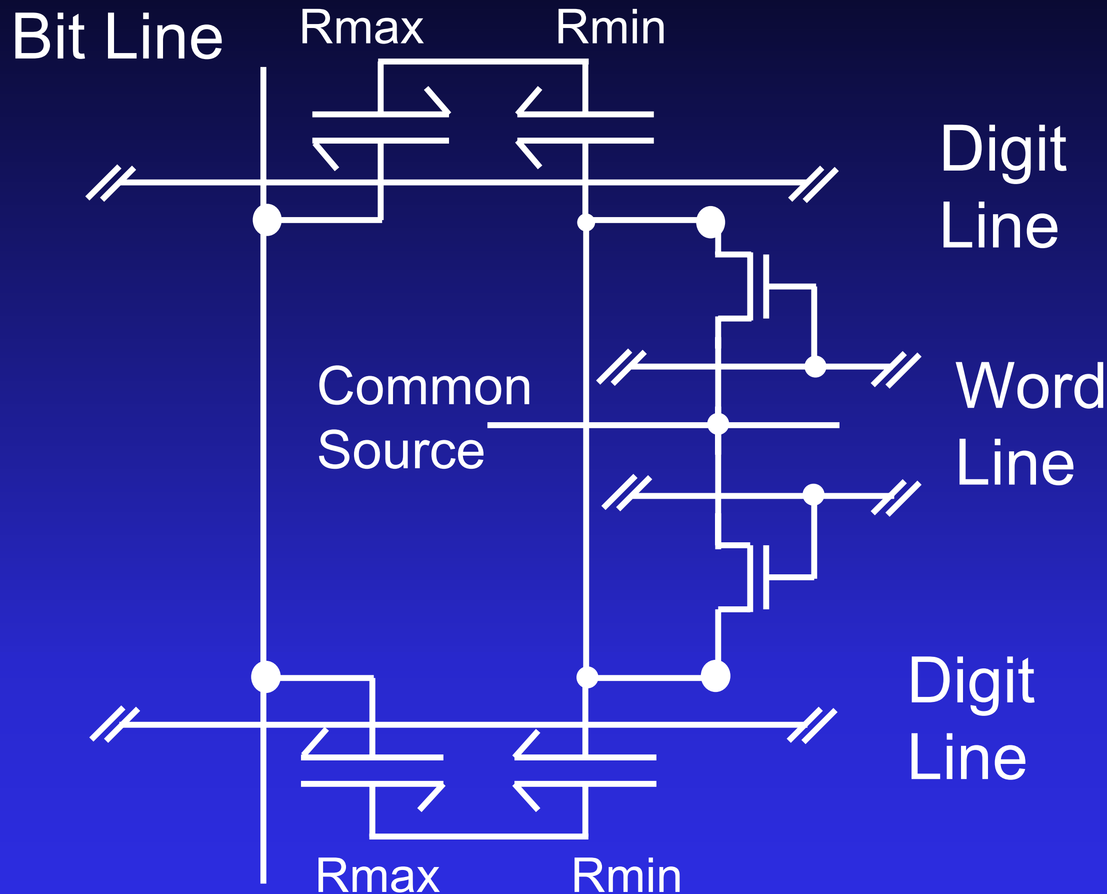
MRAM 32Kb Memory Segment with Reference Generator



MRAM 32Kb Memory Segment with Reference Generator



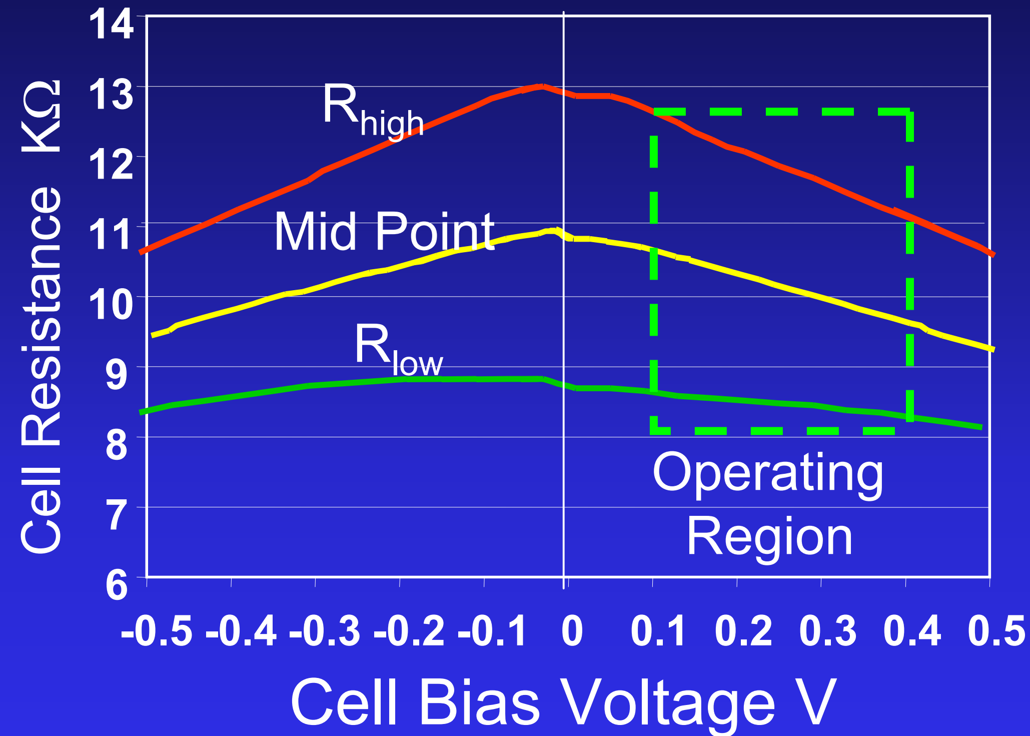
Reference Generator

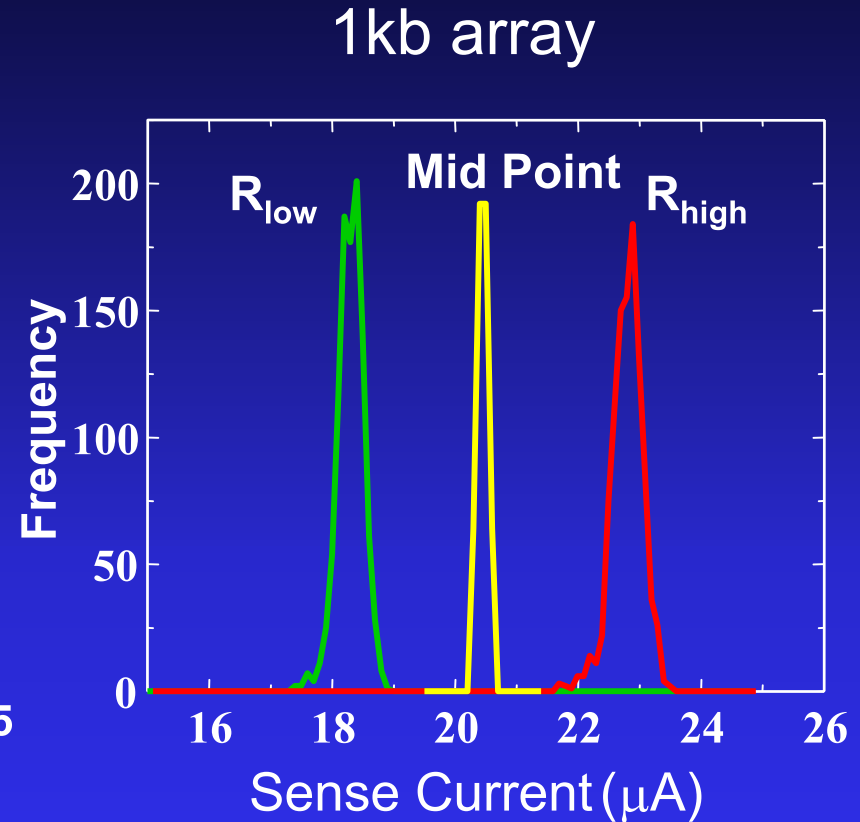


$R_{Ref} = \frac{1}{2}(R_{max}+R_{min})$

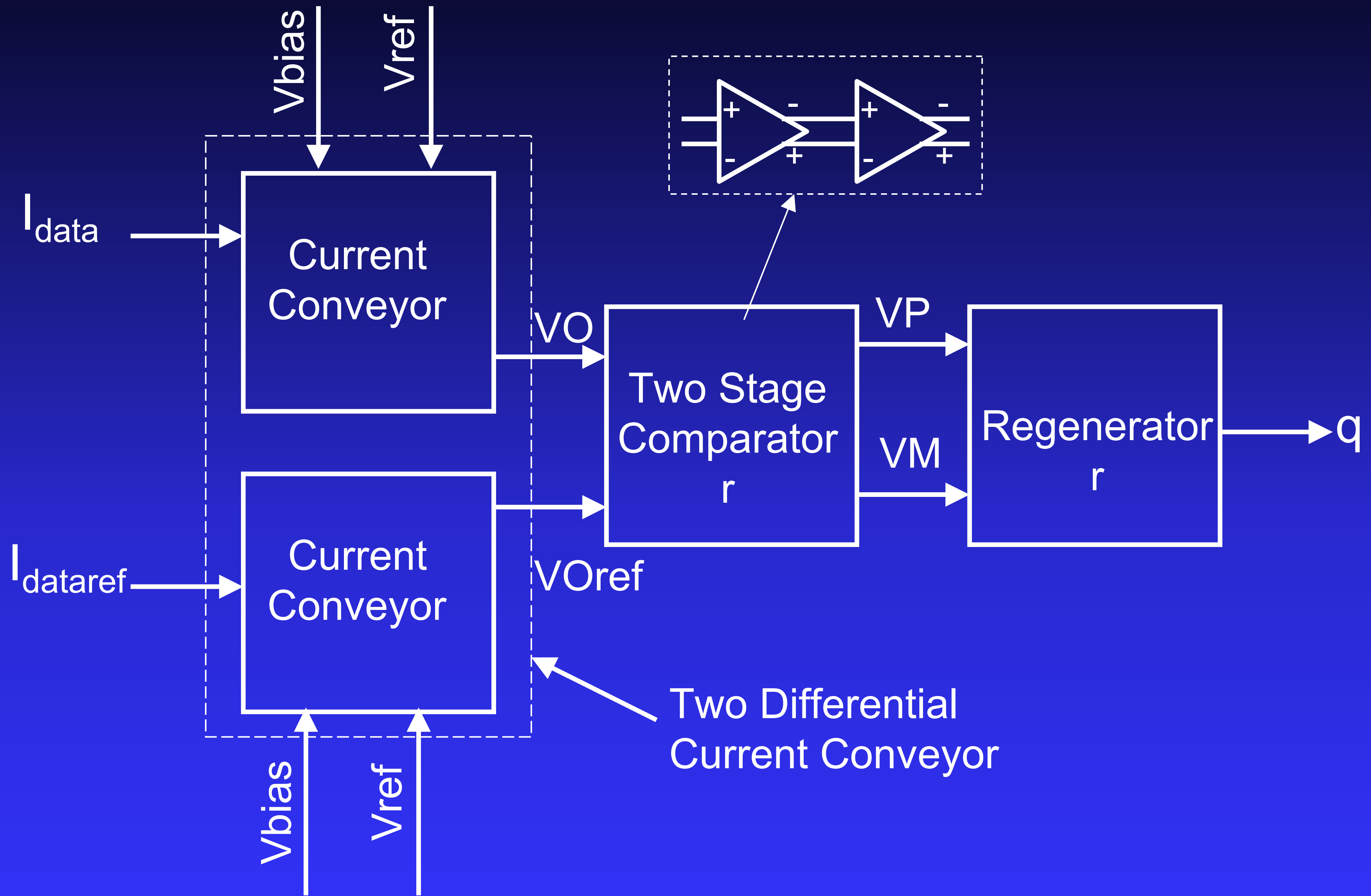
Reference cell-Series/Parallel combination of MTJ devices generating mid resistance between the two memory states

Reference Performance

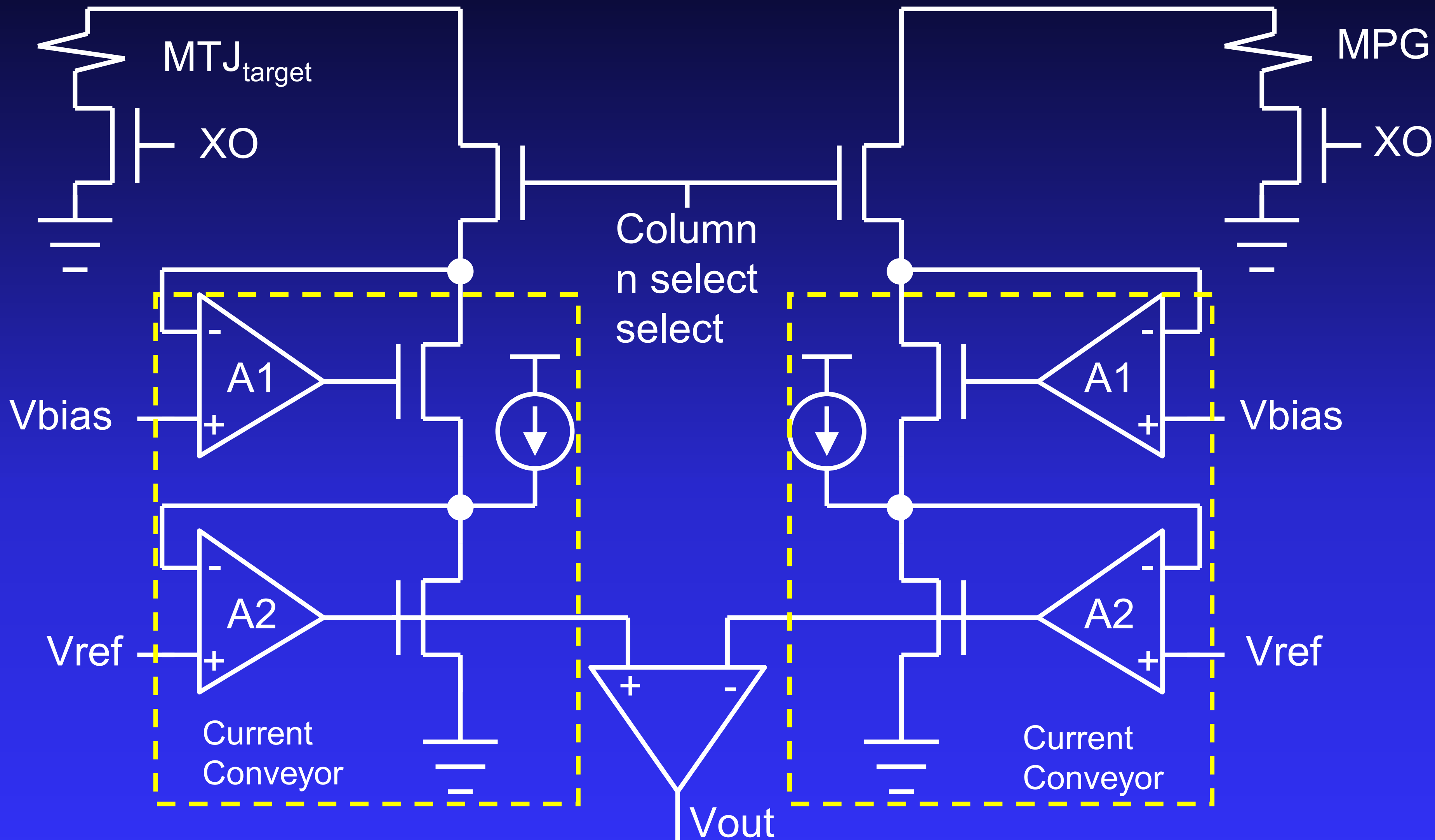




1Mb MRAM Read Circuit



Differential Current Conveyor

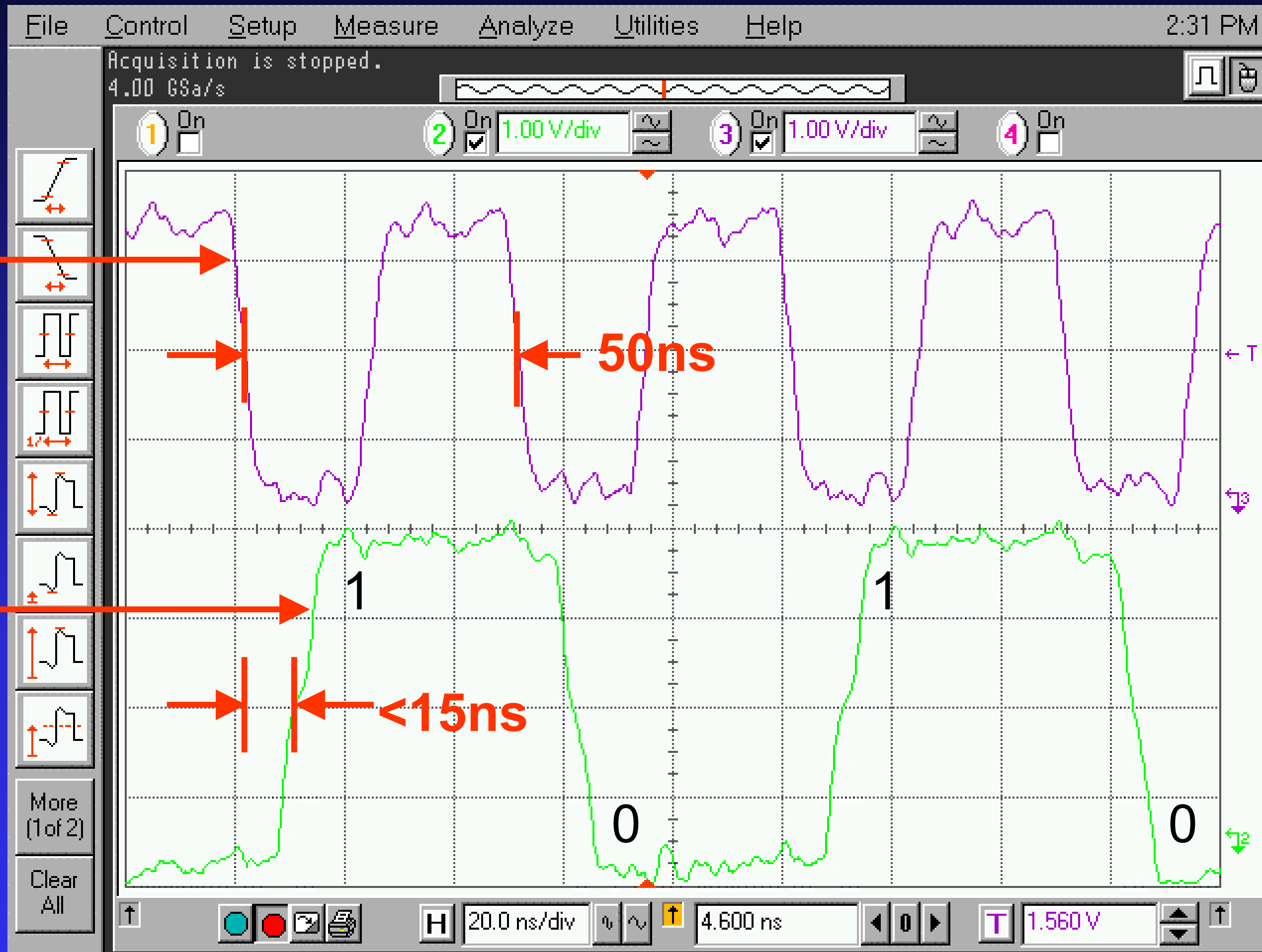


1Mb Measured Access Time

1.00V/div

Output Enable
e

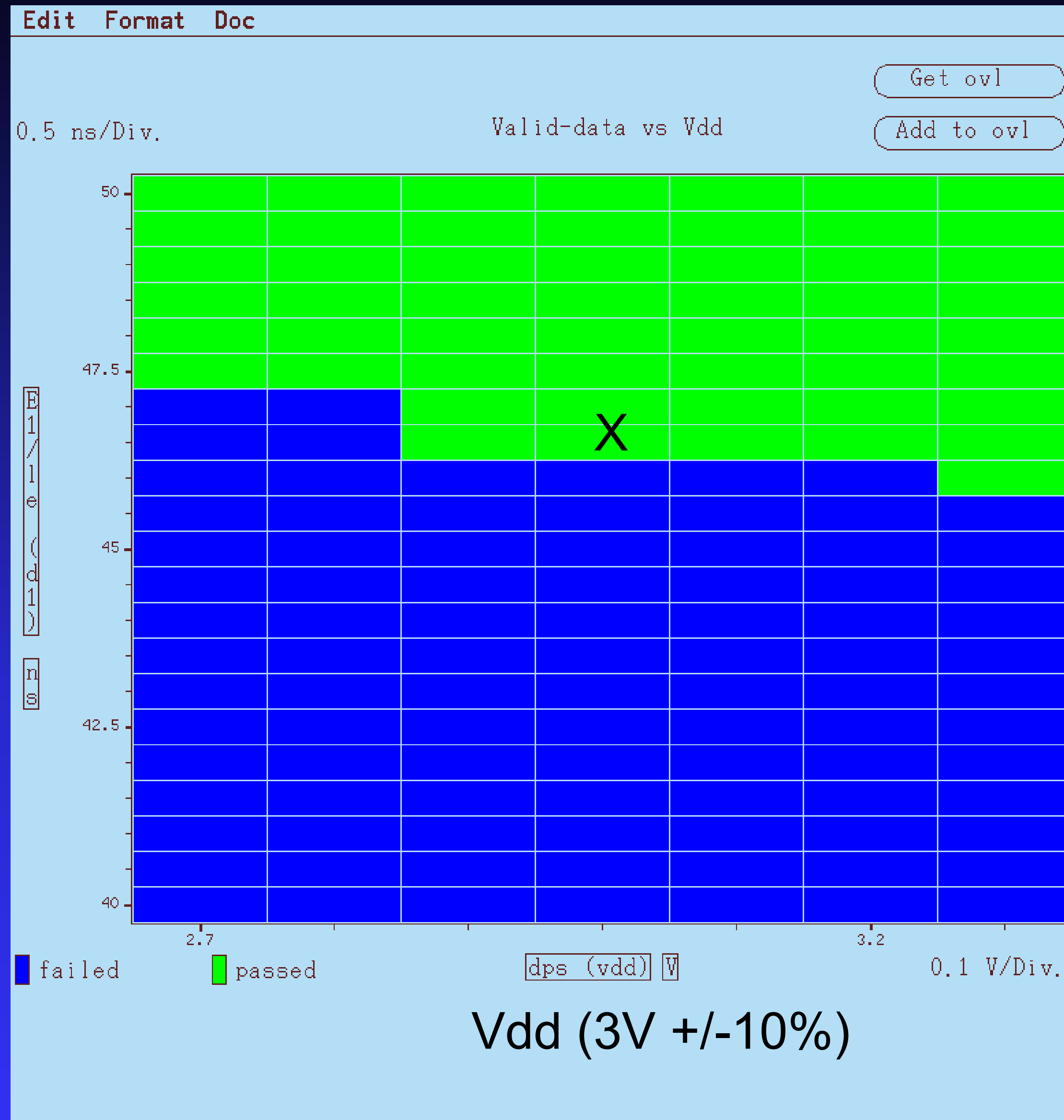
Data Out



20ns/div

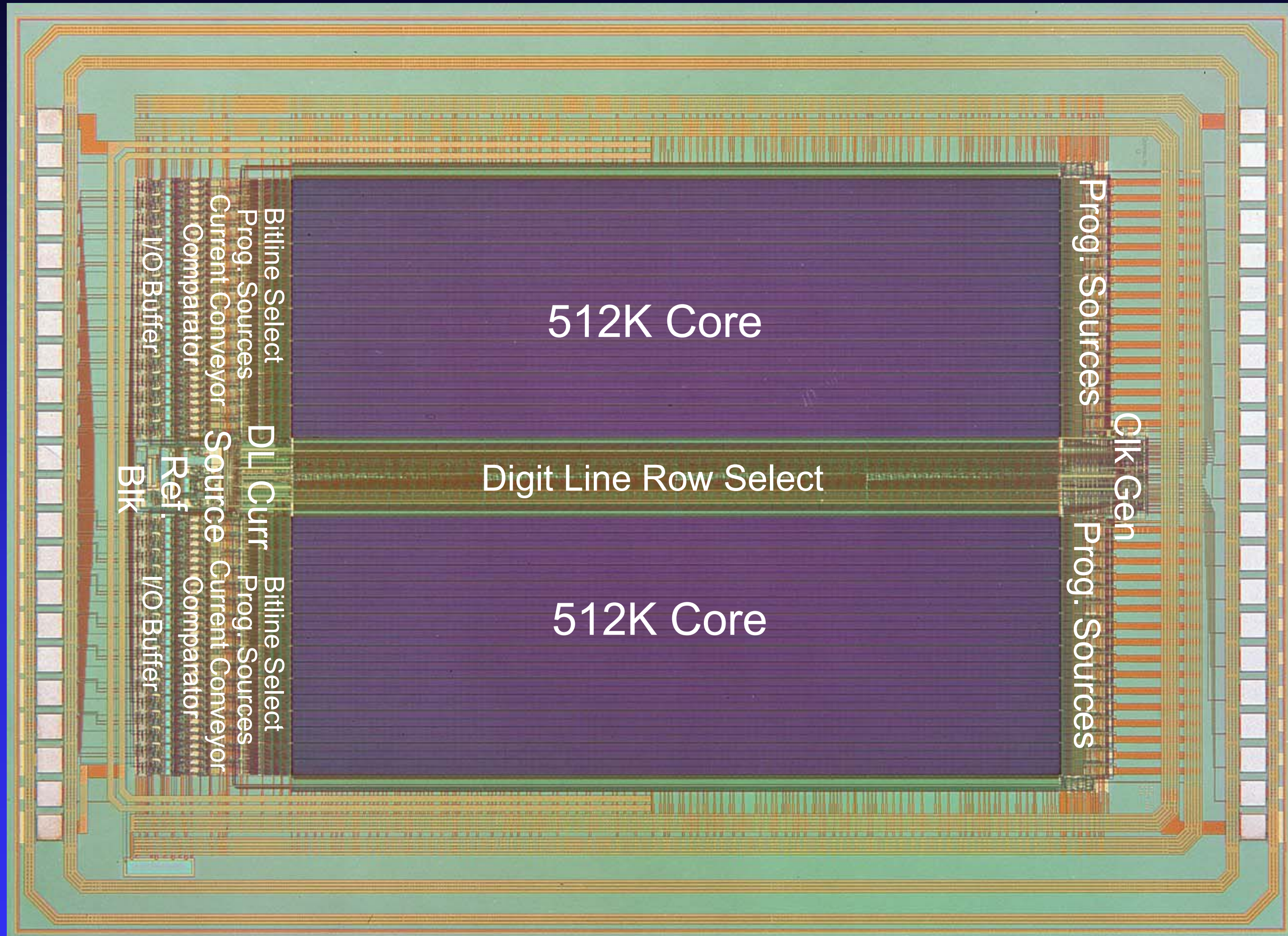
Shmoo Plot of Valid Data out vs. Vdd

Valid Data Out



<50ns @ 3V

1Mb MRAM



1M MRAM Specification

CMOS Technology	0.6μm Five Metal Double Poly (used as linear resistor)
Memory Organization	16K X 16
Cell Size	7.1 μm^2
1M Die Size	4.25mm X 5.89mm
Array Efficiency	>60%
Supply Voltage	2.7V to 3.3V
Access Time	50ns
Cycle Time	50ns

Summary

- Demonstrated 1Mb MRAM with 50ns read and program access time
- Integrated MRAM with Cu metal interconnect
- Cladding of metal layers reduced the power power for programming by factor of four
- New reference generator was demonstrated demonstrated for robust operation
- Demonstrated MRAM material uniformity on on 200mm substrate