



White Paper

Freescalé Technologies for Energy Efficiency

2007 Overview

Contents

1	Overview	3
2	The Design Challenge.....	3
2.1	Process Technology	3
2.2	Circuit Techniques.....	4
2.3	Architectural Techniques	5
2.4	Platform Techniques	5
2.5	Design Methodology and Tools	6
2.6	Software	6
3	Energy Efficiency Technologies at Work.....	6
3.1	QE128 MCUs	6
3.2	MPC8313E PowerQUICC® II Pro Processor.....	7
3.3	MPC8544E PowerQUICC III Processor	7
3.4	i.MX31 Multimedia Applications Processor	7
3.5	MC13783 PMIC	7
3.6	MC1322x Platform-in-Package™ Solution Containing ZigBee® Protocol	7
4	Collaborating for Energy-Efficient Performance	8
5	Conclusion	8

1 Overview

The days of “performance at all cost” are over. Electronic products manufacturers say that achieving raw performance is no longer their number one issue—it’s now “performance within an energy budget.” And, even if the end products are not battery-powered, energy is still a strong design consideration, since energy costs are continuing to rise and wasting energy is environmentally irresponsible. Performance within an energy budget applies to all aspects of industrial, consumer and automotive applications, even if the energy budgets themselves vary considerably.

As semiconductor content increases with each new generation of applications, the semiconductor manufacturer’s contribution to application energy consumption tends to increase accordingly. Market trends are driving for reduced energy consumption while continuing to meet the demands for increased performance and functionality. Our products must be optimized for high performance with constrained energy budgets. This optimization must be tackled across a broad front, including semiconductor process technology, circuit design techniques, system architectures, platform configurations and design methodologies. This optimization also extends to the system software, a key piece in semiconductor-based products.

Power consumption in complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs) is broadly classified as dynamic power in a circuit while it is operating, such as switching, and static power, such as leakage, measured any time a circuit is powered on. Traditionally, static power consumes less energy than dynamic power, yet as CMOS geometries continue to shrink static power is becoming a larger portion of the total energy used. Therefore, power-saving technologies must address both forms of power consumption.

2 The Design Challenge

As a leader in embedded energy-efficient solutions, Freescale is enabling a new generation of electronics that makes the world a smarter and cleaner place. Freescale is dedicated to continually driving down energy costs. The design challenge is to use the technologies and techniques available to intelligently design for energy-efficient operation in all applications.

This challenge is basically a balancing act—finding the most energy-efficient operating point while maintaining target performance levels. Unfortunately, there is no single power reduction technique that is able to meet all the system requirements for energy minimization. The trick is to combine the advantages of one without significantly degrading the advantages of the other.

Freescale combines the attributes of a number of different technologies and techniques highlighted in the Energy Efficiency Target to achieve optimal energy efficiency.



Figure 1: Freescale Energy Efficiency Target

The Freescale Energy Efficiency Target is a holistic approach to energy management, where interaction among the technologies and techniques is critical to achieve optimal energy savings.

Each area of technology can be optimized toward more efficient operation while still contributing to the overall performance goals. The key deliverable for each area of development is that it contributes to the overall goal of best possible performance within a specified energy budget over the life of the application.

2.1 Process Technology

Process technology is the basic building block of any semiconductor product. The characteristics of the process determine the power consumption of circuits built on that process. Our technologies for energy efficiency include process considerations targeted specifically for power optimized circuit operations. Associated techniques for limiting power consumption include:

- **Multi- V_T Process**—Each transistor in a semiconductor design has an associated threshold voltage (V_T) that determines the drive current of that transistor. A lower V_T transistor offers higher performance because of the increased drive current available from that transistor. However, the electrical characteristics of lower V_T transistors tend to make them higher leakage devices. Our manufacturing processes allow us to include both high and low V_T transistors in the same chip. We can design our circuits using low V_T transistors only for those critical paths that need the extra performance. The remainder can use higher V_T transistors, which have the advantage of lower leakage current, which translates into lower standby current.

In addition, Freescale uses innovative structures, materials and process techniques to optimize a transistor's performance while minimizing the leakage. These techniques are used to help improve the efficiency of all transistors, whether high V_T or low V_T .

- **Active Well Bias**—Well-biasing techniques help control channel leakage currents. Active well bias enhances the energy/performance relationship by manipulating transistor performance real-time. With an active back bias technique we use a low V_T device for maximum performance, then raise the threshold in standby mode, thus providing two performance levels in one transistor.

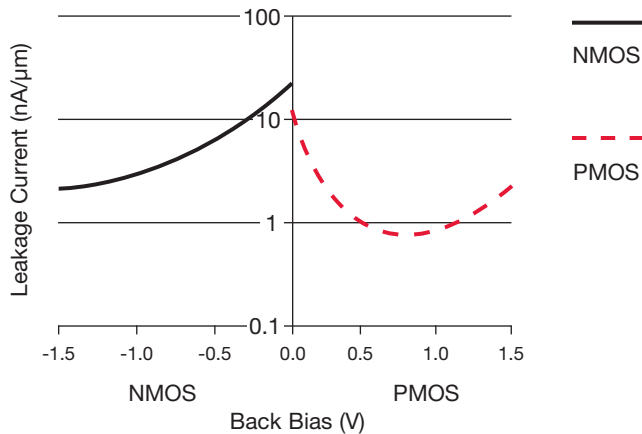


Figure 2: Active Well Bias

Active well bias affects the threshold voltage, which in turn affects the sub-threshold leakage currents. If the body of a PMOS device is increased above V_{DD} or the body of an NMOS device is reduced below ground, the device is said to be in back bias and the sub-threshold leakage current can be reduced.

- **SMARTMOS™ Technology**—Freescale's hybrid processing and integration techniques offer another powerful tool to create highly energy-efficient devices. Our SMARTMOS technology enables high density analog/mixed-signal integration, highly efficient power MOSFETs and complex digital circuitry on a single die. It allows our power management IC (PMIC) solutions to incorporate load protection, high-power efficiency and multiple outputs—even as die sizes shrink—without eroding overall device performance. Introduced two decades ago, SMARTMOS technology has been scaled through multiple generations and is under continual development to improve its capabilities.

Power MOSFETs must be conductive with low switching losses to achieve the most efficient use of the available power supply. Freescale's SMARTMOS technology allows for optimizing the MOSFET design for both drain-to-source resistance and gate charge control by making the gate oxide very thin along with using precise doping techniques to and achieve very low drain-to-source resistance.

The thinner gate oxide allows us to reduce the gate area on the silicon and minimize the charge required to drive the gate, thus reducing switching circuit losses.

2.2 Circuit Techniques

To avoid forfeiting energy efficiency for greater application effectiveness we rely on an entire spectrum of circuit techniques, which when used in combination help regain the energy efficiency edge without sacrificing the optimal performance characteristics.

- **Regulator Design**—Designing for energy efficiency often requires a tradeoff—a decision on which technique is best for whatever application the solution is designed to serve. For instance, a switching regulator is more efficient than a linear or low-dropout (LDO) regulator. However, LDOs are not as costly (you don't need an inductor or other components) and inject less noise into the power supply line. For radio frequency (RF) applications, low noise is a requirement and trumps the greater efficiency of a noisier switching regulator.

Switching regulators normally operate at high frequency using pulse-width modulation (PWM) techniques. Under light load conditions, the switching regulator may transition to pulse frequency modulation (PFM) to maintain high power conversion efficiency. This technique, also called pulse skipping, allows high-efficiency switching regulation under light loads. PFM, with its longer cycle time, is slower to wake from a sleep mode. However, in applications where energy efficiency is critical, designers and users are normally willing to give up a little speed for a longer battery life.

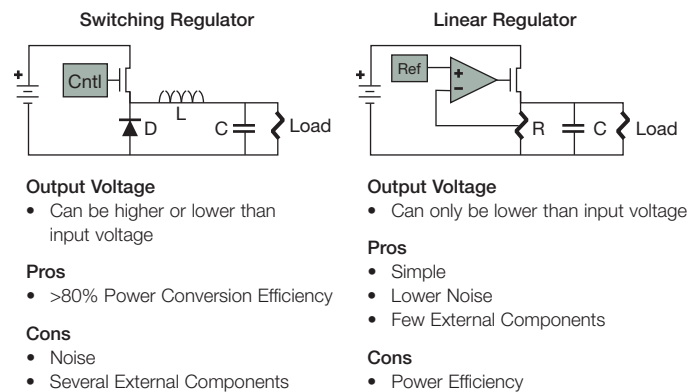


Figure 3: Switching and Linear Regulators

This illustrates the differences between switching and linear regulators.

- **DPTC**—Our dynamic process temperature compensation (DPTC) mechanism measures the frequency of a reference circuit on the product. This reference circuit captures the product's speed dependency on the process technology and existing operating temperature. The DPTC then lowers the voltage to the minimum level needed to support the existing required operating frequency.

- DVFS—Dynamic voltage and frequency scaling (DVFS) allows on-the-fly frequency adjustment according to the existing system performance requirements. By lowering the frequency, it is possible to lower the operating voltage (on-the-fly as well), dramatically reducing the power consumption. There are two common implementations of this methodology—hardware-assisted and software-enabled. The DVFS hardware mechanism automatically monitors the processor load and controls the supply voltage and the frequency with minimal software and operating system involvement. Circuits without DVFS hardware can still implement DVFS through enabling software.
- SRPG—State-retention power gating (SRPG) is a technique that allows the voltage supply to be reduced to zero for the majority of a block's logic gates while maintaining the supply for the state elements of that block. SRPG can thereby greatly reduce power consumption when the application is in stop mode, yet it still accommodates fast wake-up times. Reducing the supply to zero in the stop mode allows both the dynamic and static power to be removed. Retaining the supply on the state elements allows a quick continuation of processing when exiting the stop mode.

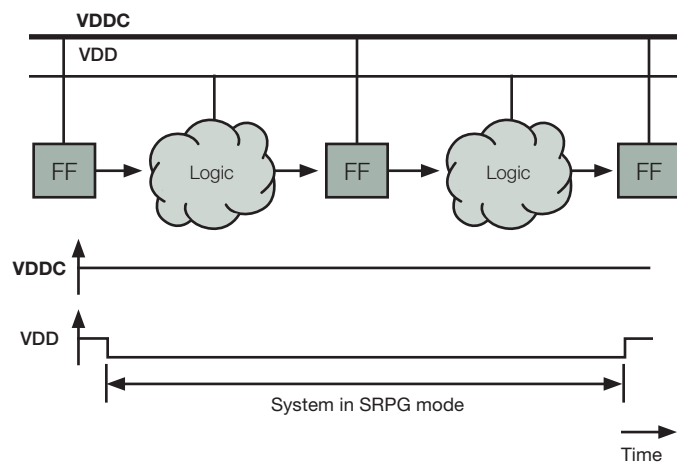


Figure 4: State Retention Power Gating

Since the state of the digital logic is stored in the flip flops, if the flip flops are kept on a constantly powered voltage grid, the intermediate logic can be put onto a voltage grid that can be power gated. When the voltage is reapplied to the intermediate logic, the state of the flip flops will be re-propagated through the logic and the system can start where it has left off.

2.3 Architectural Techniques

At the architectural level, energy efficiency technologies leverage the circuit techniques to enable energy savings across the chip design. These include:

- Clock Gating—This is an effective strategy that is widely used to help reduce power consumption while maintaining the same levels of performance and functionality.

A circuit uses more power when it's being clocked than when the clock is gated, or turned off. The clocks can consume as much as 40 percent of the active power. By shutting off the clocks and stopping the toggling of data in unused portions of the semiconductor we can realize sizable energy savings. The energy savings are particularly significant when the gating is engineered to control the toggling at the individual instruction level.

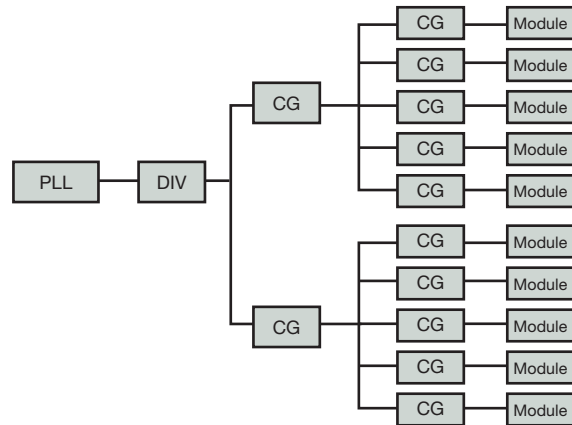


Figure 5: Clock Gating

A typical clock tree where individual modules can be clock gated when not in use. Automatic clock gating control by the modules simplifies the software control.

- Clock Location—The physical mapping of the chip architecture can have a significant effect on energy efficiency by simply shortening the signal and clock routes. For instance, the global clock distribution design must appropriately manage the delays to the end tap points. A poorly designed, ad-hoc distribution may increase the amount of buffering necessary to correct skew at the tap points. This buffering can add to the power dissipation in the clock network. A well-structured distribution can lead to a more efficiently balanced clock tree.
- Power Modes—On-chip power modes are designed to offer peak application performance (and attendant energy consumption) only when absolutely necessary. To deliver the greatest energy efficiency over the life of the application, on-chip power modes, such as run, wait, stop and standby, are used to manipulate power usage to get the most efficient use of the available energy source.

2.4 Platform Techniques

Platforms are made up of a collection of component modules connected together for a specific purpose. A platform may be a collection of modules on a board, in a package or in a single semiconductor device. The combination of modules provides yet another opportunity for energy efficiency optimization.

- **Platform Power Modes**—The power saving modes can be extended to board-level applications. For example, in a memory hold mode, everything can be powered-down except the PMIC and memory, which is kept in a state-retention mode. This is a very low-power state, and in many applications different components, such as an application or baseband processor, will have to reboot at wake-up, creating some latency issues. However, if the core processor is kept in a low-leakage standby mode, wake-up is much quicker because the baseband reboot won't be necessary. The application requirements will often dictate which memory hold state is used for best performance/energy efficiency optimization.

2.5 Design Methodology and Tools

Support/analysis, design, implementation, architecture and power estimation tools help ensure system-to-silicon IC design optimization across power, throughput, latency and area constraints. They help designers create a reliable methodology for energy-efficient semiconductor design, such as:

- **Support/analysis**—Library creation and characterization, along with power monitoring tools help support the module design and chip implementation teams as well as use-case power analysis
- **Design**—Creating the modules used in the product design, tools assist in module functionality and power partitioning as well as module power estimation
- **Implementation**—Integration optimization of all modules into a product. Tools include floor planning, synthesis, clock tree creation and embedded power, timing and power supply voltage (IR drop) analysis
- **Architecture**—Performance/power trade-off analysis for inter- and intra-chip partitions plus use-case analysis
- A platform power estimation tool is used to combine the platform connectivity, the component architecture information, the module power data and the use-case definition into a common database to calculate the estimated power of the platform for a given application. The output of the platform power estimation tool breaks down the power usage per component and module to identify areas of the platform to optimize for overall power.

2.6 Software

Software is an important consideration when designing for energy efficiency. For example, Freescale's eXtreme Energy Conservation (XEC) software, developed for application processors, is an advanced run-time system-software technology. With event-monitoring and predictive algorithms, XEC software dynamically manages performance and optimizes energy conservation. This is a system-wide approach that exploits DVFS, multiple low-power idle modes and other platform power management features to provide "just enough" performance and minimize wasted energy. XEC also features performance predictors, real-time cost/benefit analyzers, performance/power policies and a

policy manager plus many other advanced algorithms to help improve IC and overall system energy efficiency.

3 Energy Efficiency Technologies at Work

Below are a few examples of advanced Freescale semiconductor solutions and some of the technologies employed to provide world-class energy efficiency with minimal impact to product performance.

3.1 QE128 MCUs: the First Flexis™ Family

The S08QE128 (8-bit) and ColdFire V1 MCF51QE128 (32-bit) members of the Flexis series of MCUs are not only the industry's first pin-compatible 8- and 32-bit architectures, but also they both demonstrate extreme energy efficiency for ultra-long battery life in portable applications using deep sleep modes. Each device has multiple stages of stop modes in addition to new low-power wait and low-power run modes, each adding significant energy savings. The low-power wait and low-power run modes allow you to run the device in a low power mode with all peripherals enabled. Additionally, a newly implemented ultra-low-power 32 KHz external oscillator consumes less than 1 uA and can be used in all these modes.

Normally, in run mode an IC has to run at a frequency of at least 1 MHz. Cycling through sleep and wake-up modes to monitor system needs and events can add significantly to peak energy consumption (remember, the clock trees can consume as much as 40 percent of the IC's active power). The QE128 devices offer the alternative to use our 32 KHz oscillator with very low run current, which also avoids the current spikes normally experienced each time the mode is changed. The 32 KHz oscillator is a new module for both the S08QE128 and ColdFire V1 QE128.

The QE128 devices are manufactured using a low-voltage low-power (LVLP) process, which employs transistors with an increased channel length that reduces leakage current, which decreases static power consumption. We subsequently optimized our standard cell library, which includes a number of low-power elements.

The QE128 devices also feature a peripheral clock gating register that can disable clocks to unused modules and an ultra-low-power external oscillator that can be used in stop modes to provide accurate clock source to the real-time counter module.

By implementing a wide variety of energy efficiency technologies in our QE128 devices, we give you the exceptional opportunity to choose the ideal combination of MCU performance and energy efficiency for more different kinds of battery-powered applications than can be offered by any other product portfolio in the industry.

3.2 MPC8313E PowerQUICC® II Pro Processor

Applications in the digital home show high-performance activity interspersed among extended periods of inactivity. The MPC8313E PowerQUICC II Pro processor is a high-performance, cost-effective communications processor particularly well-suited for these applications. It supports doze, nap, sleep and hibernation modes. The MPC8313E processor enables high bandwidth streaming networks in fanless enclosures while hibernation mode allows Energy Star guidelines to be met. Energy Star is a US government program to promote energy efficiency in consumer products.

Hibernation mode begins with a “snapshot” of the processor’s memory content that is then saved to non-volatile memory, enabling the system to be powered down without losing the data. Normally, some form of human interface initiates wake-up from hibernation, such as a key stroke or mouse click, however the MPC8313E’s Wake-on-LAN (WoL) support enables remote wake-up, which helps make hibernation a more flexible low-power mode.

WoL involves sending a special Ethernet packet on demand with a specific byte sequence that initiates the wake-up procedure. For example, the processor core can move into hibernation mode when it makes sense to turn off the power to remove leakage currents. When the application needs the core to wake back up, the special Ethernet packet is recognized as a wake-up command and the power supply is enabled for the processor core. After the core has finished the required task, it may then revert back to hibernation mode.

Remote wake-up capabilities allow designers to utilize the exceptional low-power characteristics of hibernation mode over a broader range of networked applications. The MPC8313E also supports Wake-on-USB and Wake-on-I/O as well as WoL.

3.3 MPC8544E PowerQUICC III Processor

This is a very low-power gigahertz system-on-a-chip (SoC). A selection of low-power transistors and an operating voltage level set at 1.0 volts are the primary drivers for the low dynamic and static power levels. The MPC8544E processor generates just 3.75 watts typical power dissipation at 1 GHz operation, an extremely low-power level for a 1 GHz SoC.

3.4 i.MX31 Multimedia Applications Processor

The i.MX31 processor utilizes a number of techniques to provide energy-efficient performance for computationally-intensive battery powered applications. The 90 nm CMOS processing with dual- V_T transistors provides the optimal performance versus leakage current balance. Active well bias minimizes leakage, and several power domains and clock gating power modes are used.

The i.MX31 architecture leverages specialized execution units (SEUs) to perform processor-intensive tasks. SEUs use less energy than general execution units (GEUs), plus they have the advantage of needing little to no instructions transferred from memory and are more

efficient at utilizing memory for performing a task. Multiple SEUs make it possible to complete more than one instruction per clock cycle, thereby achieving an effective cycle-per-instruction (eCPI) of less than one. More work is completed using fewer clock cycles, thus saving additional energy.

The i.MX31 bus architecture is built to support parallelism through the Smart Speed crossbar switch. The crossbar switch allows all the modules connected on one side (master side) of the chip to communicate with to all the modules connected on the other side (slave side), achieving a more effective throughput. The Smart Speed crossbar switch enables the various SEUs to work in parallel, allowing more work to be done faster and more efficiently.

3.5 MC13783 PMIC

Using SMARTMOS 8 technology and low RDS(on)/low gate charge BiCMOS processing, the MC13783 PMIC offers exceptional power management capabilities to drive energy efficiency through an entire system. The MC13783 is an energy-efficient, highly integrated power management, audio and user interface component that uses buck switches, low capacitance dielectrics, platform power modes and other techniques to extend the battery life for handsets and other portable applications.

3.6 MC1322x Platform-in-Package™ Solution

Manufactured in 90 nm CMOS low-power for radio frequency (LPRF) processing, the MC1322x Platform-in-Package is a highly integrated ZigBee® solution with low-power transistors for digital and RF circuitry running as low as 0.9 volts. It is optimized for Lithium-ion or NiCad batteries, supporting sizes as small as coin cells, providing up to 20 years of system life.

In a personal area network (PAN) environment, the MC1322x Platform-in-Package enables low-power doze and hibernation, with different variations of both, depending on how much memory is to be retained.

The media access controller (MAC) accelerator for IEEE® 802.15.4 is implemented in hardware, so general housekeeping can be performed during beaconing without waking up the MCU or memory. The MAC is also the interface between the radio and peripherals and the MCU and memory. In addition, our process technology allows the Platform-in-Package to conserve energy while transmitting and receiving. Instead of running the radio and CPU concurrently to send and receive a packet, the MC1322x Platform-in-Package bounces the packet between the radio and CPU before and after transmit and receive cycles to conserve power.

4 Collaborating for Energy-Efficient Performance

Ultimately, energy efficiency is measured against customer needs. Whether the application requires a longer battery life or needs to reduce heat dissipation, the system designers have to rely on semiconductors that meet their performance requirements without exceeding a limited energy budget. We work very closely with our customers to clearly define the performance and energy parameters they require. Through close cooperation, we can optimize our solutions to help them make energy-efficient designs that are easy to develop, speed time to market and are more attractive to their customers.

Energy efficiency is also relative to the application. Not every application has to conform to the same criteria for energy optimization as a small hand-held device, such as a cell phone. However, that doesn't mean the same technology used in wireless devices cannot be used to create energy-efficient designs that have an entirely different set of energy guidelines.

For instance, the MPC8311E PowerQUICC® II processor is partitioned so that portions of the chip can be turned on or off. Our wireless divisions have been using this technique for some time for battery powered applications, but it can also be used to improve energy efficiency in the MPC8311E's printing applications. This is an example of how mobile technology is migrating to more performance-driven products.

5 Conclusion

Freescale technologies for energy efficiency are distinctive combinations of advanced architectural and circuit techniques with the latest design methodology and process technology that deliver energy-efficient performance. Freescale applies these technologies and techniques to provide the highest possible performance levels within a restricted energy budget. They can apply to any application, benefiting the user by extending battery life without significantly impacting performance in portable applications as well as keeping energy costs lower and heat dissipation down in wirelined applications across all industries.

It's Freescale's responsibility to deliver products that hit your performance goals while also dramatically improving energy efficiency. We have to measure the tradeoffs and optimize static and dynamic power so you can continue to lower your energy budgets, because we realize you require energy-efficient performance for the life of your applications, across all different modes of operation.

Freescale is dedicated to expanding our technologies for energy efficiency, developing new techniques for next generation products that are even more energy-efficient than today's. We are continuing to work with our customers and our business partners to help you produce more work using less energy.

How to Reach Us:

Home Page:

www.freescale.com

e-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright license granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.
All other product or service names are the property of their respective owners.
© Freescale Semiconductor, Inc. 2007.

Document Number: ENRGYEFFWP
REV 1

