Platform SoC

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Platform SoC

OVERVIEW

Freescale Semiconductor offers highly integrated, customized System-on-Chip (SoC) solutions for the printing and imaging, broadband, network and multimedia markets. The Application Specific Products operation develops platform SoC products built on a foundation of standard Freescale processor cores and proven peripheral intellectual property (IP). The offering is designed to provide customers with the benefits of scalable performance, fast time to market, low system cost and flexible, System-on-Chip platforms that allow easy migration to next-generation system designs.

PLATFORM SoC DESIGN OPTIONS

Freescale Semiconductor offers options for customers who are designing platform SoC devices that enable them to meet maximum performance, differentiation, and high levels of integration requirements.

- Industry required IP
- Design services for system analysis, integration and connectivity
- State of the art process technology
- Package options covering low-cost solutions to high-end flip-chip BGAs

FREESCALE COMPREHENSIVE IP PORTFOLIO

Freescale provides industry standard and cutting edge IP to the platform SoC designer. Where possible, the following IP portfolio is developed in high-level behavioral languages to facilitate the porting of Freescale technologies to future processes.

- Processor cores
- PQ family comm engines
- DSP cores
- External buses
- General communication peripherals
- System fabric IP
- Networking interconnect IP
- Encryption accelerators
- Mixed signal IP
- Memory controllers
- System integration IP
- Industry standard integration structures

FREESCALE DESIGN SERVICES

Freescale platform SoC Design Services offer a flexible customer engagement model for the designer utilizing industry-leading 3rd party tools and providing design handoffs at the RTL (Register-Transfer Level), Gate-Level and COT (Customer Owned Tooling) Sign-Off level at our worldwide design center locations.

- RTL Sign-off—Freescale offers RTL sign-off service to customers who choose to have Freescale handle both synthesis and layout.
- Gate-Level Sign-off—Customers complete the synthesis and then deliver gate-level netlists to Freescale for layout.
- COT—A COT service is available for select customers who choose to do the entire design themselves. Customers deliver the designs in GDSII database format.

Additional design services that are available include:

- Floor planning
- Placement-based synthesis
- Timing analysis
- Test structure insertion
- Clock tree insertion
- Test pattern generation

LEADING EDGE PROCESS TECHNOLOGY

Freescale's manufacturing capabilities include advanced CMOS (complementary metal oxide semiconductor) and related technologies such as silicon-on-insulator (SOI) as well as specialty technologies such as SiGe. These capabilities offer designers the following:

- Process technology available today: 0.18-micron, 130 nm and 90 nm in bulk and SOI with a roadmap to 65 nm and 45 nm
- Proven experience in multiple generations of high-performance SOI, low-k dielectrics, and multi-layer copper metallization

LEADING EDGE PROCESS TECHNOLOGY (continued)

- High-performance BiCMOS process featuring a low-noise SiGe:C HBT for mixed-signal needs across all markets
- Partner on 300 mm CMOS process technology
- Relationships with external foundries

Freescale Process Technologies

Process	0.18 µm	0.13 µm	0.13 µm	90 nm	90 nm SOI
Core Voltage	1.8 V	1.5 V	1.2 V	1.0 V	1.0 V
I/O Voltage (max)	3.3 V	2.5/3.3 V	2.5/3.3 V	1.8/2.5/3.3 V	2.5 V
Metal	AlCu	Cu	Cu	Cu	Cu

PACKAGE AND ASSEMBLY TECHNOLOGY

Freescale offers an assembly package portfolio that covers a wide range of packaging alternatives for the platform SoC customer.

Packaging technology available:

- FCPBGA—Flip Chip Plastic Ball Grid Array
- MAPBGA—Molded Array Process Ball Grid Array
- PBGA—Plastic Ball Grid Array
- QFP—Quad Flat Pack
- SBGA—Stacked Ball Grid Array
- SiP—System in Package
- TBGA—Tape Ball Grid Array
- TEPBGA—Thermally Enhanced Plastic Ball Grid Array
- TQFP—Thin Quad Flat Pack

Assembly Interconnects available:

- Flip Chip Bump—225 µm or 185 µm bump pitch and 1 mm or 0.8 mm ball pitch
- In-line Wire Bond—Pitch down to 44 µm
- Staggered Wire Bond—Pitch down to 35/70 µm

The following table lists some examples of production capable packaging solutions.

Package Style	Performance (MHz)	Thermal Performance @ 45°C T_A (Watts)	Package Pitch (mm)	Ball Count	Body Size (mm)
MAPBGA	100–400	1.25–1.75	0.5–1.0	16–480	8–19
4 Lyr PBGA	100–400	2.25–2.5	1.0–1.27	144–900	17–40
TEPBGA-2	100–400	2.5–2.75	1.0–1.27	144–900	17–40
SBGA	100–1000	2.75–4.0	1.0–1.27	256–900	23–45
TBGA	25–125	2.75–4.5	1.0–1.27	276–1036	23–45
Flip Chip with HS	1000–10000	2.0–60.0	0.5–1.27	119–1500	16–35

SUMMARY

Use Freescale platform SoC solutions to get:

- Benefits of scalable performance
- Fast time-to-market
- Flexible customer engagement model
- Easy migration to next-generation system designs
- Leading edge process technology
- Broad IP portfolio
- Expertise in systems engineering and architectures
- Global design centers

For more information on platform SoC solutions, go to: http://www.freescale.com

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