

Configuration of FlexRay Controller System Memory Access Timeout Value

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1 Introduction

This document describes the configuration of the timeout value in System Memory Access Time-Out Register.

The correct configuration of the timeout value is required for reliable and defined operation of the FlexRay Controller. This value depends only on the frequency of the system bus clock, which is used as the clock of the CHI module in the FlexRay controller.

The timeout value corresponds directly to a certain acceptable number of wait states on the system bus.

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2 Configure System Memory Access Time-Out Register (FR_SYMATOR)

To ensure reliable operation of the FlexRay Controller, the application must ensure that the TIMEOUT value in System Memory Access Time-Out Register (FR_SYMATOR) and the CHI clock frequency f_{CHI} in MHz fulfill [Equation 2-1](#).

$$0 \leq \text{SYMATOR}[\text{TIMEOUT}] \leq \lfloor 0.45 \cdot f_{CHI} - 8 \rfloor \quad \text{Eqn. 2-1}$$

If the SYMATOR[TIMEOUT] value and f_{CHI} violates [Equation 2-1](#), the behavior of the FlexRay Controller becomes unreliable and undefined. It may happen that frames are not transmitted at all, including key slot frames.

For a given SYMATOR[TIMEOUT] value, f_{CHI} can be increased without causing unreliable operation of the FlexRay Controller. The same holds for reducing the SYMATOR[TIMEOUT] value for a given f_{CHI} .

Some examples for maximum values of the SYMATOR[TIMEOUT] for a minimum CHI frequency are given in [Table 2-1](#).

Table 2-1. Maximum SYMATOR[TIMEOUT] examples

f_{CHI}	SYMATOR[TIMEOUT]
≥ 18 MHz	0
≥ 23 MHz	≤ 2
≥ 27 MHz	≤ 4
≥ 32 MHz	≤ 6
≥ 60 MHz	≤ 19
≥ 80 MHz	≤ 28

3 System Bus Wait State Constraints

The SYMATOR[TIMEOUT] value corresponds directly to a certain acceptable number of wait states on the system bus.

For single-channel configurations and if the sync frame table generation functionality is *not* used ($\text{FR_SFTCCSR}[\text{SDVEN}, \text{SIDEN}] = 0$), no timeout will be detected if less than $2 \cdot \text{SYMATOR}[\text{TIMEOUT}] + 1$ wait states will be seen on the system bus for each system bus access.

For dual-channel configurations, or if the sync frame table generation functionality is used, no timeout will be detected if less than $\text{SYMATOR}[\text{TIMEOUT}] - 1$ wait states will be seen on the system bus for each system bus access.

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