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A comparison of the MC9S12DP256 (mask set 0K36N) versus the HC12

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Introduction

Overview

This document compares the various modules of the MC9S12DP256 (mask 0K36N) with equivalent modules in the HC12 family and is meant to be used as a guide in conjunction with the appropriate device Data Books.

It is structured (where possible) to align with the Chapter structure of the MC9S12DP256 Technical Data Book, MC9S12DP256/D.

Generally, the first subsection of each chapter highlights the differences in features of the two devices. Where appropriate, this is followed by a comparison of the individual registers and bits.

The HCS12 (MC9S12DP256) design methodology includes a greatly improved highly flexible I/O structure. On the HC12, port control is managed by register bits in the appropriate peripheral modules. On the MC9S12DP256, the functionality of these bits has been greatly expanded and centralized in the **Port Integration Module (PIM)**.

Conventions Used Throughout This Document

In the register comparisons, the bits highlighted in bold italics indicate the differences between the corresponding registers of the devices being compared.

Registers not identified remain identical.

Port I/O control bits are not included in the register comparisons as their functionality has been transferred to the PIM. For detail on the I/O philosophy and Port registers refer to the **Port Integration Module (PIM)** chapter in this document and in the MC9S12DP256 Technical Data Book, MC9S12DP256/D.

Module Base Addresses

The following table lists the base addresses for each module on the MC9S12DP256 and their equivalent on the 68HC912DG128 (or 68HC912B32 in the case of the BDLC module).

Table 1Module Base Addresses

Module	Base Address	
	68HC912DG128	**MC9S12DP256**
BKPT	$20	$28
CRG	(CGM) $34	$34
ECT	$80	$40
ATD0	$60	$80
PWM	$40	$A0
SCI0	$C0	$C8
SCI1	$C8	$D0
SPI0	$D0	$D8
IIC	$E0	$E0
BDLC	$F8 (on 68HC912B32 not 68HC912DG128)	$E8
SPI1	—	$F0
SPI2	—	$F8
Flash	$F4	$100
EEPROM	$F0	$110
ATD1	$1E0	$120
MSCAN0	$100	$140
MSCAN1	$300	$180
MSCAN2	—	$1C0
MSCAN3	—	$200
PIM	—	$240
MSCAN4	—	$280
BDM	$FF00	$FF00

Central Processing Unit (CPU)

Introduction

- Identical programmers model.
- Pipe increased to 3 stages (from 2 plus latch) giving deterministic behavior.
- All instructions implemented using same Mnemonics & Op codes.
- Further detail can be found in the HCS12 CPU Reference Guide.

MOVB/MOVW instructions:

On the HC12, when using the PC relative addressing mode, an offset is required to be added to/subtracted from the displacement computed from the base address, which is equal to the address of the next instruction. This is detailed in chapter 3.9.1 of the CPU12 Reference Manual (CPU12M/AD). It is handled transparently by assemblers and compilers for the HC12 today.

On the HCS12 this is no longer the case. This base is the same for both source and destination operands and any assemblers/compilers that calculate an offset will generate incorrect code.

Examples

```
MOVB2,PCR,$1000
DC.B1,2,3,4,5,6,7,8,9
```

HCS12: $1000 is written to 3
HC12: $1000 is written to 1

The other way round

```
MOVB$1000,2,PCR
TEMPDS.B    10
```

HCS12: Value read at $1000 is moved to TEMP+2
HC12: Value read at $1000 is moved to TEMP+5

It is important to ensure that a compiler or assembler is HCS12 compliant on this point.

Instructions with cycle count reduced by 1

BRCLR	IDX1
BRSET	IDX1
CALL	EXT, IDX, IDX1, IDX2 (7,7,7,8)
CLR	[D,IDX], [IDX2]
STAA	[D,IDX], [IDX2]
STAB	[D,IDX], [IDX2]
STD	[D,IDX], [IDX2]
STS	[D,IDX], [IDX2]
STX	[D,IDX], [IDX2]
STY	[D,IDX], [IDX2]
STOP	INH (entering)
TRAP	INH (mapped to multiple op codes)
WAI	INH (entering)

Instructions with cycle count reduced by 2

BRCLR	IDX2
BRSET	IDX2
MUL	INH
TBL	IDX

Instructions with cycle count increased by 1

RTC	INH
RTI	INH (with pending interrupt)
STOP	INH (exiting)
WAI	INH (interrupt occurs)

NOTE: *The increase in RTC is compensated for by the reduction in the number of cycles in the CALL instruction. Effective throughput is the same number of cycles except CALL IDX2, RTC.*

Instructions with operations re-ordered

In order to make the cycle by cycle operation the same for similar instructions, the free cycle "f" has been moved to the last operation (133 cases). [Pf at end of instruction = even number of cycles]

In order to make the cycle by cycle operation the same for similar instructions, the optional program word fetch cycle "O" has been moved to the last operation (72 cases). [PO at the end of instruction = odd number of cycles]

In 14 other cases the cycle by cycle sequence has been modified to end in the program word fetch "P" (no "f" or "O" cycles in instructions).

A total of 219 cycle order changes have been made in the CPU operation. These should be transparent for most applications.

Hardware

Introduction

The MC9S12DP256 has many more (multiplexed) peripheral modules than the 68HC912DG128 and a significantly different power supply structure to cater for it's low voltage, high performance 0.25µ core logic and 5V compatible, highly flexible I/O ports.

This requires a different printed circuit board (PCB) layout.

Hybrid layouts, supporting both foot prints, can be achieved using a combination of jumpers, pull-up/down resistors and solderable links but these are likely to result in significant compromises in performance and EMC.

This section compares the PCB requirements of the MC9S12DP256 with those of the 68HC912DG128. The first section highlights the differences in features, including some considerations on power supply layout and decoupling.

Summary of Additional Functions on MC9S12DP256

- ATDVRL and VRH voltage reference input

  The MC9S12DP256 requires a single ATD voltage reference input and reference ground pin shared by both converters as opposed to the separate reference connections for each converter on the 68HC912DG128.

- Pin out changes and Package details

  The mechanical package is identical (112 pin LQFP, Case 987) to the 68HC912DG128 but many pins with equivalent functionality have changed location.

- ATD channel convention

  On the MC9S12DP256, the channels for ATD1 are referred to in the documentation by AN08–AN15 instead of AN10–AN17 as on the 68HC912DG128. This gives clear and consistent channel numbering from 00 on up allowing for future implementations of converters with greater than 8 input channels.

  Physically, the channels of ATD1 (AN08–AN15) remain interlaced with the channels of ATD0 (AN00–AN07) as on the 68HC912DG128 but their location relative to pin 1 has moved.

- EXTAL pin

  The oscillator is part of the higher frequency logic, hence EXTAL input is limited to 2.5V signals.

- XTAL pin

  The XTAL output can be buffered with a high-impedance buffer to drive the EXTAL input of another device. On the MC9S12DP256, the maximum output voltage of this pin is VDDPLL (2.5V).

- Port K

  The MC9S12DP256 has 6 pins on Port K to support 64 x 16K pages of external memory (1 Mbyte).

- VSTBY pin

  There is no RAM standby function on the MC9S12DP256, so the VSTBY pin has been removed.

- MODC pin

  Previously referred to as SMODN, this is for factory test only. The pin continues to act as the background debug pin in user applications.

- TEST pin

  This is a ‘factory-test’ only input and MUST be grounded or pulled to ground with a pull-down resistor in all other applications.

- ECLK output

  ECLK control is significantly different. Please refer to the Port E and PEAR register sections of the MC9S12DP256 Technical Data Book, MC9S12DP256/D for details.

- Port E7 pin

  On the MC9S12DP256, the alternate functionality of this pin has changed – (CAL function not available, *ECLK not available, *DBE not available). Pulling PE7 (*XCLKS) low during the reset phase bypasses the internal low current oscillator and an internal buffer (2.5V) driven by EXTAL feeds the internal clocks.

- Port K7 pin.

  On the MC9S12DP256, this pin is used as an emulation chip select signal for the emulation of the internal memory expansion or as general purpose I/O, depending upon the state of the EMK bit in the MODE register.

  The value on this pin during reset determines the state of the ROMON bit during reset into all expanded modes.

- Flash programming voltage

  On the MC9S12DP256, the non-volatile Flash memory is '5V only' and does not require an external VFP Pin as on the 68HC912DG128; this removes the need for an external charge pump.

MC9S12DP256 Power Supply Detail

The MC9S12DP256 has an internal 2.5V regulator to supply the high performance core logic as opposed to the 5V only logic supply of the 68HC912DG128. Some key points are highlighted here, but it is essential that the Voltage Regulator (VREG) Chapter of the MC9S12DP256 Technical Data Book be reviewed in detail.

- VREGEN Pin

  I/P used to define the standby operating mode of the internal voltage regulator.

- VDD1 & VDD2 Pins

  2.5V supply pins for the core logic which require decoupling.

- VDDPLL Pin

  On the 68HC912DG128, this pin, when grounded, caused the PLL circuitry to be bypassed. On the MC9S12DP256, it is a 2.5V (internal) supply pin for the high performance PLL logic and must NOT be grounded (or connected to 5V).

- Layout considerations

  Avoid current loops in power supply tracks.
  All ground pins (VSS**) must be connected externally.
  VDDA/VSSA and VRH/VRL supplies MUST be clean.
  Connection for external power supply monitor should be close to VDDA.

- Further Decoupling Guidelines

  For all capacitors in the nF range, it is essential to use a type with low ESR.
  All recommendations are load and PC board routing dependent.

  – VDDX

    This is highly dependent on the type of load and switching frequency since VDDX supplies only the 5V drivers in Ports J, K, T, P, M & S.

    Start with 47–220nF and add 10µF if big loads are switched and the supply track is long (highly inductive).
    All fast switching peripherals, PWM, timer, CAN etc. are located on this bus.

– VDDA

Here a good noise decoupling is key; the internal load is almost static.
Recommended 22nF–100nF.

– VDD1,2

These are the outputs of the internal voltage regulator.
Recommended 47–220nF.

– VDDR

This pin supplies the internal regulator as well as the I/O ports A, B, E & H.
Two alternatives:

a. Expanded bus
High peak current through Port A, B, E mainly.
Recommended 100nF + 10uF.

b. Single chip mode.
Here we have a load dependent variant. Since the are no fast switching peripherals on this supply relatively slow switching outputs under software control assumed.
Recommended 100nF if no big loads on the output.
If higher output currents are required, add 1µF – 10µF.

– VDDPLL

The most important point here is decoupling of the high frequency noise generated by the oscillator and PLL switching.
Recommended 22nF – 100nF.

– VRH & VRL

This is the reference for the ADT convertor so it must be a ‘clean’ supply.
Recommended 10nF, high frequency.

EEPROM Memory

EEPROM Memory

A new EEPROM technology has been implemented on the MC9S12DP256 which differs completely from the 68HC912DG128. It is recommended that the appropriate sections of the MC9S12DP256 Technical Data Book, MC9S12DP256/D, should be read and understood before attempting any code conversions.

The 4Kbyte EEPROM module is arranged in a 2048 by 16-bit configuration and may be read as bytes, aligned words or misaligned words. Write operations for program or erase are only allowed as aligned word accesses. An erased word reads $FFFF.

A command state machine has been added to the flash block to simplify the program and erase algorithms.

It is not possible to read from the EEPROM array while it is being programmed or erased.

The base addresses for the EEPROM registers are as follows:

68HC912DG128	MC9S12DP256
$F0	$110

MC9S12DP256 Versus 68HC912DG128

- New register block.
- ECLKDIV register used to supply the command state machine with a clock reference between 150 and 200 KHz, from the extal input reference.
- EEPROM size increased to 4Kbytes from 2Kbytes.
- Aligned word programmable only, no longer byte programmable.
- Minimum erase sector size 4 bytes, compared to byte erasable.
- The command state machine can generate interrupts, therefore programming and erase routines can be interrupt driven.

- A configurable protected area is available. The size of the protected area can be set from 0 to 512 bytes in multiples of 64 bytes. The EPROT (EEPROM protection) register is preloaded out of reset with a value stored in EEPROM.

Flash Memory

Flash Memory

A new flash technology has been implemented on the MC9S12DP256 which differs completely from the 68HC912DG128. It is recommended that the appropriate sections of the MC9S12DP256 Technical Data Book, MC9S12DP256/D, should be read and understood before attempting any code conversions.

The 256Kbyte flash module is comprised of four 64Kbyte blocks. Each 64Kbyte block is arranged in a 32K by 16-bit configuration and may be read as bytes, aligned words or misaligned words. Write operations for program or erase are only allowed as aligned word accesses. An erased word reads $FFFF.

A command state machine has been added to the flash block to simplify the program and erase algorithms.

The base addresses for the Flash registers are as follows:

68HC912DG128	MC9S12DP256
$F4	$100

MC9S12DP256 Versus 68HC912DG128

- New register block.
- FCLKDIV register used to supply the command state machine with a clock reference between 150 and 200 KHz, from the extal input reference.
- Flash size increased to 256Kbytes from 128Kbytes.
- No requirement for an external programming voltage, VFP pin removed.
- Aligned word programmable only, no longer byte programmable.
- Erase sector size 512 bytes, bulk erase also available, compared to bulk erase only.
- All four blocks can be programmed and erased in parallel.
- The command state machine can generate interrupts, therefore programming and erase routines can be interrupt driven.

- Two configurable protected areas within each 64 Kbyte block. One area can be configured as a 0.5, 1, 2 or 4 Kbyte protected block, the other as a 2, 4, 8 or 16 Kbyte protected block.
- One 64 Kbyte block contains all the information relating to security and the protected areas within the entire 256 Kbytes. The FPROT (Flash protection) and FSEC (Flash security) registers are preloaded out of reset with the values stored in flash, there is also an additional eight bytes used as a security backdoor comparison key.
- Improved write/erase cycle performance.

Port Integration Module (PIM)

Introduction

The MC9S12DP256 has an extremely flexible I/O structure which is centrally configured in the Port Integration Module (PIM) providing a high level of multiplexed functionality on pins.

The PIM provides two basic functions

- Arbitration of which module has control of the pads for a given configuration, i.e. which module is allowed to drive the pads and in what direction at any one time.

  Each module takes control in turn according to an assigned priority.
- Defines the "electrical" characteristics where appropriate for each pin.

  Those are:
  - reduced drive
  - wired-or mode (more accurately open-drain mode)
  - pull-ups/downs. Here certain precautions are taken, such as if the CAN is enabled pull-up is allowed, but pull-down is blocked.

The 68HC912DG128 port control was more limited and controlled by individual register bits in the appropriate peripheral modules with limited sharing of I/O functions.

The base addresses for the PIM registers are as follows:

68HC912DG128	MC9S12DP256
—	$240

I/O port configuration

On the MC9S12DP256 each port has a set of control registers (in the PIM) arranged in a similar structure where each individual I/O pin can be configured for:

- Input/output selection
- Drive strength reduction
- Enable and select of pull resistors
- Interrupt enable and status flags

A standard port has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strengths
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections
- Interrupt inputs with glitch filtering

Port Input Registers can be used to detect overload or short circuit conditions on output pins.

Refer to the external pin description section of the MC9S12DP256 Technical Data Book, MC9S12DP256/D, for further details.

Clocks and Reset Generator (CRG)

Clocks and Reset Generator (CRG)

The CRG module provides system clock generation and is responsible for oscillator, phase locked loop (PLL), real time interrupt (RTI) and computer operating properly (COP) watchdog control.

The CRG replaces the Clock Generator Module (CGM) found on the 68HC912DG128 and although they both provide similar functionality, the CRG should be considered as a new module.

This section is intended to highlight the differences between the CRG and CGM, but due to the complexity and importance of this module it is recommended that the appropriate sections of the MC9S12DP256 Technical Data Book, MC9S12DP256/D, should be read and understood before attempting any code conversions.

The base addresses for the CRG registers are as follows:

68HC912DG128	MC9S12DP256
(CGM) $34	$34

MC9S12DP256 Versus 68HC912DG128

- Restructured register block.
- Maximum bus speed increased to 25 MHz (extal 50 MHz) from 8MHz (extal 16MHz).
- If extal is driven by an external clock source then the signal amplitude swing MUST be limited between VSS and VDDPLL (2.5 Volts).
- VDDPLL is no longer used as a logic level when exiting reset. It is internally generated from an onboard VREG and under no circumstances should it be connected to VSS.
- The reset state of PE7 (not XCLKS) can be used to bypass the oscillator when using an external clock signal to drive extal (PE7 = VSS).
- Self Clock Mode (SCM) is a terminology change from Limp Home Mode.
- The startup counter, used by the crystal monitor to check for proper oscillator startup recovery has been changed to a 14-stage (8192 cycles) from a 13-stage (4096 cycles) counter.

- COP is disabled out of reset in normal modes, the time-out rates have changed.
- RTI rates have been enhanced offering increased flexibility.
- The SLOW MODE divide feature on the 68HC912DG128 has been removed.
- Increased control over PLL functionality.
- Internal resets hold the reset pin low for 128 SYSCLK cycles, the reset pin is then sampled a further 64 cycles later to determine whether the reset source is internal or external. In comparison the 68HC912DG128 asserts the reset pin low for 16 ECLK cycles and then samples a further 9 cycles later.

Pulse Width Modulator (PWM)

Introduction

This section compares the PWM module of the MC9S12DP256 with that of the 68HC912DG128.

The base addresses for the PWM registers are as follows:

68HC912DG128	MC9S12DP256
$40	$A0

Summary of Additional Functions on MC9S12DP256

- Expanded to eight full channels.
- Independent justification control of all channels.
- Emergency shutdown

  An Emergency shutdown function has been incorporated into the MC9S12DP256. If the emergency shutdown function is enabled and port P bit 7 becomes active, all enabled PWM output channels are immediately driven to the level defined by PWMLVL in the PWMSDN register.
- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Comparison of PWM Equations

PWM Scaling equations

68HC912DG128

Clock S0 = Clock A / (2 * (PWSCAL0 + 1))
Clock S1 = Clock B / (2 * (PWSCAL1 + 1))

MC9S12DP256

Clock SA = Clock A / (2 * PWMSCLA)
Clock SB = Clock B / (2 * PWMSCLB)

PWM Period Equations

68HC912DG128

Left Aligned Output
Period = [Channel-Clock-Period * (PWPER + 1)]

Centre Aligned Output
Period = [Channel-Clock-Period * (2 * PWPER)]

MC9S12DP256

Left Aligned Output
PWMx Period = Channel Clock Period * PWMPERx

Center Aligned Output
PWMx Period = Channel Clock Period * (2 * PWMPERx)

Register Block Comparison

Symbolic names have been modified from PWxx to PWMxx. Software equates should be adjusted to suit.

The greatest changes to the MC9S12DP256 PWM register map occur due to the expansion of the PWM from four to eight modulators. The additional modulator control registers PWMCNT4–7, PWMPER4–7, PWMDTY4–7 and reorganization of PWME, PWMPOL, PWMCLK, PWMPRCLK, PWMCAE, and PWMCTL facilitate this addition.

PWM Enable Register:

Address offset: $02

	0	***0***	***0***	***0***	PWEN3	PWEN2	PWEN1	PWEN0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – PWEN

Address offset: $00

	PWME7	***PWME6***	***PWME5***	***PWME4***	PWME3	PWME2	PWME1	PWME0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWME

PWME7..0 — PWM Enable Bits

PWM channel enabled. The pulse modulated signal becomes available at PWM output line when its clock source begins its next cycle.

PWM Polarity Register and Clock Select Register:

Address offset: $01

	PCLK3	***PCLK2***	***PCLK1***	***PCLK0***	PPOL3	PPOL2	PPOL1	PPOL0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – PWPOL

Address offset: $01

	PPOL7	***PPOL6***	***PPOL5***	***PPOL4***	PPOL3	PPOL2	PPOL1	PPOL0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMPOL

Address offset: $02

	PCLK7	***PCLK6***	***PCLK5***	***PCLK4***	***PCLK3***	***PCLK2***	***PCLK1***	***PCLK0***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMCLK

PPOL7..0 — PWM Enable Bits

If set, PWM channel output is high at the beginning of the period, then goes low when the duty count is reached.

PCLK7..0 — PWM Clock Select Bits

The PWM clock select bits, which were contained in the upper nibble of the PWPOL, register are now in a dedicated PWMCLK register.

PWM Prescale Clock Select Registers:

Address offset: $00

	CON23	***CON01***	***PCLKA2***	***PCLKA1***	***PCLKA0***	***PCLKB2***	***PCLKB1***	***PCLKB0***
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – PWCLK

Address offset: $03

	0	***PCKB2***	***PCKB1***	***PCKB0***	***0***	***PCKA2***	***PCKA1***	***PCKA0***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMPRCLK

Address offset: $05

	CON67	***CON45***	***CON23***	***CON01***	PSWAI	PFRZ	0	0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMCTL

PCKA2..0, PCKB2..0 — PWM Prescale A and B Clock Select Bits

The PWM prescale clock select bits, which were contained in the PWCLK register, are now in a dedicated PWMPRCLK register. Notice that the bit definitions have moved as well.

CON67, 45, 23, 01 – Concatenation Control Select Bits

The concatenation control bits have been increased for the additional channels and moved to the PWMCTL register.

PWM Control Registers (continued)

Address offset: $14

	0	0	0	***PSWAI***	***CENTR***	RDPP	PUPP	PSBCK
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – PWCTL

Address offset: $05

	CON67	CON45	CON23	CON01	***PSWAI***	***PFRZ***	***0***	***0***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMCTL

Address offset: $04

	CAE7	***CAE6***	***CAE5***	***CAE4***	***CAE3***	***CAE2***	***CAE1***	***CAE0***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – PWMCAE

PSWAI — PWM Stops in Wait Mode

The PSWAI bit has be moved from the 5th bit position to the 4th position in the PWMCNT register.

PFRZ — PWM Counters Stop in Freeze Mode

The PFRZ bit has been added to disable the PWM input clock to the prescaler whenever the part is in freeze (background) mode. This is useful for emulation.

CAE7..0 — PWM Center Align Enable Select Bits

Independent control of channel justification is now available in a dedicated PWMCAE register. In the 68HC912DG128, all channels were controlled collectively by one bit, CENTR, but in the MC9S12DP256, each channel can be justified individually by its own CAE bit.

Enhanced Capture Timer (ECT)

Introduction

The enhanced capture timer can be used for generating periodic pulses (output compare), time measurements (e.g. measure of a pulse frequency or measure between two occurred pulse events – input capture), counting the number of times an event occurs (using a pulse accumulator) or to generate a periodic interrupt (using the modulus down counter).

This section compares the ECT module of the MCS912DP256 with that of the 68HC912DG128.

The base addresses for the ECT registers are as follows:

68HC912DG128	MC9S12DP256
$80	$40

Summary of Additional Functions on MC9S12DP256

- Toggle on overflow

  The MC9S12DP256 can be configured to toggle output compare pins on timer overflow. This feature is enabled using a new register.
- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Register Block Comparison

Timer Toggle On Overflow Register1 (TTOV):

This register has been added to the MC9S12DP256. It gives the user additional control over the I/O pins in output compare mode.

Address offset: $07

	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
Reset:	0	0	0	0	0	0	0	0

MCS912DP256 – TTOV

TOVx — Toggle On Overflow Bits

TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 7 override events.

Timer System Control Register 1 (TSCR1)

TSCR1 was called TSCR in the 68HC912DG128.

Address offset: $06

	TEN	TSWAI	***TSBCK***	TFFCA	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – TSCR

Address offset: $06

	TEN	TSWAI	***TSFRZ***	TFFCA	0	0	0	0
Reset:	0	0	**0**	0	0	0	0	0

MC9S12DP256 – TSCR1

TSFRZ

Timer and Modulus Counter Stop while in Freeze (background) Mode.

Timer System Control Register 2 (TSCR2)

TSCR2 was called TMSK2 in the 68HC912DG128.

Address offset: $0D

	TOI	0	***PUPT***	***RDPT***	TCRE	PR2	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – TMSK2

Address offset: $0D

	TOI	0	***0***	***0***	TCRE	PR2	PR1	PR0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – TSCR2

Timer Interrupt Enable Register 1 (TIE)

TIE was called TMSK1 in the 68HC912DG128.

Address offset: $0C

	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
Reset:	0	0	0	0	0	0	0	0

Serial Communications Interface (SCI)

Introduction

The MC9S12DP256 has 2 identical SCI modules identified as SCI0 and SCI1 respectively.

This section compares the SCI module of the MC9S12DP256 with that of the 68HC912DG128.

The base addresses for the SCI registers are as follows:

	68HC912DG128	MC9S12DP256
SCI0	$C0	$C8
SCI1	$C8	$D0

Summary of Additional Functions on MC9S12DP256

- SCI Stop in Wait Mode enable

  Control of the SCI power utilization in wait mode has been added. If this function is enabled all clocks to the module will be disabled and the module will be in its lowest power state.

- Transmitter pin data direction in Single-Wire mode

  Transmitter pin direction is now controlled via the SCI module registers instead of the port control registers.

- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Register Block Comparison

SCI Control Register1:

Address offset: $02

	LOOPS	SWOM	RSRC	M	WAKE	ILT	PE	PT
Reset:	0	**0**	0	0	0	0	0	0

68HC912DG128 – SCIxCR1

Address offset: $02

	LOOPS	***SCISWAI***	RSRC	M	WAKE	ILT	PE	PT
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – SCIxCR1

SCISWAI — SCI Stop in Wait Mode enable

This bit controls the enable of the SCI in wait mode.

The SWOM function is now part of the PIM functionality.

SCI Status Register2:

Address offset: $05

	0	0	0	0	0	0	0	RAF
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – SCIxSR2

Address offset: $05

	0	0	0	0	0	0	***TXDIR***	RAF
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – SCIxSR2

TXDIR — Transmitter pin data direction in Single-Wire mode

This bit controls whether the TX pin of the SCI is an output or input in single-wire mode.

The state of this bit overrides the setting of the respective port S data direction register bit.

Serial Peripheral Interface (SPI)

Introduction

The MC9S12DP256 has 3 identical SPI modules identified as SPI0, SPI1 and SPI2 respectively.

This section compares the SPI module of the MC9S12DP256 with that of the 68HC912DG128.

The base addresses for the SPI registers are as follows:

	68HC912DG128	MC9S12DP256
SPI0	$D0	$D8
SPI1	—	$F0
SPI2	—	$F8

Summary of Additional Functions on MC9S12DP256

- Baud rate Control

  The SPI baud rate register has three additional bits that pre-scale the module clock allowing greater baud rate selection possibilities.
- 16 bit transfers

  An idle master or idle slave that has no data loaded into its transmit buffer allows the user to queue up 16-bit values to send.
- SPI0 may be defined to operate in wired-or mode.
- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Register Block Comparison

SPI Control Register1:

Address offset: $00

	SPIE	SPE	*SWOM*	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

68HC912DG128 – SPxCR1

Address offset: $00

	SPIE	SPE	***SPTIE***	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset:	0	0	0	0	0	1	0	0

MC9S12DP256 – SPIxCR1

SPTIE — SPI Transmit Interrupt Enable

This bit enables an SPI interrupt to be generated each time the SPTEF flag is set.

The SWOM function is now part of the PIM functionality.

SPI Baud Rate Register:

Address offset: $02

	0	0	0	0	0	SPR2	SPR1	SPR0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – SPxBR

Address offset: $02

	0	***SPPR2***	***SPPR1***	***SPPR0***	0	SPR2	SPR1	SPR0
Reset:	0	0	0	0	0	1	0	0

MC9S12DP256 – SPIxBR

SPPR2..0 — SPI Baud Rate Pre-selection Bits

The baud rate divisor equation is as follows:

BaudRateDivisor = (SPPR +1) *2(SPR+ 1)

The additional bits allow pre-scaling of the module clock to compensate for increased clock rates.

SPI Status Register:

Address offset: $03

	SPIF	WCOL	0	MODF	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – SPxSR

Address offset: $03

	SPIF	0	***SPTEF***	MODF	0	0	0	0
Reset:	0	0	1	0	0	0	0	0

MC9S12DP256 – SPIxSR

SPIF — SPI Interrupt Flag

This bit is set after a received data byte has been transferred into the SPI Data Register. This bit is cleared by reading the SPISR register (with SPIF set) followed by a **read** access to the SPI Data Register.

1 = New data copied into the SPIDR
0 = Transfer not yet complete

The clearing mechanism of this bit has been changed. In the previous version the bit was cleared by reading the SPISR (with SPIF set) followed by **reading or writing** the SPI Data Register.

The write collision status flag has been removed.

SPTEF — SPI Transmit Empty Interrupt Flag

This bit is set each time the transmit data register transfers a byte into the transmit register.

The write collision status flag has been removed.

Inter-IC Bus (IIC)

Introduction

The Inter-IC Bus (IIC or I2C) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC Bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This section compares the IIC module of the MC9S12DP256 to the IIC module of the 68HC912DG128.

The base addresses for the IIC registers are as follows:

68HC912DG128	MC9S12DP256
$E0	$E0

Summary of Additional Functions on the MC9S12DP256

- The number of programmable serial clock frequencies has increased from 64 (68HC912DG128) to 256 (MC9S12DP256).
- IBIF flag requires writing a "0" to clear. The 68HC912DG128 requires a "1".
- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Register Block Comparison

IIC Bus Frequency Divider Register:

Address offset: $01

	0	0	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – IBFD

Address offset: $01

	IBC7	***IBC6***	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – IBFD

IBC7–IBC0 — IIC Bus Clock Rate 7–0

This field is used to prescale the clock for bit rate selection. The bit clock generator is implemented as a prescaled shift register. IBC7–3 select the prescaler divider and IBC2-0 select the shift register tap point. Two addition bits, IBC[7:6], have been added to the MC9S12DP256, which provide an additional divider factor to increase the number of programmable clock frequencies to 256.

Motorola Scalable CAN (MSCAN)

Introduction

The MSCAN module is a serial messaging interface designed to communicate on a Controller Area Network (CAN) communication bus. The module implements the CAN 2.0 A/B protocol as defined in the BOSCH specification dated September 1991.

The MC9S12DP256 has 5 identical MSCAN modules identified as CAN0 to CAN4, each with its own RxCAN and TxCAN pins.

This section compares the MSCAN module of the MC9S12DP256 with that of the 68HC912DG128. The first section highlights the difference in features of the two devices.

The functionality of the MSCAN module has changed from previous HC12 designs to the MC9S12DP256 version. Most of the changes are additions to the functionality, but a few are changes to the way that user software interacts with the MSCAN module. One other major difference with the MC9S12DP256 is that is has 5 MSCAN modules on board.

Refer to Motorola Application Note AN2011/D and the MC9S12DP256 Technical Data Book, MC9S12DP256/D, for a detailed description of all of the changes to the memory map, registers, control bits and other details of the new MSCAN module.

The base addresses for the MSCAN registers are as follows:

	68HC912DG128	MC9S12DP256
MSCAN0	$100	$140
MSCAN1	$300	$180
MSCAN2	—	$1C0
MSCAN3	—	$200
MSCAN4	—	$280

Summary of Additional Functions on MC9S12DP256

- Listen Only Mode

  Listen Only mode allows the MSCAN module to be used to monitor CAN bus traffic without being able to send out any messages of its own, as the name implies. Listen Only Mode supports applications which require “hot plugging” or throughput analysis. No ACK or Error frames are transmitted in this mode.
- Wired-OR mode

  Available only with CAN0-CAN3

  This affords the ability to effectively increase the hardware filtering capability of MSCAN on a given network. For example, with two MSCAN modules in Wired-OR mode on the same network (e.g. – CAN0 and CAN1) two different hardware filtering configurations can be used to look for separate sets of messages on the bus. Each set of messages will then produce filter hits on the appropriate CAN module, resulting in separate interrupt vectors being called. This allows the user to write two sets of receive interrupt service routines (ISR) to handle each set of messages separately. This can drastically reduce the need for software filtering mechanisms in what would have been a single ISR before resulting in faster ISR execution and therefore lower CPU impact.

  Selection is controlled by the **Port Integration Module (PIM)**.

  Wired-OR mode changes the transmit structures of the port M pins to open drain outputs (active low only).

  An external pull-up resistor should be used (3.3kohm or so at most), located at the transceiver, especially for higher speed (>125kbps) communications. Internal pull-ups might not provide sufficient strength to adequately reduce the RC time constant on the transmit pin connection to the transciever.
- Increased Receive Buffer Capacity

  The receive message buffer has been expanded on this new version of the MSCAN from 2 to 4 message buffers. This allows twice as many messages as before to be received before the buffer overflows. This buys time for the application software to service the message receive ISR without as much risk of losing messages. This is very important as more features are being added to microcontrollers and users are implementing increased functionality with a single MCU.

- Message Buffer Time Stamping

  The new MSCAN module contains a time stamping feature for transmitted and received messages. This feature utilizes an internal 16-bit timer in the MSCAN module and places the timer value into a previously reserved two-byte segment of the active message buffer when a message is transmitted or received and the timer is active.
- The five MSCAN modules on the MC9S12DP256 share pins with several other modules, namely Port M, Port J[7:6], Key Wakeup Pins KWJ[7:6], and the Inter-IC (IIC) Bus module.
- Expanded I/O Pin control now handled by the Port Integration Module (PIM), including prioritization of access to pins by active modules. The PIM arbitrates between modules sharing pin resources. Please refer to the **Port Integration Module (PIM)** section for more details.

Register Block Comparison

Please refer to AN2011/D for a detailed description of all of the changes to the memory map, registers, control bits and other details of the new MSCAN module.

Analog-to-Digital Converter (ATD)

Introduction

The MC9S12DP256 has 2 identical ATD modules identified as ATD0 and ATD1 respectively. With the exception of the VDDA &VSSA (analog supply voltage) and VRH & VRL (analog conversion reference) all other pins are duplicated for each module.

The ATD module is an 8-Channel, 10-bit, multiplexed input, successive approximation, analog to digital converter accurate to ± 1LSB.

This section compares the ATD module of the MC9S12DP256 with that of the 68HC912DG128.

The base addresses for the ATD registers are as follows:

	68HC912DG128	MC9S12DP256
ATD0	$60	$80
ATD1	$1E0	$120

Summary of Additional Functions on MC9S12DP256

- External triggering

  The MC9S12DP256 has an additional external triggering function that allows the user to synchronize the ATD conversion process with external events. The device can be configured to trigger on edges or levels of different polarities. Register ATDxCTL2 controls this function.
- External Trigger Input Pin

  This pin is multiplexed with the CH7 input and is used to provide an external trigger input signal for the device when it is used in external trigger mode.
- Conversion sequence length

  The MC9S12DP256 allows additional control over the number of conversions in a sequence. In the 68HC912DG128, the user has a choice of 4 or 8 conversions depending on the S8CM control bit in the ATDxCTL5 control register. However, in the MC9S12DP256 device, the number of conversions is controlled by a binary value in the ATDxCTL3 control resister.

- FIFO Mode

  The MC9S12DP256 allows the user to select between different result register assignments in a conversion sequence. The reset state is identical to the 68HC912DG128 in that the first result converted is stored in the first register, the second result in the second etc. However, an additional FIFO mode is available that changes the register assignments. In this mode, the results are placed in consecutive registers between conversion sequences. The result registers mapping wraps around when the end of the register file is reached. Register ATDxCTL2 controls this function.

- Data justification

  The MC9S12DP256 allows the user to control the justification (left or right) of the result that is stored into the data registers. The justification depends on the resolution that is selected. Register ATDxCTL5 controls this function.

- Signed/Unsigned control

  The MC9S12DP256 allows the user to control if the data that is stored in the result registers is signed or unsigned. Register ATDxCTL5 controls this function.

- Multichannel Conversion

  The MC9S12DP256 allows the user additional flexibility when using the multi-channel conversions function. The user can configure the device to sample across several channels. The number of channels sampled is controlled by the S8C–S1C bits in the ATDxCTL3 register. The first channel sampled is determined by the state of the CC, CB and CA bits in the ATDxCTL5 register.

- Analog/Digital Input Pin Multiplexing

  The MC9S12DP256 has an Input Enable Mask register that allows the user to individually enable each digital input buffer. This multiplexing feature gives the user greater control. Register ATDDIEN controls this function.

- Expanded I/O Pin control (ref **Port Integration Module (PIM)**)

Register Block Comparison

ATD Control Register 2: .

Address offset: $02

	ADPU	AFFC	ASWAI	0	0	0	ASCIE	ASCIF
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – ATDxCTL2

Address offset: $02

	ADPU	AFFC	ASWAI	***ETRIGLE***	***ETRIGP***	***ETRIGE***	ASCIE	ASCIF
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – ATDxCTL2

ETRIGE – External Trigger Mode enable

This bit controls the enable of the external trigger mode.

ETRIGP – External Trigger Polarity control

This bit controls the polarity of the external trigger signal.

ETRIGLE – External Trigger Level/Edge control

This bit controls the mode of the incoming external trigger signal.

Reset Condition

Out of Reset the external trigger mode, on the MC9S12DP256, is disabled. Operation is identical to the 68HC912DG128.

ATD Control Register 3:

Address offset: $03

	0	0	0	0	0	0	FRZ1	FRZ0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – ATDxCTL3

Address offset: $03

	0	***S8C***	***S4C***	***S2C***	***S1C***	***FIFO***	FRZ1	FRZ0
Reset:	0	0	1	0	0	0	0	0

MC9S12DP256 – ATDxCTL3

S8C/S4C/S2C/S1C – Conversion Sequence Length

These bits represent a binary value, which is the length of the conversion sequence. The conversion sequence length coding table in the ATDxCTL3 register description in the MC9S12DP256 Technical Data Book lists the coding combinations.

FIFO – Result register FIFO mode

This bit determines if the result registers map to the conversion sequence.

Reset Condition

Out of Reset the conversion length sequence is set to 4 and the FIFO mode is disabled. This operation identical to the 68HC912DG128.

ATD Control Register 4:

Address offset: $04

	RES10	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
Reset:	0	0	0	0	0	0	0	1

68HC912DG128 – ATDxCTL4

Address offset: $04

	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
Reset:	0	0	0	0	0	1	0	1

MC9S12DP256 – ATDxCTL4

SRES8 – A/D Resolution select

This bit determines the resolution of the ATD conversion and the result register. The MC9S12DP256 reset default is 10-bit conversion mode.

Reset Condition

On the MC9S12DP256 the reset default resolution is 10-bit and the pre-scale value initialized to 6. On the 68HC912DG128 the reset default resolution is 8-bit and the pre-scale is set to 2. (On both devices the pre-scaler is further divided by 2)

ATD Control Register 5:

Address offset: $05

	0	S8CM	SCAN	MULT	CD	CC	CB	CA
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – ATDxCTL5

Address offset: $05

	DJM	***DSGN***	SCAN	MULT	0	CC	CB	CA
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – ATDxCTL5

DJM – Result Register Data Justification Mode

This bit determines how the converted result maps into the result register (left or right justified).

DSGN – Signed/Unsigned Result Data Mode

This bit determines if the result of the conversion is signed or unsigned.

CC/CB/CA – Analog Input Channel Select code

These bits are used to select the analog input channel that is to be converted (if MULT=0) and the first channel to be converted in a sequence (if MULT=1). The 68HC912DG128 has an additional CD control bit as the channel selection and sequence selection is slightly different. On the MC9S12DP256 the S8CM bit has been replaced by conversion length bits in the ATDxCTL3 register. Refer to MC9S12DP256 Technical Data Book, MC9S12DP256/D for details.

Reset Condition

Out of reset the device is configured for unsigned, left justified which is identical to the 68HC912DG128.

ATD Status Register High:

Address offset: $06

	SCF	0	0	0	0	C2	C1	C0
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – ATDxSTAT0

Address offset: $06

	SCF	0	***ETORF***	***FIFOR***	0	C2	C1	C0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – ATDxSTAT0

ETORF – External Trigger Overrun Flag

This flag is associated with edge trigger mode option. It is set if additional active edges are detected during a conversion sequence.

FIFOR – FIFO over Run Flag

This bit indicates that a result register has been written to before its associated conversion complete flag has been cleared.

Reset Condition

Out of reset the register is identical to the 68HC912DG128.

ATD Test Module Test Register High:

Address offset: $08

	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
Reset:	***0***	0	0	0	0	0	0	0

68HC912DG128 – ATDxTESTH

Address offset: $08

	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
Reset:	***1***	0	0	0	0	0	0	0

MC9S12DP256 – ATDxTEST0

The registers are identical apart from the reset condition of SAR9.

ATD Test Module
Test Register Low:

Address offset: $09

	SAR1	SAR0	***RST***	***TSTOUT***	***TST3***	***TST2***	***TST1***	***TST0***
Reset:	0	0	0	0	0	0	0	0

68HC912DG128 – ATDxTESTL

Address offset: $09

	SAR1	SAR0	***0***	***0***	***0***	***RST***	***ATDCLK***	***SC***
Reset:	1	0	0	0	0	0	0	0

MC9S12DP256 – ATDxTEST1

RST – Test Mode Reset Bit

This bit causes the ATD Module to reset itself. The bit is identical on the 68HC912DG128, but its bit position has changed.

TSTOUT – Multiplex Output of TST[3:0]

This bit is not available on the MC9S12DP256.

TST[3:0] – Test Bits 3 to 0

These bits are not available on the MC9S12DP256.

ATDCLK – Display the state of the ATD conversion clock

This bit can be used to display the ATDCLK in test mode.

SC – Special Channel Conversion Mode

This bit is used to select the source of the ATD input channel. Conversions can be performed on any analog input channel (normal mode) or on one of the special channels (used to test the ATD module and convert reference potentials). This bit has the same functionality as the CD bit in the ATDxCTL5 register on the 68HC912DG128.

Reset Condition

Out of reset the register is identical to the 68HC912DG128.

ATD Input Enable Mask register: This register has been added to the MC9S12DP256. It gives the user additional control over the use of the port. It allows each digital input buffer to be enabled/disabled on a per pin basis. Refer to the MC9S12DP256 Technical Data Book, MC9S12DP256/D for further details.

Address offset: $0D

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – ATDxDIEN

Reset Condition

Out of reset the digital input buffers are disabled. (Reading PORTAD1 returns undetermined data).

Port Data Register:

Address offset: $0F

	PADx7	PADx6	PADx5	PADx4	PADx3	PADx2	PADx1	PADx0
Reset:	–	–	–	–	–	–	–	–

68HC912DG128 – PORTADx

Address offset: $0F

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reset:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

MC9S12DP256 – PORTADx

Reset Condition

Out of reset the digital input buffers of the MC9S12DP256 are disabled. The port returns the value 0xFF. On the 68HC912DG128 the port is configured for digital input.

ATD Conversion result Registers

Address offset: $10–$1F

ADRxnH	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
ADRxnL	BIT7	BIT6	0	0	0	0	0	0
Reset:	U	U	U	U	U	U	U	U

68HC912DG128

Address offset: $10–$1F

ATDxDRnH10 bit 8 bit	BIT15 BIT7	BIT14 BIT6	BIT13 BIT5	BIT12 BIT5	BIT11 BIT3	BIT10 BIT2	BIT9 BIT1	BIT8 BIT0
ATDxDRnL10 bit 8 bit	BIT7 1	BIT6 0	0 0	0 0	0 0	0 0	0 0	0 0
Reset:	U	U	U	U	U	U	U	U

MC9S12DP256 – Left Justified

Address offset: $10–$1F

ATDxDRnH10 bit 8 bit	0 0	0 0	0 0	0 0	0 0	0 0	BIT9 0	BIT8 0
ATDxDRnL10 bit 8 bit	BIT7 BIT7	BIT6 BIT6	BIT5 BIT5	BIT4 BIT4	BIT3 BIT3	BIT2 BIT2	BIT1 BIT1	BIT0 BIT0
Reset:	U	U	U	U	U	U	U	U

MC9S12DP256 – Right Justified

The ATD conversion results are stored in 8 result registers. The data for the 68HC912DG128 can be stored in several different formats depending on the control bits is the ADCxCTL5 register. Refer to the ADC conversion result register description for additional details.

Byte Data Link Controller (BDLC)

Introduction

For complete detailed information on the operation of the BDLC, please refer to the BDLC Reference Manual (BDLCRM/D).

The BDLC module is a byte-level serial messaging interface that has been designed to meet Society of Automotive Engineers (SAE) J1850 Class B Data Communication serial communications protocol for Variable Pulse Width (VPW) encoded messaging. The VPW portion of the J1850 specification is used by General Motors and Chrysler, enabling the BDLC to be used to communicate to systems from either of these manufacturers. Since the BDLC is only designed to send one byte at a time, the user must take into account many of the requirements of the J1850 protocol when writing their drivers, such as the total byte count of the message. The BDLC module does handle all of the network access, bit arbitration, message framing, and error detection.

This section compares the BDLC module of the MC9S12DP256 with that of the 68HC912B32, as this is the closest derivative of the HC12 family to contain a BDLC module.

The base addresses for the BDLC registers are as follows:

68HC912B32	MC9S12DP256
$F8	$E8

Summary of Additional Functions on MC9S12DP256

The functionality of the BDLC module has not changed from previous HC12 designs to the MC9S12DP256 version. Some unused features have been removed.

- The BDLC shares its TxB and RxB pins with Port M[1:0] and RxCAN and TxCAN of CAN0. The two least significant bits of Port M serve the same function as the two least significant bits of Port DLC on the 68HC912B32.
- Expanded I/O Pin control now handled by the Port Integration Module (PIM), including prioritization of access to pins by active modules. The PIM arbitrates between modules sharing pin resources. Please refer to the **Port Integration Module (PIM)** section for more details.
- New status register/bit to indicate when the module is transmitting or receiving.

Register Block Comparison

BDLC Control Register1 and Rate Select Register:

Address offset: $00

	IMSG	CLKS	***R1***	***R0***	0	0	IE	WCM
Reset:	1	1	1	0	0	0	0	0

68HC912B32 – BCR1

Address offset: $00

	IMSG	CLKS	***0***	***0***	0	0	IE	WCM
Reset:	1	1	0	0	0	0	0	0

MC9S12DP256 – DLCBCR1

Address offset: $05

	0	0	***R5***	***R4***	***R3***	***R2***	***R1***	***R0***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – DLCBRSR

The rate select register in the MC9S12DP256 determines the divider prescaler value for the mux interface clock (f_{bdlc}). The prescaler value has been increased to accommodate the faster e-clock frequencies possible with the MC9S12DP256. In the 68HC912B32, the prescaler value is determined by only two bits, R1 and R0, which are located in BDLC control register 1.

BDLC State Vector Register:

Name change of register only, from BSVR to DLCBSVR.

BDLC Control Register2:

Address offset: $02

	ALOOP	DLOOP	RX4E	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
Reset:	1	1	1	0	0	0	0	0

68HC912B32 – BCR2

Address offset: $02

	SMRST	DLOOP	RX4E	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
Reset:	0	1	1	0	0	0	0	0

MC9S12DP256 – DLCBCR2

ALOOP – Analog Loopback Mode

This feature has been removed.

SMRST – BDLC State Machine Reset

This new bit allows the user to reset the BDLC state machines to an initial state after the user puts the off-chip analog transceiver in loop back mode.

BDLC Data Register: Name change of register only, from BDR to DLCBDR.

BDLC Analog Round Trip Delay Register:

Address offset: $04

	ATE	RXPOL	0	0	BO3	BO2	BO1	BO0
Reset:	1	1	0	0	0	1	1	1

68HC912B32 – BARD

Address offset: $04

	0	RXPOL	0	0	BO3	BO2	BO1	BO0
Reset:	1	1	0	0	0	1	1	1

MC9S12DP256 – DLCBARD

ATE – Analog Transceiver Enable

This feature has been removed.

BDLC Control Register:

Address offset: $05

	0	0	0	0	0	***BDLCEN***	PUPDLC	RDPDLC
Reset:	0	0	0	0	0	0	0	0

68HC912B32 – DLCSCR

Address offset: $06

	0	0	0	***BDLCE***	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – DLCSCR

The BDLCEN bit from the 68HC912B32 device has been renamed (BDLCE) and relocated (bit 4 of the DLCSCR register) but serves the same function of enabling or disabling the BDLC module for power savings.

BDLC Status Register:

Address offset: $07

	0	0	0	0	0	0	0	***IDLE***
Reset:	0	0	0	0	0	0	0	0

MC9S12DP256 – DLCBSTAT

This new register indicates the status of the BDLC. The IDLE bit indicates when the module is transmitting or receiving data.

Background Debug Module (BDM)

Introduction

The BDM is a single wire background debug system implemented in on-chip hardware for minimal CPU intervention. The breakpoint sub module provides hardware breakpoints that are used to debug software on the CPU by comparing actual addresses and data to predetermined data in setup registers.

This section compares the BDM module and breakpoint module of the MC9S12DP256 with that of the 68HC912DG128.

The base addresses for the BDM registers are as follows:

68HC912DG128	MC9S12DP256
$FF00	$FF00

Summary of Additional Functions on MC9S12DP256

- Security

  The MC9S12DP256 has additional security that prevents the contents of the FLASH and EEPROM from being Read or Written and blocks out BDM communications. The 68HC912DG128 has limited security that blocks out BDM communications.
- Freeze mode

  This is not actually a new feature as the ability to freeze module clocks when entering background mode in order to assist emulation is supported on the 68HC912DG128. On the MC9S12DP256 a common terminology has been adopted and there are FRZ bits in the ECT, PWM and ATD registers.
- Full breakpoint mode

  The MC9S12DP256 can enter BDM or execute an SWI on a breakpoint. On the 68HC912DG128, a breakpoint causes the device to only enter BDM mode.
- Additional compares

  The MC9S12DP256 allows compare on different data and address configurations, including 16K pages. This feature permits full support for page breakpointing.

Register Block Comparison

BDM Status register:

Address offset: $01

Read:	ENBDM	BDMACT	ENTAG	SDV	TRACE	CLKSW	0	0
Write:								

68HC912DG128 – STATUS

Address offset: $01

Read:	ENBDM	BDMACT	ENTAG	SDV	TRACE	CLKSW	***UNSEC***	0
Write:								

MC9S12DP256 – BDMSTS

UNSEC – Unsecure

If the user resets into single chip mode, with the system secured, the UNSEC bit in the BDMSTS register is cleared and the secure BDM firmware lookup table is placed in the memory map with the standard BDM firmware. This firmware verifies that the FLASH and EEPROM are erased and if so sets the UNSEC bit and jumps to the start of the standard BDM firmware. With the UNSEC bit set the user can change the state of the SEC bits in the on chip flash to unsecure the device. If the FLASH and/or EEPROM are not erased, when security is enabled, BDM communications are locked out.

NOTE: *There is a back door key that allows the user to bypass security, if the key is enabled and the 4 16-bit key comparison words are known. Refer to Flash section for further details.*

Breakpoint registers

The break point module has several additional features that allow greater control. Refer to the MC9S12DP256 Technical Data Book, MC9S12DP256/D for details.

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