

Application Note

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*Configuring the System and
Peripheral Clocks in the
MC9S08GB/GT*

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Introduction

This application note addresses the features and usage of the internal clock generator (ICG) module residing in the MC9S08GB/GT Family of microcontrollers. It will describe initialization and usage in its various modes of operation and address clock configurations for the MCU peripherals.

Features of the ICG Module

The ICG module provides the system clock to the MC9S08GB/GT microcontroller. **Figure 1** is a block diagram showing a functional view of the ICG module. This module provides multiple selections for system clock sources, allowing the user to choose among system cost, precision, and performance needs. The module consists of four major functional blocks:

- Oscillator block
- Internal reference generator (IRG)
- Frequency-locked loop (FLL)
- Clock select block



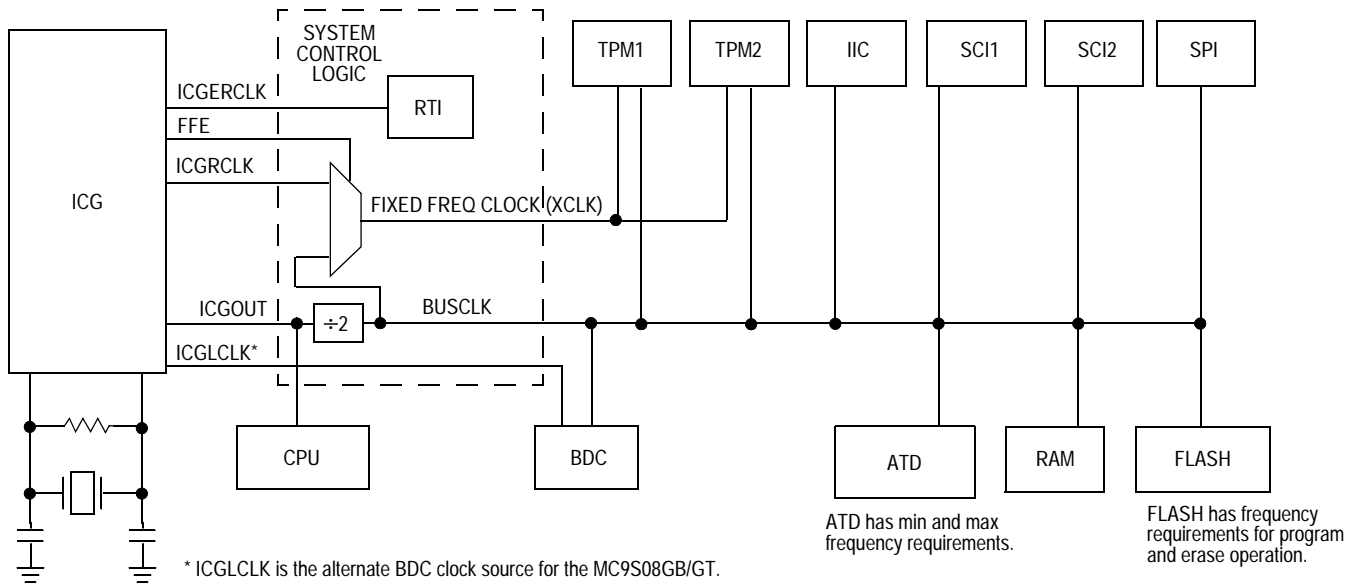


Figure 1. System Clocks Block Diagram

The ICG provides three separate clock output signals:

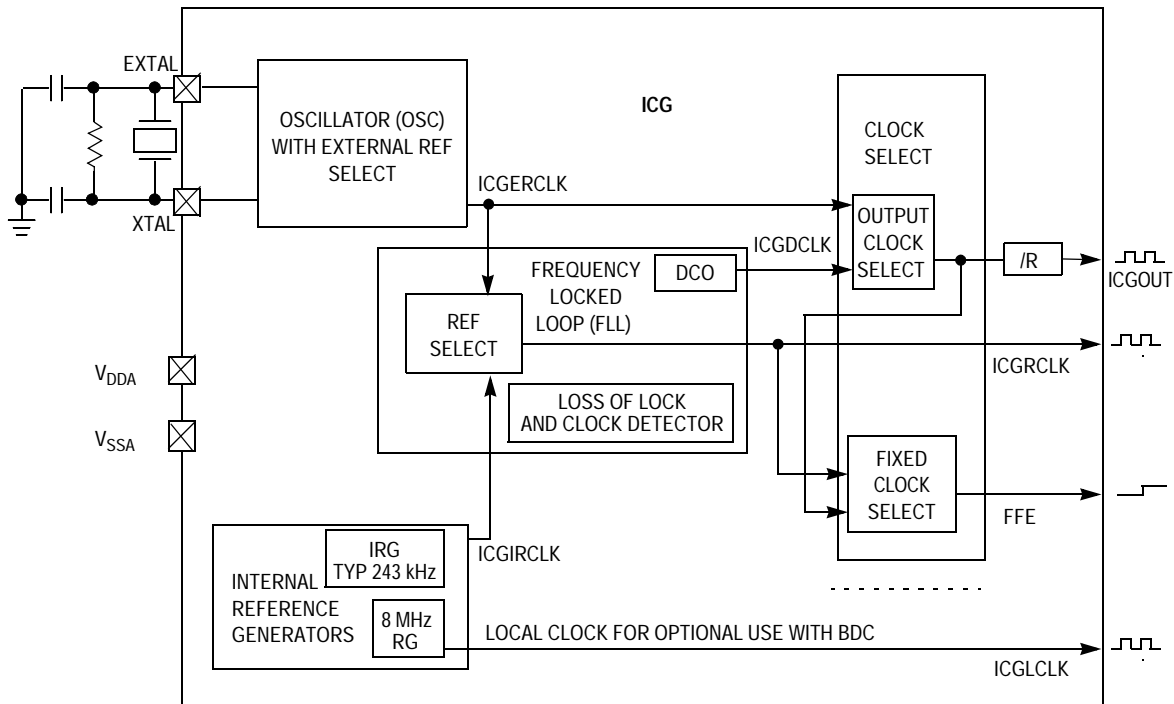
- ICGOUT — The main CPU clock which is divided by 2 to create the bus clock
- ICGRCLK — The reference clock for the FLL; is available for use with certain peripherals under certain conditions
- ICGLCLK — An optional clock source for the background debug controller (BDC); is fixed at 8 MHz, $\pm 30\%$

Modes of the ICG

The ICG has five modes of operation

- Off
- Self-clocked mode (SCM)
- FLL engaged-internal reference (FEI)
- FLL bypassed-external reference (FBE)
- FLL engaged-external reference (FEE)

Figure 2 is a top-level diagram that shows the functional organization of the internal clock generation (ICG) module.



NOTES:
1. See chip level clock routing diagram for specific use of ICGCLK, FFE, ICGLCLK, ICGERCLK, ICGIRCLK.

Figure 2. ICG Block Diagram

Mode 1:
Off

Mode 1, off, is the powered-down state of the ICG. The output clock, ICGOUT, is held in a static or stopped state. This mode is entered when a STOP instruction is executed, and it is exited upon waking up from stop. Figure 3 shows the stop mode recovery states of the ICG.

In the case of stop1 and stop2 modes, off mode is exited directly into SCM. In the case of stop3, if a reset is used to exit stop, SCM is entered. If an interrupt is used to exit stop3, SCM is entered unless FBE mode was selected prior to entering stop mode. If FBE was selected, the ICG module will hold ICGOUT static until the external clock source is stable. If FEI or FEE was selected upon entering stop3, then SCM is entered with the frequency retained from the pre-stop settings. Then the desired mode is entered when the FLL is stable.

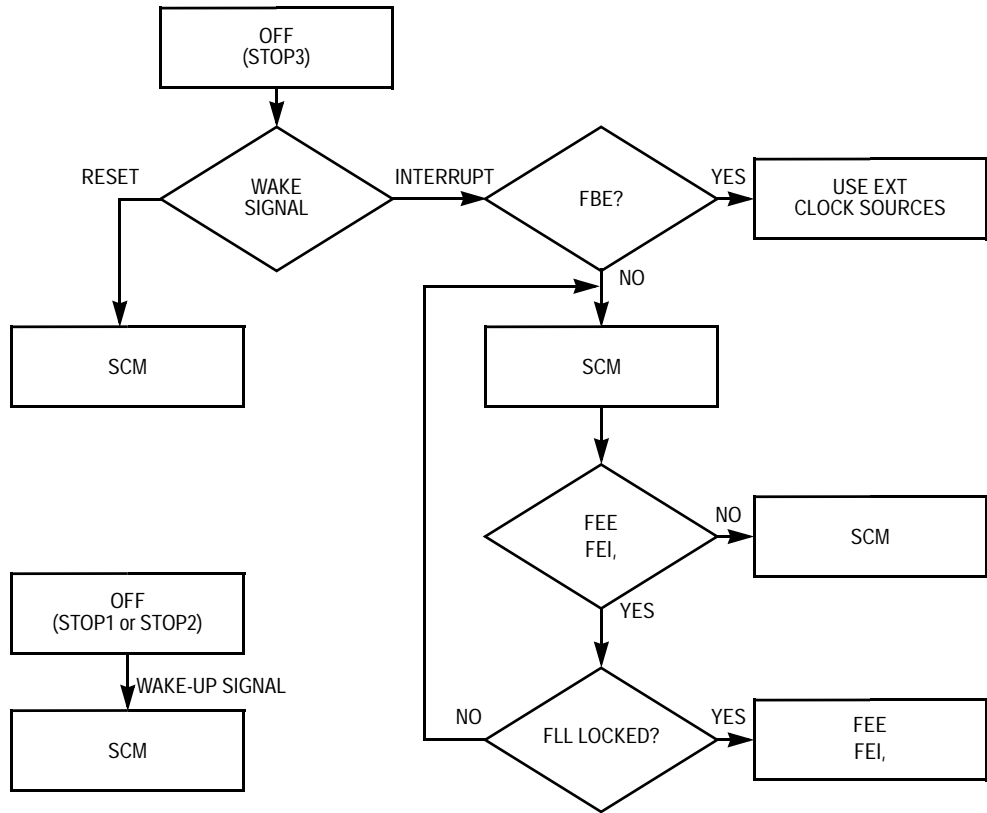


Figure 3. Stop Mode Recovery

*Mode 2:
Self-Clocked Mode
(SCM)*

Mode 2, SCM, is the self-clocked default mode. In this mode, the FLL loop is opened and the digitally controlled oscillator (DCO) is used as a stand-alone clock source. ICGOUT will be clocked at approximately 8 MHz, yielding a bus clock of approximately 4 MHz. No external oscillator components are required for this mode.

SCM is the ICG default mode of operation from reset. This mode requires no software intervention or external components to control the ICG. It enables the normal use of I/O port G bits 1 and 2, as there is no requirement for connections to XTAL or EXTAL. Use of this mode is limited to systems where timing requirements are very flexible.

SCM is entered when any of the following four conditions occur:

- After any reset.
- Exiting stop mode if CLKS bits in the ICG control register are not equal to 10. If CLKS bits = x1, the ICG will temporarily enter this state until the DCO becomes stable.
- CLKS bits are written from x1 to 00.
- CLKS bits = x1 and the external reference clock is not detected (ICGERCLK). In other words, the external reference clock is not stable or its frequency is too low and the external clock is lost.

The frequency of the ICG will be approximately 8 MHz. This ICGOUT frequency can be varied from 8 MHz to 40 MHz by writing a new value into the ICG filter registers (ICGFLTU:ICGFLTL). The value and frequency are related in direct proportion to each other. Only during SCM can the filter registers be written. In all other modes, the filter registers are read-only.

Mode 3:
FLL Engaged-Internal
Reference (FEI)

Mode 3, FEI, is used to provide MCU frequencies that are programmable multiples of the 243-kHz internal reference clock (ICGIRCLK). No external oscillator components are required for this mode.

To construct an inexpensive, but very functional, system from an ICG point of view, the designer can elect to use mode 3, internal self-clocked mode. There are advantages and disadvantages when using this mode of operation.

The main advantage of this mode is that the system requires no external oscillator components. Also, using mode 3 frees the XTAL and EXTAL pins normally associated with the external oscillator to be used as general-purpose I/O. Another advantage of using this internal oscillator is that it starts up very quickly at power-up time or upon recovery from a STOP instruction. Mode 3 uses the FLL to create frequencies programmable in multiples of the internal 243-kHz reference clock.

The disadvantage of using this mode is the initial accuracy of the internal reference generator. It can vary as much as $\pm 25\%$, however it can be trimmed by user software. When using the ICG in untrimmed self-clocked mode, the MCU is limited to 75% of the maximum 20 MHz bus frequency. This is because at the worst case untrimmed internal reference, you would not want to clock the MCU faster than the maximum specified bus frequency.

Trimming the internal reference generator is beyond the scope of this document and will be discussed in another application note, Freescale document number AN2496/D: *Calibrating the MC9S08GB/GT Internal Clock Generator (ICG)*. Suffice to say, the internal oscillator can be trimmed to $\pm 25\%$ by writing an 8-bit value to the ICG trim register. By using a known timing reference input to the microcontroller and user software, the internal reference oscillator can be accurately calibrated with a resolution of approximately 0.2%.

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