

Freescale Semiconductor

56F807 Product Brief

The 56F807 is a member of the 56800 core-based family of Digital Signal Controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F807 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

BENEFITS

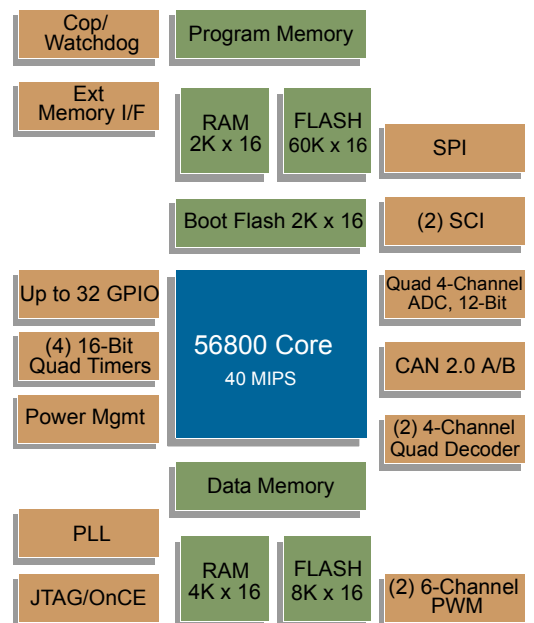
- On-board voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage
- Flash memory is engineered to provide reliable, non-volatile memory storage, eliminating the need for external storage devices
- Easy to program with flexible application development tools
- Simple updating of Flash memory through SPI, SCI or OnCE™, using on-chip boot loader
- Program can boot directly from Flash
- Supports multiple processor connections
- Patented distortion correction in PWM for design risk and better performance control
- PWM and ADC modules are tightly coupled to reduce processing overhead
- Low voltage interrupts protect the system during brownout or power failure
- Simple interface with other asynchronous serial communication devices and off-chip EE memory

56800 CORE FEATURES

- Efficient 16-bit 56800 controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

EXAMPLE APPLICATIONS

- Conveyors
- UPS
- Servo drives
- Fuel management systems
- Lifts/elevators/cranes
- Underwater acoustics
- Industrial frequency inverters
- Noise cancellation
- General purpose devices



MEMORY FEATURES

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip Memory including a low-cost, high-volume Flash solution
 - 60K x 16-bit words of Program Flash
 - 2K x 16-bit words of Program RAM
 - 8K x 16-bit words of Data Flash
 - 4K x 16-bit words of Data RAM
 - 2K x 16-bit words of Boot Flash
- Off-chip memory expansion capabilities
 - As much as 64K x 16 bits of data memory
 - As much as 64K x 16 bits of program memory

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

56F807 PERIPHERAL CIRCUIT FEATURES

- Two Pulse Width Modulator (PWM) modules, each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes
- Four 12-bit Analog-to-Digital Converters (ADCs), supporting two simultaneous conversions; ADC and PWM modules can be synchronized
- Two Quadrature Decoders
- Four dedicated general purpose Quad Timers
- CAN 2.0 A/B module
- Two Serial Communication Interfaces (SCI)
- Serial Peripheral Interface (SPI)
- Computer Operating Properly (COP)/Watchdog timer
- Two dedicated external interrupt pins
- 14 multiplexed General Purpose I/O (GPIO) pins, 18 multiplexed GPIO pins
- External reset pin for hardware reset
- External reset output pin for system reset
- JTAG/OnCE™ for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer

PRODUCT DOCUMENTATION

56800 Reference Manual	Detailed peripheral description of the 56800 architecture, 16-bit core processor and the instruction set Order Number: DSP56800FM
56F80x User Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F802, 56F803, and 56F807 Order Number: DSP56F801-7UM
56F807 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions Order Number: DSP56F807

ORDERING INFORMATION

PART	DSP56F807
PACKAGES	160 LQFP (80 MHz) 160 MBGA (80 MHz)
ORDER NUMBERS	DSP56F807PY80 DSP56F807VF80
SUPPLY VOLTAGE	3.0V - 3.6V