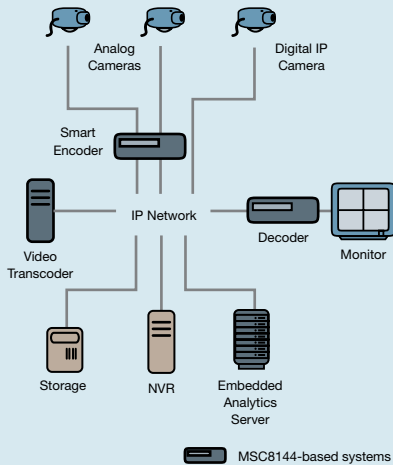




## Intelligent Embedded Open-IP System



## Open-IP Surveillance Systems

The introduction of Open-IP Surveillance systems allows for a host of new features and efficiencies. These include: standard, cost-effective networking, high reliability, availability, accessibility and integration with other security and business applications.

With the proliferation of Open-IP Surveillance systems there is a need to automate a large portion of the video monitoring. This may be done by deploying intelligent video systems that utilize sophisticated algorithmic software to analyze the video stream content (i.e. video analytics). Embedded intelligent systems provide the benefits of lower cost and power, accelerating market acceptance and mass deployment.

The unparalleled compute performance of the MSC8144 multi-channel media processor enables its use in a wide range of security applications. These include video encoders, transcoders, HD smart cameras, analytics servers and digital viewing stations. All of these applications use one or more of the following video algorithms: analytics, encoding/decoding/transcoding and pre- and post-processing. Networking and security (encryption) stacks are also required.

The system diagram shows a robust embedded intelligent Open-IP Surveillance system, highlighting the targeted MSC8144 applications.



## MSC8144 Features

- Four fully programmable StarCore™ SC3400 DSP cores, each running at up to 1 GHz for a 4 GHz-equivalent performance
- Each subsystem includes:
  - SC3400 DSP core architecture optimized for media processing
  - 16 KB instruction cache, 32 KB data cache
  - Memory management unit (MMU) for memory protection and address translation
  - Debug, profiling, interrupt, timers and profiling unit
- 10.5 MB embedded memory—the industry's largest—in a single package
- QUICC Engine™ communications technology—dual RISC-based packet-processing engine
- 128 KB shared L2-cache
- Supports next-generation and legacy interfaces:
  - 1x/4x Serial RapidIO®
  - Packet
    - .. Dual Ethernet controllers supporting RGMII, SGMII, MII, RMII, SMII
    - .. UTOPIA L2 50 MHz 8-/18-bit slave, supporting AAL1, AAL2, AAL5 ATM adaptation layers in firmware
  - TDM—2048 DS-0 channels
  - PCI 2.2 32-bit at 66 MHz
- 16-/32-bit DDRI/DDRII at 400 MHz data rate, 32 channels DMA
- Debug, boot, configuration:
  - I<sup>2</sup>C, UART, EOnCE/JTAG
- Package/voltage/process:
  - 29 mm x 29 mm FCPBGA, 1 mm pitch
  - Core nominal voltage—1V
  - M3 memory voltage—1.2V
  - I/O voltage—1.8V/2.5V/3.3V
  - 90 nm SOI

## Development Tools

### Freescale CodeWarrior® Tools

- Integrated development environment
- ANSI 'C', 'C++' optimizing compilers
- Source level debugger
- SmartDSP OS multi-core, royalty-free operating system
- Integrated device drivers
- Integrated cycle and functional accurate simulators

### Enea® OSEck RTOS

- OSEck real-time kernel
- Preemptive multi-tasking
- Multi-core DSP support
- OSEck soft kernel environment, link handler and illuminator
- Board support package (BSP)

## Learn More:

For current information about Freescale products and documentation, please visit [www.freescale.com](http://www.freescale.com).