

32-bit Power Architecture® Automotive Software and Tools Ecosystem																	
<b>Software and Hardware Tools</b>																	
Compilers	√	√	√														
Debugger		√	√				√	√	√								
Simulator		√	√				√						√	√			
Initialization tool	√																
Modeling and code generation										√	√						√
Evaluation boards	√							√	√			√				√	
<b>Run-Time Software</b>																	
eTPU libraries	√																
DSP libraries	√																
Motor control libraries	√																
AUTOSAR low level drivers	√			√	√												
AUTOSAR OS	√			√	√												
Core self-test	√																
CAN, LIN and FlexRay™ stacks				√	√	√											

**CodeWarrior™ Tools for MPC55xx v2.3 (Special Edition or Evaluation Version)**

This version of the product contains the compiler and build tools only. A fully integrated solution, which includes a debugger, is available for purchase from several third-party tools providers. CodeWarrior tools offer a range of individual products and services to help you easily migrate to Freescale's MPC5500 family. To expand beyond the 128 KB limit upgrade to a "Standard" or "Professional" Development Suite license.

This version contains CodeWarrior development suite for EPPC Build Tools for MPC55xx family and P&E PowerPC Nexus Starter Edition. In addition, debugger "Windows-hosted" support has been added for MPC5517/16/15/14, MPC560xB, MPC560xP, MPC560xS and MPC563xM processors.

**RAppID: Rapid Application Initialization and Documentation**

RAppID, a family of graphical development tools for the MPC5XXX family of controllers built on Power Architecture® technology, enables the user to quickly and easily configure the controller and generate complete documentation. It can also be used as a learning tool to gain an understanding of the controller and its peripherals. RAppID not only generates C code for initializing the registers, but provides a system initialization function that brings the controller up in an orderly sequence. Use RAppID to help save time and become an expert on the MPC5XXX family.

**MPC55xxEVB: MPC55xx Evaluation Board**

The MPC55xxEVB Evaluation Kits include everything necessary to begin development with the MPC55xx family of microcontrollers. A comprehensive set of hardware and software development tool options are available, including a flash programmer, initialization tools and an assembly-level debug tool.

**MPC5510KIT144/208 and MPC5510DEMO**

Provides development platform for MPC5510 family of MCUs. Includes CodeWarrior for MPC55xx v2.3, P&E Multilink, MPC5517 samples and technical documentation.

**MPC56XXXKITxxxS**

Provides development platform for either MPC560xB, MPC560xP, MPC560xS or MPC563xM MCUs. Kit includes CodeWarrior for MPC55xx v2.3, P&E Multilink, samples and technical documentation.

**AUTOSAR OS and MCAL Evaluation Package**

Evaluate Freescale's AUTOSAR-compliant OS and Microcontroller Abstraction Layer (MCAL) on the MPC5500 family. The evaluation package includes the OS, MCAL drivers and a configuration tool.



**Automotive 32-bit Microcontrollers**  
Product map

# Automotive 32-bit Microcontrollers

## Driving automotive excellence with MPC56xx and MPC55xx MCUs

The MPC56xx and MPC55xx families of 32-bit microcontrollers built on Power Architecture® technology, are designed for engine management, advanced driver assistance, central body and gateway applications. The MPC56xx and MPC55xx families offer significant benefits to automotive designers:

- Software and hardware compatibility from low to high end
- Scalability among different core versions and product features
- Embedded flash experience implemented in a high-density, floating-gate technology
- Unmatched efficiency—parallel processing in conjunction with sophisticated peripheral sets leverages Power Architecture tools and software ecosystem

A = -55°C to +125°C  
 C = -40°C to +85°C  
 V = -40°C to +105°C  
 M = -40°C to +125°C

Device	Core Platform	Program Flash	SRAM	DMA	EEPROM	eSC/LINFlex	DSPI	CAN	PC	FlexRay™	Ethernet (100Base-T)	MLB	Ext. Bus	Nexus	ETPU	eMIOS	PIT	GPIO	ADC	Voltage	Temp Range	Frequency Range	Package Options	In Production	Market Focus		
<b>MPC56XX Family</b>																											
MPC5604B	Power Architecture® e200z0	512 KB	32 KB		64K Data Flash	4	3	3	1					Yes (emul-only package)		56-ch., 16-bit	✓	Up to 121	36-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP, 144 LQFP, 208 MAPBGA (emul-only)		Body/Gateway		
MPC5603B	Power Architecture e200z0	384 KB	28 KB		64K Data Flash	4	3	3	1					Yes (emul-only package)		56-ch., 16-bit	✓	Up to 121	36-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP, 144 LQFP		Body/Gateway		
MPC5602B	Power Architecture e200z0	256 KB	24 KB		64K Data Flash	4	3	2	1					Yes (emul-only package)		56-ch., 16-bit	✓	Up to 121	36-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP, 144 LQFP		Body/Gateway		
MPC5604C	Power Architecture e200z0	512 KB	32 KB		64K Data Flash	4	3	6	1					Yes (emul-only package)		28-ch., 16-bit	✓	Up to 77	28-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP, 208 MAPBGA (emul-only)		Body/Gateway		
MPC5603C	Power Architecture e200z0	384 KB	32 KB		64K Data Flash	4	3	6	1					Yes (emul-only package)		28-ch., 16-bit	✓	Up to 77	28-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP		Body/Gateway		
MPC5602C	Power Architecture e200z0	256 KB	32 KB		64K Data Flash	3	3	6	1					Yes (emul-only package)		28-ch., 16-bit	✓	Up to 77	28-ch., 10-bit	3.3V and 5V	C, V, M	Static to 64 MHz	100 LQFP		Body/Gateway		
MPC5634M	Power Architecture e200z3	1.5 MB	94 KB	32-ch.	Emulated in program flash	2	2	2	0					✓	32-ch.	16-ch., 24-bit	✓	Up to 114	Dual 34-ch., 12-bit	5V	M	40 MHz, 60 MHz, 80 MHz	144 LQFP, 176 LQFP, 208 MAPBGA, 496 CSP, Vertical Calibration Bus		Low-end Powertrain		
MPC5633M	Power Architecture e200z3	1 MB	64 KB	32-ch.	Emulated in program flash	2	2	2	0					✓	32-ch.	16-ch., 24-bit	✓	Up to 114	Dual 32-ch., 12-bit	5V	M	40 MHz, 60 MHz, 80 MHz	100 LQFP, 144 LQFP, 176 LQFP, 208 MAPBGA, 496 CSP, Vertical Calibration Bus		Low-end Powertrain		
MPC5632M	Power Architecture e200z3	768 KB	32 KB	32-ch.	Emulated in program flash	2	2	2	0					✓	32-ch.	8-ch., 24-bit	✓	Up to 105	Dual 32-ch., 12-bit	5V	M	40 MHz, 60 MHz, 80 MHz	100 LQFP, 144 LQFP, 496 CSP, Vertical Calibration Bus		Low-end Powertrain		
MPC5604P	Power Architecture e200z0	512 KB	40 KB	16-ch.	Emulated in program flash		4	1	0	2				✓			✓	Up to 108	Dual 13-ch., 10-bit	3.3V/5V	M	60 MHz	100 LQFP, 144 LQFP		Chassis, Safety		
MPC5603P	Power Architecture e200z0	384 KB	32 KB	16-ch.	Emulated in program flash		4	1	0	2				✓			✓	Up to 108	Dual 13-ch., 10-bit	3.3V/5V	M	60 MHz	100 LQFP, 144 LQFP		Chassis, Safety		
MPC5602P	Power Architecture e200z0	256 KB	24 KB	16-ch.	Emulated in program flash		4	1	0	2				✓			✓	Up to 108	Dual 13-ch., 10-bit	3.3V/5V	M	60 MHz	100 LQFP, 144 LQFP		Chassis, Safety		
<b>MPC55XX Family</b>																											
MPC5533	Power Architecture e200z3	768 KB	48 KB	32-ch.	Emulated in program flash	1	2	2					✓	3	32-ch.				192	40-ch., 1 x 12-bit	3.3V and 5V	M	40-80 MHz	208 MAPBGA, 324 PBGA	✓	Engine Management	
MPC5534	Power Architecture e200z3	1 MB	64 KB	32-ch.	Emulated in program flash	2	3	2					✓	3	32-ch.	24-ch., 24-bit			192	40-ch., 1 x 12-bit	3.3V and 5V	M	40-80 MHz	208 MAPBGA, 324 PBGA	✓	Engine Management	
MPC5553	Power Architecture e200z6	1.5 MB	64 KB	32-ch.	Emulated in program flash	2	3	2			✓		✓	3	32-ch.	24-ch., 24-bit			220	40-ch., 1 x 12-bit	3.3V and 5V	M	80-132 MHz	208 MAPBGA, 324 PBGA, 416 PBGA	✓	Engine Management	
MPC5554	Power Architecture e200z6	2 MB	64 KB	64-ch.	Emulated in program flash	2	4	3					✓	3	2 x 32-ch.	24-ch., 24-bit			256	40-ch., 1 x 12-bit	3.3V and 5V	M	80-132 MHz	416 PBGA	✓	Engine Management	
MPC5561	Power Architecture e200z6	1 MB	192 KB	32-ch.	Emulated in program flash	4	2	2		✓			✓	3		24-ch., 24-bit			150	40-ch., 1 x 12-bit	3.3V and 5V	C, M	80-132 MHz	324 PBGA		Advanced Driver Assistance	
MPC5565	Power Architecture e200z6	2 MB	80 KB	32-ch.	Emulated in program flash	2	3	3					✓	3	32-ch.	24-ch., 24-bit			192	40-ch., 1 x 12-bit	3.3V and 5V	M	80-132 MHz	324 PBGA	✓	Engine Management	
MPC5566	Power Architecture e200z6	3 MB	128 KB	64-ch.	Emulated in program flash	2	4	4			✓		✓	3	2 x 32-ch.	24-ch., 24-bit			256	40-ch., 1 x 12-bit	3.3V and 5V	C, M	80-144 MHz	416 PBGA	✓	Engine Management	
MPC5567	Power Architecture e200z6	2 MB	80 KB	32-ch.	Emulated in program flash	2	3	5		✓	✓		Emulated via eTPU	✓	3	32-ch.	24-ch., 24-bit			238	40-ch., 1 x 12-bit	3.3V and 5V	C, M	80-132 MHz	324 PBGA, 416 PBGA	✓	Engine Management
MPC5516G	Power Architecture e200z1+e200z0	1 MB	64 KB	16-ch.	Emulated in program flash	8	3	6	1	✓			Emulated via z0	✓	2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-80 MHz	144 LQFP, 208 MAPBGA		Central Body, Gateway	
MPC5516E	Power Architecture e200z1+e200z0	1 MB	64 KB	16-ch.	Emulated in program flash	6	3	5	1				Emulated via z0	✓	2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-66 MHz	144 LQFP, 208 MAPBGA		Central Body, Gateway	
MPC5516S	Power Architecture e200z1	1 MB	48 KB	16-ch.	Emulated in program flash	6	3	5	1					2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-66 MHz	144 LQFP, 208 MAPBGA		Central Body		
MPC5515S	Power Architecture e200z1	768 KB	32 KB	16-ch.	Emulated in program flash	6	3	5	1					2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-66 MHz	144 LQFP, 208 MAPBGA		Central Body		
MPC5514G	Power Architecture e200z1+e200z0	512 KB	64 KB	16-ch.	Emulated in program flash	8	3	6	1	✓			Emulated via z0	✓	2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-80 MHz	144 LQFP, 208 MAPBGA		Central Body, Gateway	
MPC5514E	Power Architecture e200z1+e200z0	512 KB	32 KB	16-ch.	Emulated in program flash	6	3	5	1				Emulated via z0	✓	2+	24-ch., 16-bit	8-ch., 32-bit		111, 144	40-ch., 1 x 12-bit	5V	C, V, M	48-66 MHz	144 LQFP, 208 MAPBGA		Central Body, Gateway	
<b>MPC5xx Family</b>																											
MPC555	Power Architecture RCPU	448 KB	28K RAM + 6 for TPU		EEE	2 SCI	1 QSPI	2 x TouCAN					✓		2 TPU3, 2 x 16-ch.	MIOS1 18-ch.	1-ch., 16-bit	Up to 89	2 QADC (10-bit A/D with 64 result registers each) 32 channels on chip	3.3 Vdc for core, 5.0 Vdc for flash	A, C, M	40 MHz	272-ball PBGA	✓	Engine Management		
MPC561	Power Architecture RCPU	0	32K RAM + 8 for TPU + 2 for DECRAM		EEE	2 SCI	1 QSPI	3 x TouCAN					✓	NEXUS debug port (class 3)	2 TPU3, 2 x 16-ch.	MIOS14 22-ch.	1-ch., 16-bit	Up to 89	2 QADC (10-bit A/D with 64 result registers each) 32 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
MPC562	Power Architecture RCPU	0	32K RAM + 8 for TPU + 2 for DECRAM		EEE	2 SCI	1 QSPI	3 x TouCAN					✓	NEXUS debug port (class 3)	2 TPU3, 2 x 16-ch.	MIOS14 22-ch.	1-ch., 16-bit	Up to 89	2 QADC (10-bit A/D with 64 result registers each) 32 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
MPC563	Power Architecture RCPU	512 KB	32K RAM + 8 for TPU + 2 for DECRAM		EEE	2 SCI	1 QSPI	3 x TouCAN					✓	NEXUS debug port (class 3)	2 TPU3, 2 x 16-ch.	MIOS14 22-ch.	1-ch., 16-bit	Up to 89	2 QADC (10-bit A/D with 64 result registers each) 32 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
MPC564	Power Architecture RCPU	512 KB	36K RAM + 8 for TPU + 2 for DECRAM		EEE	2 SCI	1 QSPI	3 x TouCAN					✓	NEXUS debug port (class 3)	2 TPU3, 2 x 16-ch.	MIOS14 22-ch.	1-ch., 16-bit	Up to 89	2 QADC (10-bit A/D with 64 result registers each) 32 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
MPC565	Power Architecture RCPU	1 MB	36K RAM + 10 for TPU + 4 for DECRAM		EEE	4 SCI	2 QSPI	3 x TouCAN + 1 J1850					✓	NEXUS debug port (class 3)	3 TPU3, 2 x 16-ch.	MIOS14 22-ch. + RTC	1-ch., 16-bit	Up to 98	2 QADC (10-bit A/D with 64 result registers each) 40 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
MPC566	Power Architecture RCPU	1 MB	36K RAM + 10 for TPU + 4 for DECRAM		EEE	4 SCI	2 QSPI	3 x TouCAN + 1 J1850					✓	NEXUS debug port (class 3)	3 TPU3, 2 x 16-ch.	MIOS14 22-ch. + RTC	1-ch., 16-bit	Up to 98	2 QADC (10-bit A/D with 64 result registers each) 40 channels on chip	2.6 Vdc for core, 5.0 Vdc for A/D and I/O	A, C, M	40 MHz or 56 MHz	388-ball PBGA	✓	Engine Management		
<b>MAC71XX Family</b>																											
MAC71x1	ARM7TDMI-S	512 KB	32 KB	16-ch.	32 KB	4	2	4	1				✓	2+		16-ch., 16-bit	10-ch., 24-bit	Up to 128	Up to 32-ch., 10-bit	3.3-5V	C, V, M	40-50 MHz	112 LQFP, 144 LQFP, 208 MAPBGA	✓	Body, Chassis, Cluster		
MAC71x2	ARM7TDMI-S	256 KB	16 KB	16-ch.	32 KB	3	2	2	1					2+		16-ch., 16-bit	10-ch., 24-bit	Up to 105	16-ch., 10-bit	3.3-5V	C, V, M	40-50 MHz	112 LQFP, 144 LQFP	✓	Body, Chassis, Cluster		
MAC71x6	ARM7TDMI-S	1 MB	48 KB	16-ch.	32 KB	4	2	4	1				✓	2+		16-ch., 16-bit	10-ch., 24-bit	Up to 128	Up to 32-ch., 10-bit	3.3-5V	C, V	40-50 MHz	112 LQFP, 144 LQFP, 208 MAPBGA	✓	Body, Chassis, Cluster		
<b>MAC72XX Family</b>																											
MAC72x2	ARM7TDMI-S	256 KB	20 KB	16-ch.	64 KB data flash	2	3	2	1				✓	3		8-ch., 16-bit	10-ch., 32-bit RTI 24-bit	Up to 102	Up to 16-ch., 12-bit	5V	C, V, M	50-70 MHz	100 LQFP, 144 LQFP	✓	Safety (Airbag)		
MAC72x1	ARM7TDMI-S	448 KB	32 KB	16-ch.	64 KB data flash	2	3	2	1				✓	3		16-ch., 16-bit	10-ch., 32-bit RTI 24-bit	Up to 102	Up to 16-ch., 12-bit	5V	C, V, M	50-70 MHz	100 LQFP, 144 LQFP	✓	Safety (Airbag)		

Note: specs given are for the largest package size stated.

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|--|--|---|---|
| <b>ADC</b> Analog-to-Digital Converter             | <b>eQADC</b> Enhanced Queued Analog-to-Digital Converter | <b>MAPBGA</b> Mold Array Process Ball Grid Array  | <b>PIT</b> Periodic Interrupt Timer     |
| <b>CAN</b> Controller Area Network                 | <b>ESCI</b> Enhanced Serial Communication Interface      | <b>mcPWM</b> Motor Control Pulse Width Modulation | <b>RAM</b> Random Access Memory         |
| <b>DMA</b> Direct Memory Access                    | <b>eTPU</b> Enhanced Timer Processing Unit               | <b>MLB</b> Media Local Bay                        | <b>RTC</b> Real-Time Clock              |
| <b>DSPI</b> Deserial Serial Peripheral Interface   | <b>GPIO</b> General Purpose Input/Output                 | <b>MOST</b> Media Oriented System Transport       | <b>RTI</b> Real-Time Interrupt          |
| <b>EEPROM</b> Electrically Erasable Programmable   | <b>I<sup>2</sup>C</b> Inter-Integrated Circuit           | <b>MPU</b> Memory Protection Unit                 | <b>SPI</b> Serial Peripheral Interface  |
| <b>eMIOS</b> Enhanced Multiple Input Output System | <b>LQFP</b> Low-Profile Quad Flat Package                | <b>PBGA</b> Plastic Ball Grid Array               | <b>SRAM</b> Static Random Access Memory |

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