2.1 Power ISA 2.03 VLE Extension

The VLE category exemplifies the breadth and adaptability of the Power Architecture model. VLE redefines encodings for many user instruction set architecture (UISA)-based instructions to fit into 16-bit opcodes. This approach allows the UISA to be introduced into environments that require a small code footprint and offers more efficient binary representations for embedded processors. This alternate encoding can not only reduce overall system cost but also can improve code performance by up to 30 percent over the standard Power ISA.

Rather than defining an entirely different ISA or supplanting the Power ISA, the VLE extension serves as a supplement that can improve code density to an application or to part of an application. The e200z0 core only implements the VLE instructions while the other cores may implement both the standard 32-bit Power ISA instructions as well as VLE.

The VLE set of alternate encodings is selected on an instruction-page basis. A single page-attribute bit selects between standard instruction encodings and VLE instructions for that page of memory. Pages of either configuration can be intermixed freely, allowing a combination of both types of encodings in an application. Instruction encodings in instruction pages marked as using the VLE extension are either 16- or 32-bits long and are aligned on 16-bit boundaries. Therefore, all pages marked as VLE must use big-endian byte ordering.

The programming model uses the same register set with both instruction encodings, although certain registers are not accessible by VLE instructions using the 16-bit formats. Not all CRs are used by condition setting or conditional branch instructions executing from a VLE instruction page. Furthermore, immediate fields and displacements differ in size and use due to more restrictive encodings imposed by VLE instructions.

Other than requiring big-endian byte ordering for instruction pages and the additional page attribute to identify whether the instruction page corresponds to a VLE section of code, VLE complies with the embedded category memory model. Likewise, the VLE extension complies with the Book III-E definitions of the exception and interrupt models, timer facilities, debug facilities and special-purpose registers (SPRs).

2.2 Power ISA 2.03 Signal Processing Engine (SPE)

The SPE supports real-time fixed-point and single-precision embedded numerics operations using the general-purpose registers. All arithmetic instructions that execute in the core operate on data in the GPRs, which have been extended to 64-bits to support SIMD vector instructions defined by the SPE category. These instructions operate on a vector pair of 16-bit or 32-bit data types and deliver vector and scalar results.

3 e200 Core Family Characteristics

Freescale's e200 family of synthesizable, high-efficiency cores, built on Power Architecture technology, is designed for cost-sensitive, embedded real-time applications. The licensable e200 cores include four versions of the e200 core family: the e200z0, e200z1, e200z3 and e200z6 cores. In 90 nm CMOS process technology, these cores range from 150 MHz to 300 MHz in performance. The cores offer low interrupt latency, low-power design through clock gating, variable cache sizes, variable MMU sizes, standard Nexus debug interface and an AMBA® AHB™ bus interface unit. The cores also may include Power ISA 2.03 features, such as SPE, single-precision floating-point unit (FPU) and VLE technology.

e200 Cores Available for Licensing					
e200z0	e200z1	e200z3		e200z6	
150 MHz	150 MHz	150 MHz		300 MHz	
4-stage	4-stage	4-stage		7-stage	
VLE	VLE/32-bit	VLE/32-bit		VLE/32-bit	
	MMU	MMU		MMU	
		FPU	SPE	FPU	SPE
				Up to 32K L1	

Note: Core frequency based on 90 nm process technology estimates

The Freescale e200 core family effectively addresses the needs of automotive, consumer, networking and industrial applications with increased system performance requirements in complex, real-time environments.

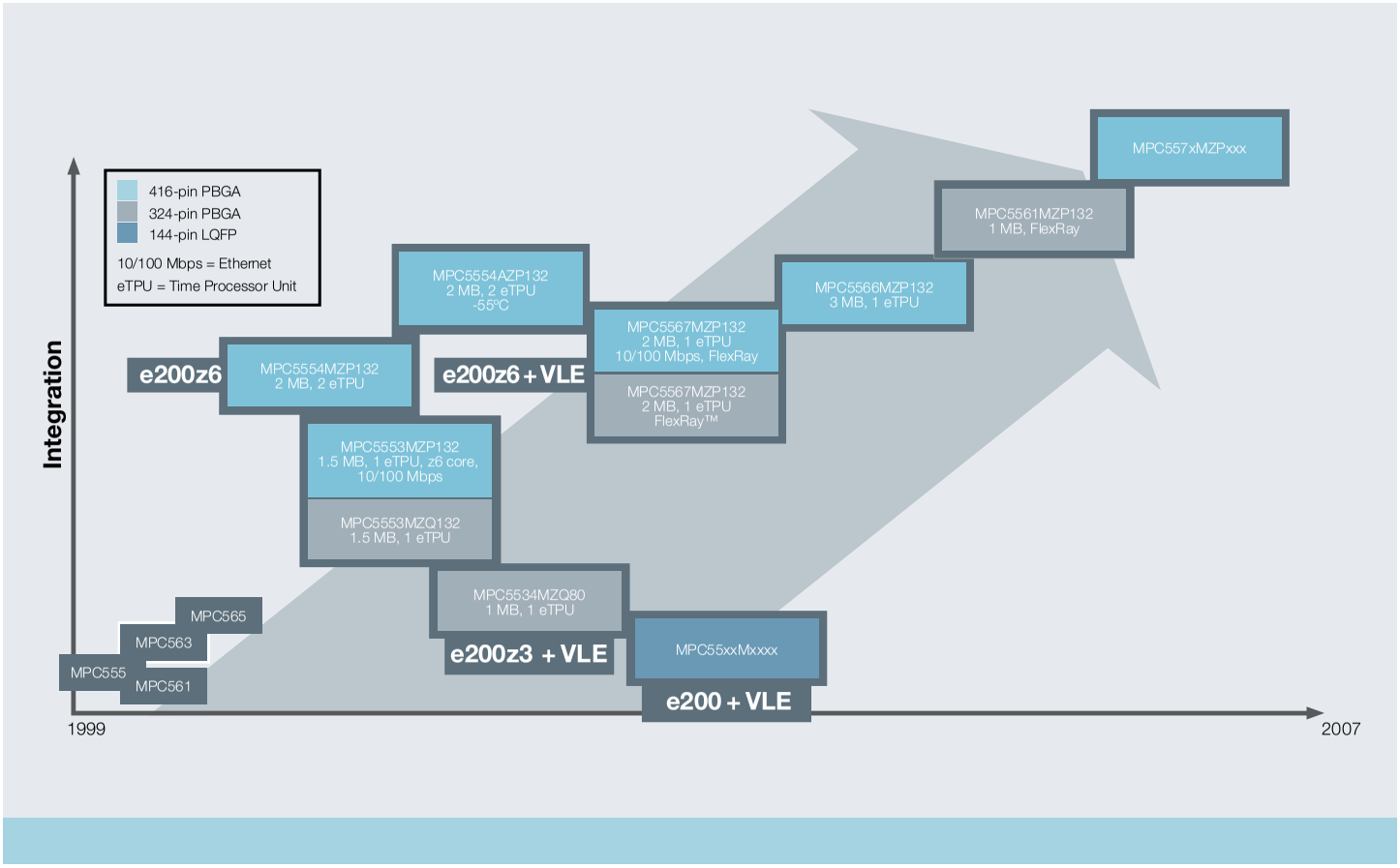
4 e200 Core SoC Example: MPC55xx Family

The MPC55xx family of 32-bit automotive microcontrollers is powered by e200 cores built on Power Architecture technology and provides high-performance processing and connectivity solutions for a wide range of automotive and industrial control applications. Offering pin compatibility throughout the entire flashed-based family, engineers are given the ability to migrate their efforts from one design to another, reducing development costs and improving time to market. MPC55xx family members include:

- MPC5567 (e200z6 core) with extensive connectivity options for next-generation automotive applications, such as advanced chassis
- MPC5566 (e200z6 core) for powertrain control, offering up to 3 MB flash memory
- MPC5561 (e200z6 core) for advanced safety applications
- MPC5510 (e200z1 core plus optional e200z0 core) for cost-sensitive body applications

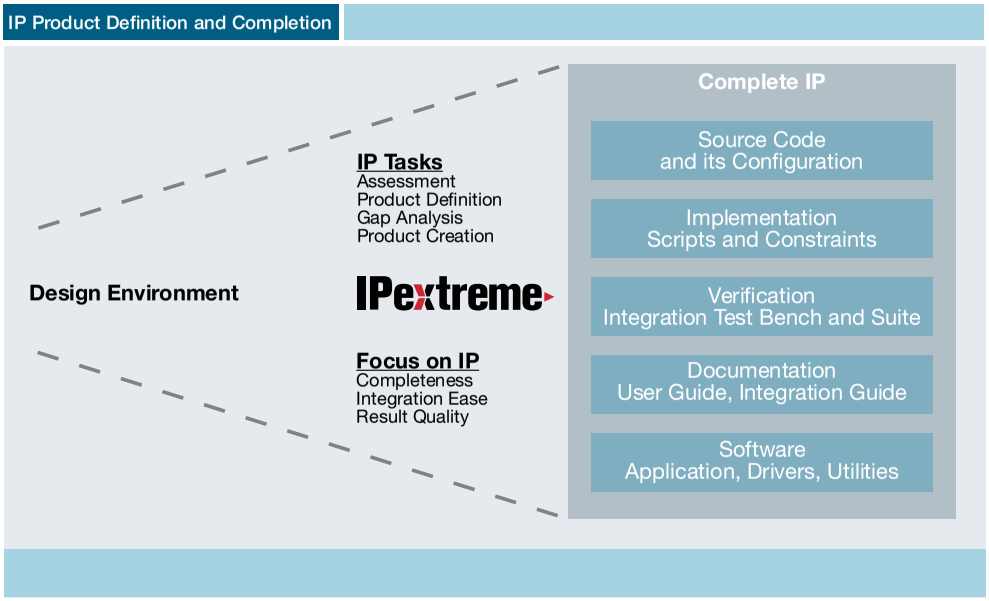
To date, Freescale has shipped more than one million e200 core-based MPC55xx family microcontrollers with zero-defect quality.

MPC55XX Family Road Map



The MPC5567 combines the high performance characteristics of the e200z6 core architecture with high-level module functions, including FlexRay™ technology, 10/100 Ethernet and enhanced Time Processor Unit (eTPU). The MPC5567 is particularly well suited for next-generation automotive applications because the FlexRay network will play a significant role in advanced chassis applications, such as stability control and brake-by-wire and steer-by-wire systems.

By making Power Architecture core technology available through IPextreme, Freescale is opening up the opportunities for chip designers to leverage this world-class architecture in a wide assortment of embedded solutions that are also compatible with Power Architecture standard products available in the marketplace today.



IPextreme markets sell and support the synthesizable e200 cores with complete IP to embedded designers who intend to integrate the cores into SoC or ASSP products targeting the automotive, consumer, industrial and networking markets.

6 Conclusion

Power Architecture technology prevails in a wide array of embedded, automotive and enterprise markets and continues to grow in the competitive marketplace because it is a single architecture that scales from very low to very high performance. It supports converging technologies, enables collaboration across industries and opens the doors to new innovations. The Power ISA is managed openly by the Power Architecture Advisory Council (PAAC) within Power.org, building new levels of extensibility and compatibility throughout the microprocessor and microcontroller development community.

Freescale takes full advantage of the scalable Power ISA to create feature-rich e200 core products for a large and growing Power Architecture customer base. Collaborating with IPextreme to license the e200 core IP ensures that more designers have access to the products and knowledge that will further expand the reach of Power Architecture technology.

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