Integrated Communications Processors

Modular AdvancedMC™ Platform
for Broadband/LTE Base Stations

freescale semiconductor

A New Generation of Long Term Evolution (LTE) Base Stations

3G Long Term Evolution (3G LTE) is a new standard under development by the 3rd Generation Partnership Project (3GPP at www.3gpp.org) to deliver next-generation broadband wireless technology for wide area networks. LTE targets higher throughput, lower latency and efficient IP backhaul compared to previous 3GPP generations, to offer a new mass deployable mobile network technology which should herald a new age of rich multimedia and real-time services.

Platform Benefits

- "Jump starts" time to market with the new LTE standard platform
- Accelerates prototyping and development time
- Helps to lower cost of ownership
- Offers portable C-based software baseline for low latency, high throughput systems

OEM Availability

The Rapid System Development reference platform, including both hardware and software, is specifically targeted for use by OEM customers developing base station equipment solutions. The individual AMC platform hardware components are widely available from a combination of Freescale and Freescale Alliance Partners, and the software is available under license to OEMs.

Turning Vision into Reality with Freescale's Rapid System Development Platform

While the LTE standards solidify in late 2007, Freescale has developed a comprehensive hardware and software reference package which enables OEMs to quickly plug together their own systems for evaluation and development.

The Rapid System Development Platform delivers a modular, programmable base station reference platform based on:

- Industry-leading processors, including networking communication processors built on Power Architecture™ technology and DSPs based on StarCore® technology
- PCI Industrial Computers Manufacturing Group (PICMG®) standard AdvancedMC™ (AMC)
- Layer 1 and 2 baseband enablement software for evolved Node B developments on Freescale processors

Rapid System Development Platform Ingredients

Function	Component	Content/Deliverables
Platform base	MicroTCA™ chassis Part #11850-013 (Schroff®)	• Industry-standard MicroTCA development chassis • Available direct from Schroff
Baseband Layer 2 processor board	MPC8548 AMC™ (PowerQUICC® processor-based AMC) Part #CWH-PPC-8548N-VE (Freescale)	• Board with user documentation • Linux® board support package (BSP) • Optional schematics, Orcad originals, Gerber files, layout files
Baseband Layer 1 processor board	MSC8144 StarCore® DSP AMC Part #MPC8144EAMC (Freescale)	• Board with user documentation • SmartDSP-OS board support package • Optional schematics, Orcad originals, Gerber files, layout files
Layer 2 software package (under OEM license)	L2 Software	• Object library, source code, GCC build environment • Test harness • Documentation
Layer 1 software package (under OEM license)	L1 Software	• Object library, source code, CodeWarrior® build environment • Test harness • MATLAB® models • Documentation

AMC Hardware Platform Details

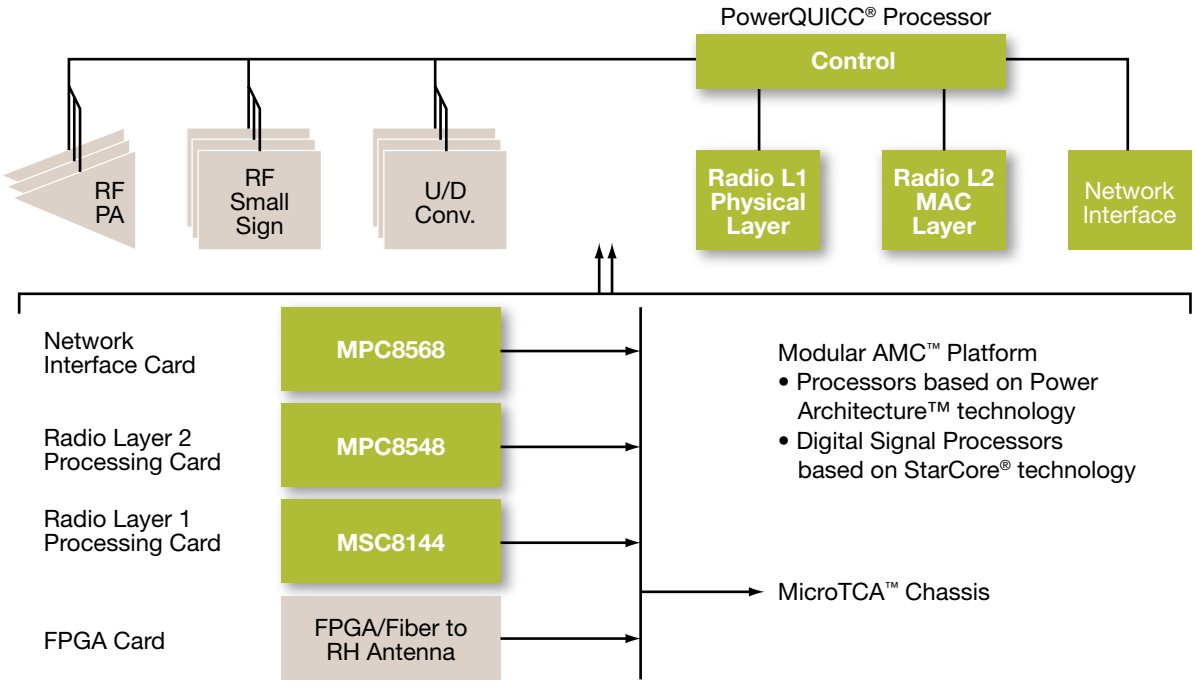
The broadband wireless baseband processing reference hardware is based on multiple modular PICMG-defined AMC modules plugged into a compact MicroTCA™ chassis. The ability to use AMC modules directly, without the need for an AdvancedTCA® or a custom carrier, enables substantial reductions in size, cost and power. The modular approach also enables individual components of the system to be upgraded, or even cost reduced, as newer hardware becomes available over time. This accelerates developer timelines and streamlines support.

The baseline platform focuses on the Baseband Layer 1 and Layer 2 processing, but the same system can be extended by adding control, network interface and FPGA cards to provide an LTE "Base Station-in-a-Box" solution. The baseline hardware platform components available are shown to the right.

Baseline Hardware Platform Components

Function	Category	Specifications/Features
Platform base	MicroTCA™ Chassis	• Schroff® MicroTCA development chassis • Part # 11850-013 (Schroff)
Baseband Layer 2 processor card	MPC8548 AMC™	• Processor: MPC8548 up to 1.3 GHz with integrated Serial RapidIO® and Gigabit Ethernet (GbE) • Operation: Stand alone or AMC plug in card • Memory: DDR2 SODIMM ,16 MB ROM • Fabric: Gigabit Ethernet (3 x SerDes) • AMC Connectivity: B+ connector , 2 x MDI for GbE, x1/x4 Serial RapidIO • IPMC: Board power up, temperature monitoring, E-keying, and status LEDs • Form factor: AMC single width, full height: 180.6 mm x 73.5 mm • Part #CWH-PPC-8548N-VE (Freescale), RoHS version
Baseband Layer 1 PHY processor card	MSC8144 AMC	• Processor: 4 x MSC8144 StarCore® DSPs up to 1.0 GHz with integrated Serial RapidIO and GbE • Operation: Stand alone or AMC plug in card • Memory: 256 MB of 32-bit wide DDR2 per MSC8144 • Connectivity: ○ 2 x Serial RapidIO (x4) interfaces from backplane routed to DSP farm via Serial RapidIO switch ○ 2 x 1000BaseX Gigabit Ethernet from backplane ports via Ethernet switch ○ 1 x Gigabit Ethernet on front plane expansion connector via Ethernet switch ○ E1/T1 TDM connection via 8 Tx/Rx on AMC connector • Boot: Stand alone (via onboard I^2C), or via back plane (e.g. Serial RapidIO, Ethernet) • Form factor: AMC single width, full height: 180.6 mm x 73.5 mm • Part # MPC8144EAMC (Freescale)

Modular AdvancedMC™ Mezzanine Hardware Platform Diagram



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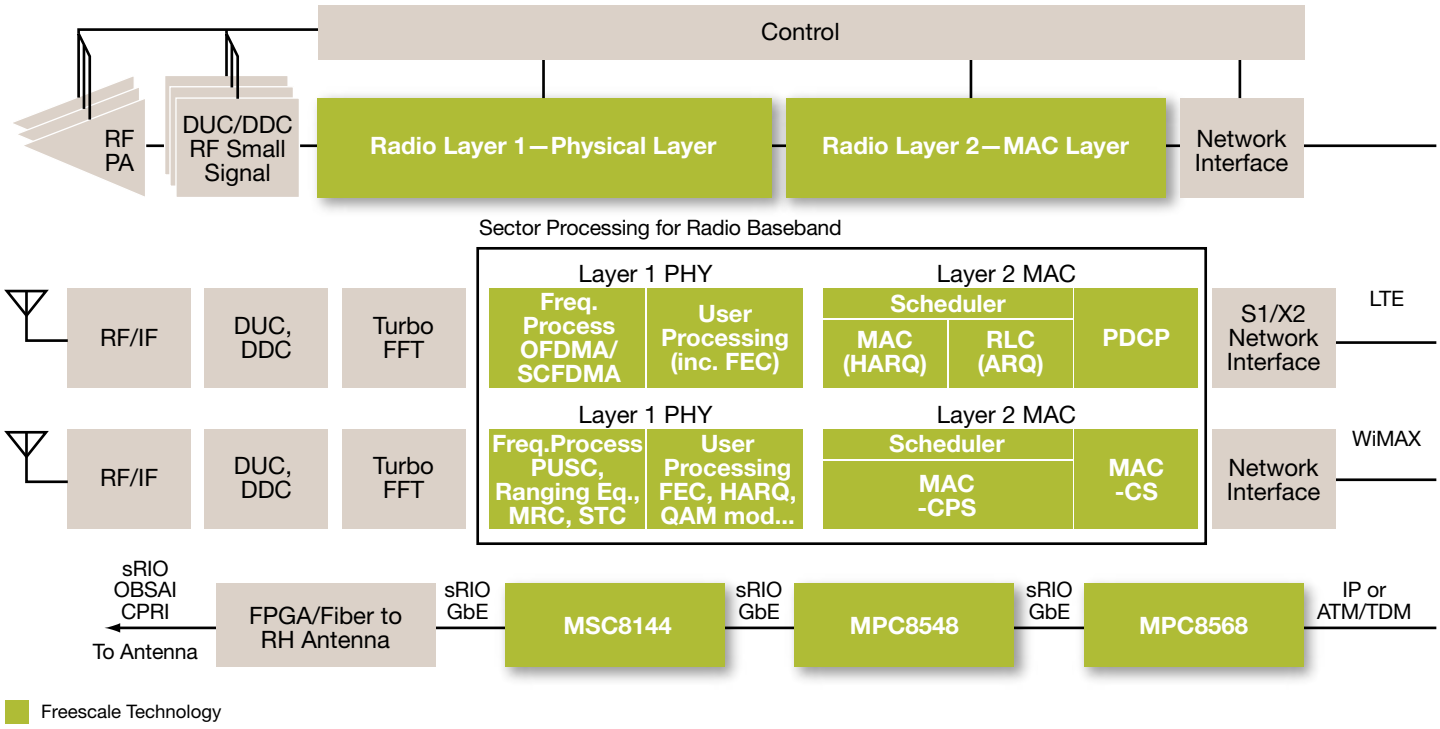
System Architecture Partitioning Diagram



System Architecture Partitioning

The base station system architecture is cleanly partitioned between separate network, Radio Layer 2 and Radio Layer 1 processors as shown above. It should be noted that for lower scale solutions—like micro-base stations—it is certainly practical to consolidate these functions into fewer components, but the baseline reference addresses the scaling needed for multi-sector macro-base station solutions, where each sector delivers high throughput and optimum range.

Major Architectural Block Responsibilities

Layer 1—Physical

Performs the Physical Layer Radio channel coding, modulation onto the carrier frequency, synchronization and MIMO multiple antenna techniques ready to carry the logical radio transport channels and higher layers over the air interface.

Layer 2—Medium Access Control

Performs the Radio Link Control Layer, including the Medium Access Control (MAC), that controls the base station and subscriber access to air interface resources. Resources are scheduled according to Quality of Service (QoS) requirements, using packet concatenation/segmentation, retransmission via automatic repeat request (ARQ) and also hybrid automatic repeat request (HARQ) in combination with Layer 1.

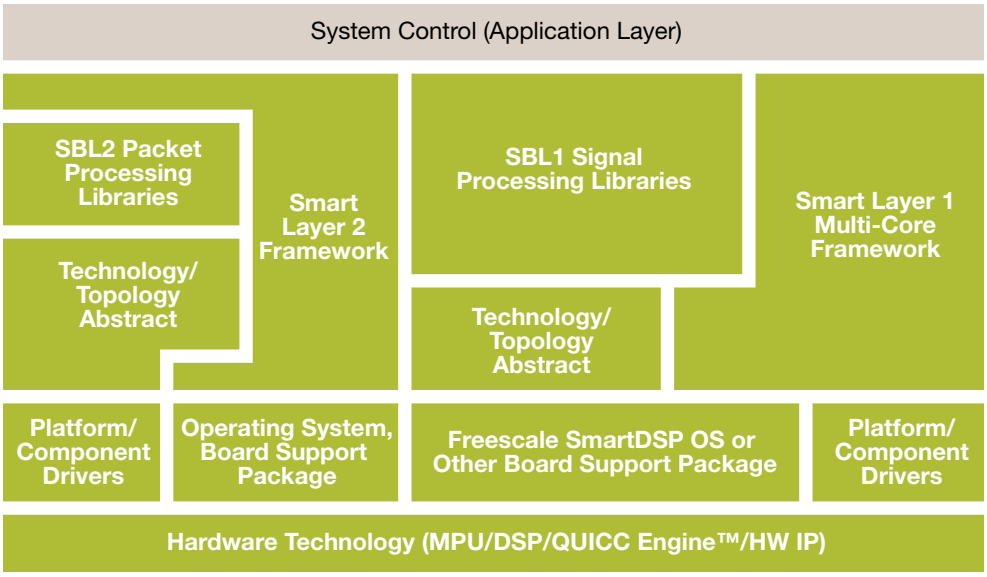
Network Interface

Performs network backhaul transport and interworking with internal interfaces. This includes processing the network layers up to OSI Layer 3, including IPsec secure network termination, header compression and traffic classification (QoS). The Network Interface Card (NIC) can optionally support the 3G LTE radio link encryption—but depending upon the selected architecture this could be partitioned to the channel card.

Layer 1 and Layer 2 Radio Software Architecture

The Layer 1 and 2 real-time software subsystems combine together to offer several key baseband ingredients for an air interface conduit to mobile subscribers. The Layer 1 and 2 real-time software subsystems operate in concert, through a commonly defined architecture and L2/L1 interface. This interface not only ensures efficient inter-operation of the two, but also enables advanced features and scheduling algorithms between them. The effort invested into the system definition and interface should translate into time to market savings for the developer, and can be considered as a baseline Layer 1/Layer 2 solution for OEMs to add differentiating intellectual property.

LTE System Architecture Layer 1 and Layer 2



Layer 2—Data Plane Module Software

Freescale provides a set of OS independent modules covering the Layer 2 processing that is executed in real time. All software is delivered as a set of modules for RLC, MAC layer and scheduler that can be ported to any RTOS. Designed for maximum real-time throughput, several optimized hardware-specific software drivers can be included for optimum performance. All software is developed in ANSI-C, and fully documented, flexible and extensible in design, with an emphasis on the scheduler architecture. As a design aid, the software can be delivered as an application running under User Mode Linux®. Further details are listed to the right.

Dataplane Module Software Features

Category	Specifications/Features
Design approach	• Modular and portable C software modules for RLC, MAC, PDCP, scheduler • Sample single thread L2 data-plane processing chain • Runs under any RTOS environment, and independent of the RTOS and associated drivers performance. Achieved by using: ○ Custom memory/buffer management, timer management and drivers for performance-critical hardware/coprocessor offload such as security and DMA ○ Minimum number of software threads for data plane operation ○ No OS specific calls in any of the data plane modules ○ Abstraction/rerouting of trace/debug information • Control plane/RRC Layer (not included) interaction possible through APIs to configure appropriate data-plane operation • Designed with the latest available drafts of specifications
RTOS support	• RTOS agnostic implementation • Example includes software ported to Linux® User Mode
API	• Full software abstraction between data plane/control plane and data plane/scheduler through well-defined and documented APIs • SBL2 API interface on L2 functional level
Validation/Test	• Software tested on ○ Unit level (individual modules) ○ Integration level (module interaction) ○ System level (system operation, performance) • Software test environment is part of the software delivery package
1. Medium Access Control (MAC) Layer	• Compatible to standard: 3GPP 36.321 (MAC) • Includes downlink/uplink scheduler
2. Radio Link Control (RLC) Layer	• Compatible to standard: 3GPP 36.322 (RLC)
3. Packet Data Convergence Protocol (PDCP) Layer	• Compatible to standard: 3GPP 36.323 (PDCP) • Includes optimized encryption drivers/hardware offload • Excludes Robust Header Compression (ROHC) and IPsec protocols (third parties)
4. L2/L1 interface	• Implements an efficient L2/L1 interface designed for seamless integration with Freescale L1 solution
5. Framework	• Example integrated processing chain running under Linux: ○ Demonstrates integration of L2 modules ○ Provides known development/test environment

Layer 1—Real-Time Software Subsystem

The LTE Layer 1 software includes physical baseband channel processing and radio transport channel functions as defined in the 3GPP standards. Freescale provides a comprehensive set of kernel modules covering the Layer 1 processing for physical downlink shared channel and physical uplink shared channels. The kernels are further combined into uplink and downlink chains, which run real time using the SmartDSP real-time operating system as a reference. All software is developed as ANSI-C callable and fully documented.

In brief, the physical layer processing functions include:

- Modulation
- Channel coding
- Transmission schemes
- Multiplexing
- MIMO/diversity
- Channel estimation
- Equalization (outside 3GPP scope)

Further details are listed to the right.

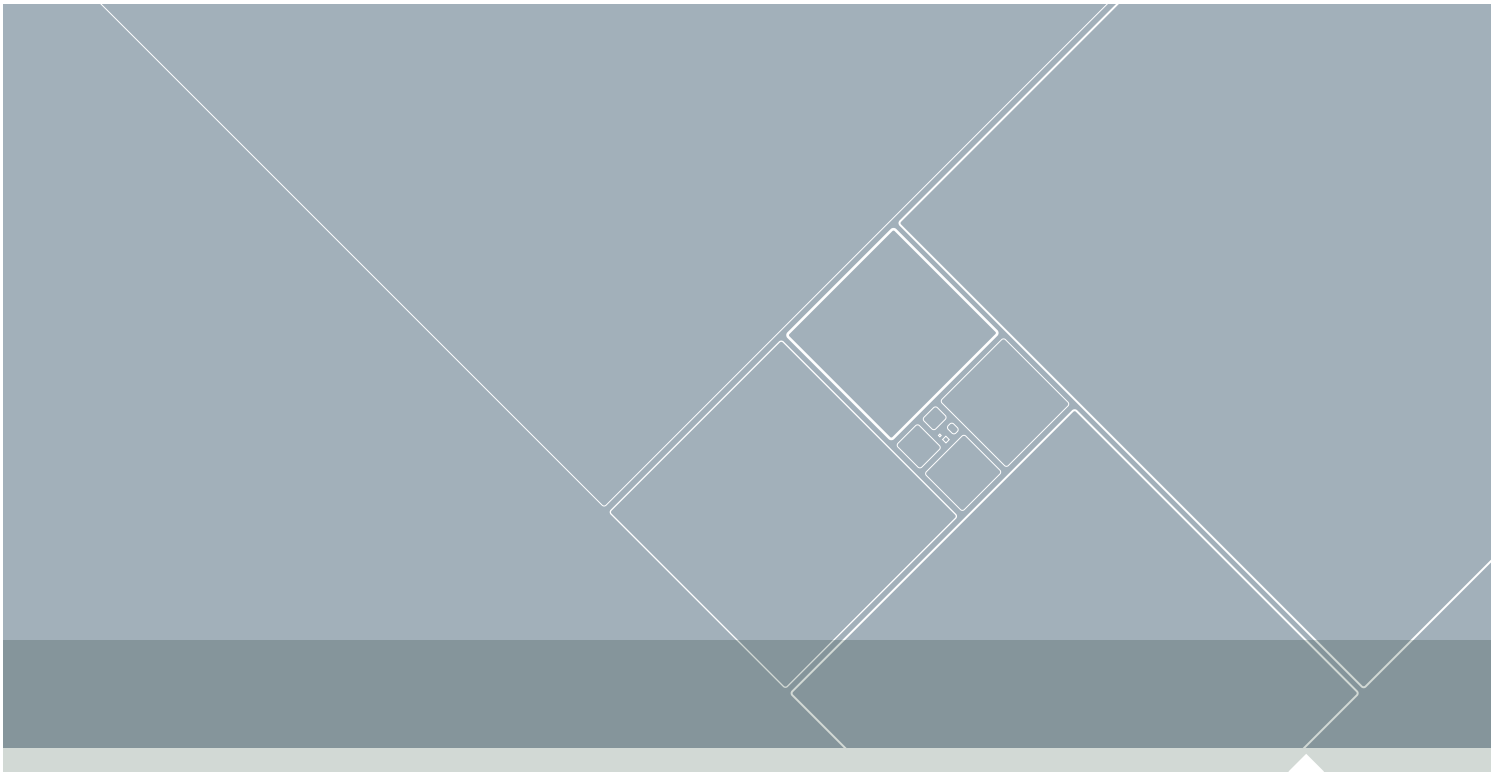
Real-time Software Subsystem Features

Category	Specifications/Features
Design approach	• Layered API software approach enables multi-level reuse eases integration with custom and IP • Modular C software modules for all subsystems—includes C wrapper for optimized real-time assembly modules • Algorithm verification with floating and fixed point simulation system • Multi-core framework allows for efficient inter-core communication and task partitioning
Features	• Designed with latest available drafts of specifications • Focus on high-speed shared user physical channels ○ Physical Downlink Shared Channel (PDSCH) (36.211 chapter 5.3) ○ Physical Uplink Shared Channel (PUSCH) (36.211 chapter 6.3) • Modular design with well defined interfaces and module interactions ○ e.g. Downlink ·· IF1Tx: L1/L2 logical interface—memory mapped over Serial RapidIO® ·· IF2Tx: Transport to physical channel interface per 3GPP 36.211 and 36.212 ·· IF3Tx: Transport to OFDMA processing interface—remaps IFFT signal generation onto FPGA ·· IF4Tx: Baseband I/Q sample interface towards the antenna FPGA ○ Message based configuration and runtime control ○ Includes MIMO processing
RTOS support	• SmartDSP OS: Integrates real-time kernels and drivers
API	• Full software abstraction through well-defined and documented APIs ○ SBL1 API structure for reuse on function level ○ Framework API for reuse of higher level, complete processing chains ○ Complete subsystem reuse possible for channel types
Validation/Test	• Software tested on ○ Unit level (individual modules) ○ Integration level (module interaction) ○ System level (system operation, performance) • Software test environment is part of the software delivery package
Standards reference	[1] 3GPP TS 36.201: LTE physical layer general description (v1.0.0) [2] 3GPP TS 36.211: Physical channels and modulation (v1.0.0) [3] 3GPP TS 36.212: Multiplexing and channel coding (v1.3.2) [4] 3GPP TS 36.213: Physical layer procedures (v1.0.0) [5] 3GPP TS 36.214: Physical layer measurements (v0.1.0) [6] 3GPP TS 36.300: E-UTRA and E-UTRAN overall description; Stage 2 (v8.0.0) [7] 3GPP TS 25.212: UTRA; multiplexing and channel coding
Layer 1 software packages	• Signal Processing Library: contains LTE Layer 1 signal processing manager and kernel library functions. The signal processing kernels are the basic processing units and the signal processing manager is the chain integration of a set of kernels which includes: ○ DL Transport Channel Package ○ DL Physical Channel Package ○ UL Transport Channel Package ○ UL Physical Channel Package • MATLAB® Model Package DL Physical Channel Chain ○ Delivers complete uplink BER performance benchmarking ○ Enables test vector generation • Functional integration of uplink/downlink chains (PDSCH/PUSCH) on multi-core MSC8144 ○ Uses SmartDSP OS real-time operation ○ L1/L2 interface package contains the application-level functionality (not driver level) descriptor, parser and state machine for protocol handling for the L1/L2 interface

Layer 1/Layer 2—Integrated System Solution

A prime advantage of the Freescale modular platform is that the Layer 1 and Layer 2 software is seamlessly integrated and tested operating in tandem on the PowerQUICC® and StarCore DSP processors. The physical interface of choice between them is a low latency Serial RapidIO® link, but this could be modified to map to other high-speed serial interconnects like PCI Express® and/or Gigabit Ethernet.

Integrated System Solutions Features	
Category	**Specifications/Features**
Design approach	• Layer 1 and Layer 2 coded with the same development process and coding standards • Coordinated design requirements management and feature set • Common L1/L2 test case definition
Validation/test	• Integrated subsystems, tested together in common real-time environment • Automated software test environment as part of the software delivery package
Features	• Well defined L2/L1 Interface over Serial RapidIO® • Layered architecture • Easy L2/L1 out-of-the-box experience through validated test cases



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Document Number: LTEWIMAXFS
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