Modular AdvancedMC™ Platform for Broadband/LTE Base Stations
A New Generation of Long Term Evolution (LTE) Base Stations

3G Long Term Evolution (3G LTE) is an advanced standard from the 3rd Generation Partnership Project (3GPP at www.3gpp.org) to deliver next-generation broadband wireless technology for wide area networks. LTE targets higher throughput, lower latency and efficient IP backhaul compared to previous 3GPP generations, to offer a new mass deployable mobile network technology heralding a new age of rich multimedia and real-time services.

Platform Benefits

- “Jump starts” time to market with the new LTE standard platform
- Accelerates prototyping and development time
- Helps to lower cost of ownership
- Offers portable C-based software baseline for low latency, high throughput systems
- Scalable code and silicon offerings building solutions from Femto to Macro

OEM Availability

The Rapid System Development reference platform, including both hardware and software, is specifically targeted for use by OEM customers developing base station equipment solutions. The individual AMC platform hardware components are widely available from a combination of Freescale and Freescale Alliance Partners, and the software is available under license to OEMs.

Turning Vision into Reality with Freescale’s Rapid System Development Platform

In order to accelerate time to market for OEMs, Freescale has developed a comprehensive hardware and software reference package enabling systems to be quickly plugged together for evaluation and development.

The Rapid System Development Platform delivers a modular, programmable base station reference platform based on:

- Industry-leading processors, including networking communication processors built on Power Architecture® technology and DSPs based on StarCore technology
- PCI Industrial Computers Manufacturing Group (PICMG®) standard AdvancedMC™ (AMC)
- Layer 1 and 2 baseband enablement software for evolved Node B developments on Freescale processors

### Rapid System Development Platform Ingredients

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<tr>
<th>Function</th>
<th>Component</th>
<th>Content/Deliverables</th>
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<tr>
<td>Platform base</td>
<td>MicroTCA™ chassis Part #11850-013 (Schroff®)</td>
<td>Industry-standard MicroTCA development chassis Available direct from Schroff</td>
</tr>
<tr>
<td>Baseband Layer 2 processor board</td>
<td>P2020 AMC™ (QorIQ™ processor-based AMC)</td>
<td>Board with user documentation Linux® board support package (BSP)</td>
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<tr>
<td>Baseband Layer 1 processor board</td>
<td>MSC8156 StarCore® DSP AMC</td>
<td>Board with user documentation SmartDSP-OS board support package</td>
</tr>
<tr>
<td>Layer 2 software package (under OEM license)</td>
<td>L2 Software</td>
<td>Object library, source code, GCC build environment Test harness Documentation</td>
</tr>
<tr>
<td>Layer 1 software package (under OEM license)</td>
<td>L1 Software</td>
<td>Object library, source code, CodeWarrior build environment Test harness MATLAB® models Documentation</td>
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AMC Hardware Platform Details

The broadband wireless baseband processing reference hardware is based on multiple AMC modules defined by the PICMG standard plugged into a compact MicroTCA™ chassis. The ability to use AMC modules directly, without the need for an AdvancedTCA® or a custom carrier, enables substantial reductions in size, cost and power. The modular approach also enables individual components of the system to be upgraded or even cost reduced, as newer hardware becomes available over time. This accelerates developer timelines and streamlines support.

The baseline platform focuses on the Baseband Layer 1 and Layer 2 processing, but the same system can be extended by adding control, network interface and FPGA cards to provide an LTE “Base Station-in-a-Box” solution. The baseline hardware platform components available are shown to the right.

Baseline Hardware Platform Components

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<tr>
<th>Function</th>
<th>Category</th>
<th>Specifications/Features</th>
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<tr>
<td>Platform base</td>
<td>MicroTCA™ Chassis</td>
<td>Schroff® MicroTCA development chassis</td>
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</table>
| Baseband Layer 2 processor card | P2020 AMC™ | Processor: P2020 dual-core processor up to 1.2 GHz/core with integrated Serial RapidIO® interconnect and Gigabit Ethernet (GbE)  
Operation: Stand alone or AMC plug in card  
Memory: DDR2 SODIMM, 64 MB flash  
sRIO or PCI Express® technology and dual 1000Base-X backplane interfaces  
1000Base-T, USB and UART front panel interfaces  
IPMC: Board power up, temperature monitoring, E-keying, and status LEDs  
Form factor: AMC single width, full height: 180.6 mm x 73.5 mm |
| Baseband Layer 1 PHY processor card | MSC8156 AMC | Processor: Up to 3x MSC8156 six core StarCore® DSPs up to 1.0 GHz with integrated Serial RapidIO and GbE  
Operation: Stand alone or AMC plug in card  
Memory: 2 x 512 MB of 64-bit wide DDR3 per MSC8156  
Four sRIO and two 1000Base-X backplane interfaces  
1000Base-T, USB and UART front panel interfaces  
IPMC: Board power up, temperature monitoring, E-keying and status LEDs  
Form factor: AMC single width, full height: 180.6 mm x 73.5 mm |

Modular AdvancedMC™ Mezzanine Hardware Platform Diagram

- PowerQUICC® Processor
- Control
- Radio L1 Physical Layer
- Radio L2 MAC Layer
- Network Interface

- Network Interface Card
- Radio Layer 2 Processing Card
- Radio Layer 1 Processing Card
- FPGA Card

- MPC8569/P2020
- P2020
- MSC8156
- FPGA/Fiber to RH Antenna

- Freescale Technology

- Modular AMC Platform
  - Processors based on Power Architecture® technology
  - Digital Signal Processors based on StarCore® technology

- MicroTCA™ Chassis
System Architecture Partitioning

The base station system architecture is cleanly partitioned between separate network, Radio Layer 2 and Radio Layer 1 processors as shown above. It should be noted that for lower scale solutions—like micro-base stations—it is certainly practical to consolidate these functions into fewer components, but the baseline reference addresses the scaling needed for multi-sector macro-base station solutions, where each sector delivers high throughput and optimum range.

Network Interface
Performs network backhaul transport and interworking with internal interfaces. This includes processing the network layers up to OSI Layer 3, including IPsec secure network termination, header compression and traffic classification (QoS). The network interface card (NIC) can optionally support the 3G LTE radio link encryption—but depending upon the selected architecture this could be partitioned to the channel card. The processing required for the network interface is ideally suited to devices such as the MPC8569 PowerQUICC III processor, the QorIQ P2020 or QorIQ P4080, depending on the system profile and performance required.

Freescale’s VortiQa Software Solutions
Freescale’s VortiQa software is designed to help you simplify your product development cycles and boost application performance. VortiQa software delivers integrated security and networking functionality to address specific vertical markets such as wireless infrastructure equipment, and enables threat protection, secure access, high availability, convergence and management in your system.
Layer 1 and Layer 2 Radio Software Architecture

The Layer 1 and 2 real-time software subsystems combine to offer several key baseband ingredients for an air interface conduit to mobile subscribers. The Layer 1 and 2 real-time software subsystems operate in concert, through a commonly defined architecture. This enables advanced features and scheduling algorithms between them. The effort invested into the system definition and interface should translate into time to market savings for the developer, and can be considered as a baseline Layer 1/Layer 2 solution for OEMs to add differentiating intellectual property.

Layer 2—Data Plane Module Software

Freescale provides a set of OS independent modules covering the Layer 2 processing that is executed in real time. All software is delivered as a set of modules for RLC, MAC layer and scheduler that can be ported to any RTOS. Designed for maximum real-time throughput, several optimized hardware-specific software drivers can be included for optimum performance. All software is developed in ANSI-C, and fully documented, flexible and extensible in design, with an emphasis on the scheduler architecture. As a design aid, the software can be delivered as an application running under User Mode Linux®. Further details are listed to the right.
Layer 1—Real-Time Software Subsystem

The LTE Layer 1 software includes physical baseband channel processing and radio transport channel functions as defined in the 3GPP standards. Freescale provides a comprehensive set of kernel modules covering the Layer 1 processing for physical downlink shared channel and physical uplink shared channels. The kernels are further combined into uplink and downlink chains, which run real time using the SmartDSP real-time operating system as a reference. All software is developed as ANSI-C callable and fully documented.

In brief, the physical layer processing functions include:
- Modulation
- Channel coding
- Transmission schemes
- Multiplexing
- MIMO/diversity
- Channel estimation
- Equalization (outside 3GPP scope)

Further details are listed to the right.

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### Real-Time Software Subsystem Features

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| **Design approach**       | - Layered API software approach enables multi-level reuse eases integration with custom and IP  
                            - Modular C software modules for all subsystems—includes C wrapper for optimized real-time assembly modules  
                            - Algorithm verification with floating and fixed point simulation system  
                            - Multicore framework allows for efficient inter-core communication and task partitioning  |
| **Features**              | - Focus on high-speed shared user physical channels                                       
                            - Physical Downlink Shared Channel (PDSCH) (36.211 chapter 5.3)  
                            - Physical Uplink Shared Channel (PUSCH) (36.211 chapter 6.3)  
                            - Random Access Channel (RACH)  
                            - Modular design with well defined interfaces and module interactions  
                            - e.g. Downlink  
                                - IF1Tx: L1/L2 logical interface—memory mapped over Serial RapidIO®  
                                - IF2Tx: Transport to physical channel interface per 3GPP 36.211 and 36.212  
                                - IF3Tx: Transport to OFDMA processing interface—remaps IFFT signal generation onto FPGA  
                                - IF4Tx: Baseband I/Q sample interface towards the antenna FPGA  
                            - Message based configuration and runtime control  
                            - Includes MIMO processing  |
| **RTOS support**          | - SmartDSP OS: Integrates real-time kernels and drivers                                   |
| **API**                   | - Full software abstraction through well-defined and documented APIs  
                            - SBL1 API structure for reuse on function level  
                            - Framework API for reuse of higher level, complete processing chains  
                            - Complete subsystem reuse possible for channel types  |
| **Validation/test**       | - Software tested on  
                            - Unit level (individual modules)  
                            - Integration level (module interaction)  
                            - System level (system operation, performance)  
                            - Software test environment is part of the software delivery package  |
| **Standards reference**   | [1] 3GPP TS 36.201: LTE physical layer general description (v1.0.0)  
                            [2] 3GPP TS 36.211: Physical channels and modulation (v1.0.0)  
                            [3] 3GPP TS 36.212: Multiplexing and channel coding (v1.3.2)  
                            [4] 3GPP TS 36.213: Physical layer procedures (v1.0.0)  
                            [5] 3GPP TS 36.214: Physical layer measurements (v0.1.0)  
                            [6] 3GPP TS 36.300: E-UTRA and E-UTRAN overall description; Stage 2 (v8.0.0)  
                            [7] 3GPP TS 25.212: UTRA; multiplexing and channel coding  |
| **Layer 1 software packages** | - Signal Processing Library: contains LTE Layer 1 signal processing manager and kernel library functions. The signal processing kernels are the basic processing units and the signal processing manager is the chain integration of a set of kernels which includes:  
                            - DL Transport Channel Package  
                            - DL Physical Channel Package  
                            - UL Transport Channel Package  
                            - UL Physical Channel Package  
                            - MATLAB® Model Package  
                                - Compiled Matlab reference chains for test vector generation  
                            - Functional integration of uplink/downlink chains (PDSCH/PUSCH) on multicore MSC8156  
                            - Uses SmartDSP OS real-time operation  |

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- Freescale provides a comprehensive set of kernel modules covering the Layer 1 processing for physical downlink shared channel and physical uplink shared channels.
- All software is developed as ANSI-C callable and fully documented.
- In brief, the physical layer processing functions include:
  - Modulation
  - Channel coding
  - Transmission schemes
  - Multiplexing
  - MIMO/diversity
  - Channel estimation
  - Equalization (outside 3GPP scope)
- Further details are listed to the right.
- Freescale's LTE Layer 1 software includes physical baseband channel processing and radio transport channel functions as defined in the 3GPP standards.
- The kernels are further combined into uplink and downlink chains, which run real-time using the SmartDSP real-time operating system as a reference.
- All software is developed as ANSI-C callable and fully documented.

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Layer 1/Layer 2—Integrated System Solution

A prime advantage of the Freescale modular platform is that both the Layer 1 and Layer 2 software components are integrated, along with a range of physical interface options, including low latency links such as Serial RapidIO® interconnect, PCI Express® technology and/or Gigabit Ethernet.

### Integrated System Solutions Features

<table>
<thead>
<tr>
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<th>Specifications/Features</th>
</tr>
</thead>
</table>
| **Design approach**    | • Layer 1 and Layer 2 coded with the same development process and coding standards  
                         • Coordinated design requirements management and feature set |
| **Validation/test**    | • Integrated subsystems, tested together in common real-time environment  
                         • Automated software test environment as part of the software delivery package |
| **Features**           | • Layered architecture  
                         • Easy L2/L1 out-of-the-box experience through validated test cases |