

MCIMX27 Multimedia Applications Processor

Silicon Revision: 2.0 and 2.1

Table 1 defines Severity values for errata described in this document.

Table 1. Definitions of Errata Severity

Severity	Errata Type	Meaning	Workaround
1	Critical	Failure mode that severely inhibits the use of the device for all or a majority of intended applications	Unavailable
2	High	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications	Generally available
3	Moderate	Unexpected behavior that does not cause significant problems for the intended applications of the device	Generally available

Table 2 provides the silicon revision and equivalent mask set and product number contained within this errata document.

Table 2. Silicon Revision to Mask Set Correlation

Silicon Revision	Mask Set	Product Number
2.0	0M72J	MCIMX27
2.1	M72J	MCIMX27

Table 3 provides the known chip errata affecting silicon version 2.0 and 2.1 of the MCIMX27 Multimedia Applications Processor.



Table 3. Chip Errata for MCIMX27

Number	Severity	Erratum ID	Summary	Details
1.	3	bo57692	<p>Module Affected: Video Codec</p> <p>Title: Video Codec module supporting MV and MVD ranges does not conform with standard.</p>	<p>Description: Video Codec module supporting MV and MVD ranges does not conform with the H.264 standard.</p> <p>1. The standard specifies the range of MVD to be –4096–4095.75. However, the Video Codec module only supports up to –2048–2047.75.</p> <p>2. The standard specifies that the range of horizontal MV to be –2048–2047.75. However, the Video Codec module only supports up to –1024–1023.75. Because the maximum image resolution in the MCIMX27 device is 720x576, it is not likely to receive a bitstream with MV/MVD in such a large range in real codec applications; therefore, there is no real impact to applications.</p> <p>Workaround: No workaround.</p> <p>Fix Plan/Status: No fix planned.</p>
2.	3	bo58229	<p>Module Affected: USB</p> <p>Title: A remote wakeup can be interpreted as a disconnect.</p>	<p>Description: In Host mode in the ULPI core, a remote wakeup can be interpreted as a disconnect. This issue involves the latency when asserting in synchronous mode. In some instances, the host will not properly latch the K state. When this occurs, the core wakes up to a J state. Eventually the host will not resume, and will show an SE0 and assume a disconnect occurred.</p> <p>Workaround: No workaround.</p> <p>Fix Plan/Status: No fix planned.</p>
3.	3	bo57815	<p>Module Affected: WEIM</p> <p>Title: A burst write access will miss the first word when the burst write follows another burst operation.</p>	<p>Description: When a burst access to WEIM external memory is immediately followed by another burst access, the first word may be missed at write burst access because the eb_b signal comes too late. Reason: The ecb_hburst_ecb_fw signal, in the WEIM Bus Controller module has an extra high pulse and only one high pulse is required.</p> <p>Workaround: Set EDC field to two breaks which continues the burst access to external memory.</p> <p>Fix Plan/Status: No fix planned.</p>

Table 3. Chip Errata for MCIMX27 (continued)

Number	Severity	Erratum ID	Summary	Details
4.	2	bo93263	<p>Module Affected: Video Codec</p> <p>Title: Lockup of Video Codec in MPEG-4 encode or decode</p> <p>Note: Applies only to silicon revision 2.0</p>	<p>Description: During encoding or decoding MPEG-4, the Video Codec module can lock up. In the combined AXI to AHB and 32to64 gasket there is a FIFO for read data. This is to buffer data that is coming from the 64-bit bus faster than the 32-bit bus can accept it. There is no logic to send a request to memory only when the FIFO has room for return data. In a case with ideal data throughput, this FIFO overruns and read data is corrupted. This ideal data throughput only happens during MPEG-4 encoding and decoding.</p> <p>Workaround: There are two workarounds:</p> <ol style="list-style-type: none"> 1. Set the Latency Hiding Disable (LHD) bit in the ESDCTL DDR Controller ESDMISC register. This adds latency between DDR transactions, removing the ideal data throughput. This should only be done during MPEG-4 encoding and decoding. Note that this reduces performance. During MPEG-4 encoding/decoding, this degradation is acceptable. LHD should not be set during H.264 or H.263 operation. 2. Assign all buffers accessed by the video code into the same DRAM bank and ensure every buffer type has a size of integer number of pages. This ensures that there will be a page miss between accesses of different sub-masters inside the VPU, increasing the delay. The DRAM is split into four equal sizes called banks, so the bank size is 1/4 of the DRAM size. <p>Fix Plan/Status: Fixed in silicon revision 2.1.</p>
5.	3	bo93708	<p>Module Affected: JTAG Controller</p> <p>Title: Boundary scan fails because of an internal timing issue.</p> <p>Note: Applies only to silicon revision 2.0</p>	<p>Description: Timing is not properly extracted for the boundary scan circuitry so post-layout gate-level simulations did not correctly simulate the circuit. A race condition prevents proper shifting of data through the Boundary Scan circuitry</p> <p>Workaround: None</p> <p>Fix Plan/Status: Fixed in silicon revision 2.1.</p>

Table 3. Chip Errata for MCIMX27 (continued)

Number	Severity	Erratum ID	Summary	Details
6.	2	bo95933	<p>Module Affected: IIM</p> <p>Title: When the incorrect power-up or power-down sequence is used on the processor, unintentional programming of IIM fuses is possible, regardless of the set Fuse_{VDD} voltage, reconfiguring the part permanently.</p>	<p>Description: Internal fuses on the processor could be unintentionally programmed, regardless of the voltage level set for Fuse_{VDD}. Even if Fuse_{VDD} is set to 1.8 V (read-only voltage), some processors may be programmed at that voltage. This only happens when the incorrect power-up or power-down sequence is used on the processor.</p> <p>Workaround: It is recommended to power up and power down the processor following the power-up and power-down sequence documented in the <i>MCIMX27 Multimedia Applications Processor Data Sheet</i>.</p> <p>Fix Plan/Status: No fix planned.</p>
7.	2		<p>Module Affected: eMMA PP (post processor)</p> <p>Title: Resize fails when the horizontal scale is bigger than two.</p>	<p>Description: The gasket that is between the Post Processor and the EMI cannot support burst accesses when the burst length is equal or over 16 words. However, the Post Processor will do the burst access over 16 words when the Post Processor resizes with the horizontal scale over two. In this case the Post Processor's access misses the data or will be pending due to no response from the gasket.</p> <p>Workaround: Use software for horizontal resizing when the scale is bigger than two. For example: When the scale is 2.5 for both horizontal and vertical, software should be used to produce the horizontal resize with scale 2, and then the Post Processor should do the vertical 2.5 and horizontal 1.25 resize.</p> <p>Fix Plan/Status: No fix planned</p>

Revision History

Erratum 7 was added since Rev. 0.1.



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