

MCF54455 Chip Errata

Silicon Revision: All

Supports: MCF54450, MCF54451, MCF54452, MCF54453, MCF54454, and MCF54455

Summary of MCF5445x Errata

The latest mask of the MCF5445x family is 2M22H.

Table 1. Summary of MCF5445x Errata

Errata	Module Affected	Date Errata Added	Revision Affected?	
			1M22H	2M22H
SECF043	SDRAM	3/27/07	No	No
SECF041	SBF	9/13/07	Yes	No
SECF016	SRAM	9/13/07	Yes	No
SECF042	SBF	9/13/07	Yes	No
SECF034	PLL	9/13/07	Yes	No
SECF129	GPIO	10/9/08	Yes	Yes
SECF162	SBF and Reset	3/1/10	Yes	Yes
SECF180	Interrupt controller	8/12/10	Yes	Yes

Revision History

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
1		Initial revision

Rev. No.	Date	Substantive Changes
2	11/2008	Added 2M22H mask throughout. All pre-existing errata are fixed on this new mask. However, a new errata, SECF129 , was added to all masks.
3	10/2009	Changed status of SECF129 errata from 'Will be fixed.' to 'Currently, there are no plans to fix this.'
4	3/2010	Added SECF162 errata.
5	8/2010	Added SECF180 errata.

SECF043: Line Read from DDR2 SDRAM

Errata type:	Silicon
Affected component:	SDRAM controller
Description:	When the system bus requests a line read from the SDRAM in DDR2 mode, the data becomes corrupted when the burst is aligned to address 0x4 or 0xC. DDR mode is not affected.
Workaround:	There is no workaround to resolve this issue other than to ensure that bursts from DDR2 memories do not begin at address 0x4 or 0xC. If cache is enabled, burst accesses beginning at these addresses are likely, so cache should be disabled.
Fix plan:	Fixed in revision 1 of the device.

SECF041: Serial Boot with a Crystal

Errata type:	Silicon
Affected component:	SBF
Description:	Booting using the serial configuration mode (BOOTMOD[1:0] == 11) with an external crystal can prevent the on-chip oscillator from starting properly. This is due to an uninitialized internal crystal oscillator enable signal from the chip configuration logic during the time between powering the part and the availability of all serial reset configuration data. If the on-chip oscillator is configured for external reference mode instead of crystal mode during that time, the external crystal does not operate correctly because the processor is not driving current on XTAL. Therefore, the crystal fails to drive a waveform into the device on EXTAL, and no internal clocks are generated by the oscillator to the PLL and other on-chip logic.
Workaround:	Do not use serial configuration mode with an external crystal. Only parallel or default configuration modes should be attempted with a crystal, or use only an external clock source (instead of a crystal) for serial configuration mode.
Fix plan:	Fixed in masks 2M22H and later.

SECF016: SRAM Simultaneous Reads

Errata type: Silicon

Affected component: V4 SRAM controller

Description: When the SRAM is enabled for core and backdoor port accesses, certain rare, but unpredictable, sequences/overlaps between core and backdoor port accesses result in incorrect read data. The core or the backdoor port access may obtain the incorrect data.

Workaround: Do not enable core and backdoor port accesses to the SRAM at the same time. The 32-kByte SRAM is controlled by RAMBAR1 with:

- Bit 0 = V (valid) — Enable direct SRAM accesses by the core
- Bit 9 = BDE (backdoor enable) — Allow access by non-core bus masters via the SRAM backdoor on the crossbar switch

Do not set V and BDE. Use one of the following settings instead:

Table 3. Available SRAM Access Modes

V	BDE	Description
0	0	No SRAM accesses allowed
1	0	Only core accesses allowed
0	1	Only backdoor accesses allowed. Note: The core can still access the SRAM backdoor port via the crossbar switch.

Fix plan: Fixed in masks 2M22H and later.

SECF042: Serial Boot on 256-Pin Devices

Errata type: Silicon

Affected component: SBF

Description: Serial configuration mode on the 256-pin devices (MCF54450 and MCF54451) configures the device with incorrect data.

Workaround: Do not use serial configuration mode with the 256-pin devices. Only use parallel or default configuration modes.

Fix plan: Fixed in masks 2M22H and later.

SECF034: PLL Loss-of-lock at Large Voltage Differentials

Errata type: Silicon

Affected component: PLL

Description: There is a sensitivity to large differentials in IVDD and EVDD/OSCVDD in the PLL feedback path. This sensitivity can cause the PLL to lose lock and, in some cases, fail to generate output clocks.

Workaround:

There are two requirements that must be met to avoid this errata:

1. Disable the PLL's loss-of-lock feature by setting bit 4 in the PLL status register (MCF_PLL_PSR |= 0x10).
2. Ensure that the IVDD, EVDD, and OSCVDD supplies are within the following limits:

Table 4. Supply Limits

Supply	Min	Max	Unit
IVDD	1.4	1.6	V
EVDD	3.0	3.45	V
OSCVDD	3.0	3.45	V

Fix plan:

Fixed in masks 2M22H and later.

SECF129: GPIO Not Available on ATA Signals on MCF54452 and MCF54453

Errata type:

Silicon

Affected component:

GPIO

Description:

The 360-TEPBGA packaged devices without an ATA interface (MCF54452 and MCF54453) do not have GPIO functionality on the following signals:

- ATA_BUFFER_EN
- ATA_CS[1:0]
- ATA_DA[2:0]
- ATA_RESET
- ATA_DMARQ
- ATA_IORDY

Workaround:

Use other pins with GPIO functionality when GPIO is required.

Fix plan:

Currently, there are no plans to fix this.

SECF162: Internal Resets Are Not Functional in SBF Mode

Errata type:

Silicon

Affected component:

SBF and Reset

Description:

When operating in SBF mode (BOOTMOD[1:0] = 11), internal SoC reset sources do not work reliably. This includes the software reset request (RCR[SOFTRST]) and the software and core watchdog timers.

Workaround:

Do not use internal SoC reset sources in SBF mode. External resets (toggling the RESET input pin) and power-on resets (POR) work correctly. If watchdog capability is needed in SBF mode, then use an external watchdog timer. If the capability for a software reset request is needed, then an external circuit could be added that monitors a GPIO line and asserts the RESET pin when the processor toggles the GPIO.

Fix plan:

Currently, there are no plans to fix this.

SECF180: Spurious Interrupts Can Cause Incorrect Vector Fetch

Errata type: Silicon

Affected component: INTC

Description: In rare cases the interrupt controller's spurious detection logic can cause a fetch to an incorrect vector number. This can occur when the core is starting the IACK for a spurious interrupt. During this small window of time, if a second interrupt at a different level arrives, the second interrupt causes the interrupt controller logic to clear the spurious request. Therefore, the interrupt controller sees no valid interrupt pending at the requested level and returns vector number 0 for INTC0 or vector number 64 for INTC1.

The second interrupt can be at any level other than the level that caused the spurious interrupt (it can even be a lower priority than the spurious interrupt). If the second interrupt is at the same level as the spurious interrupt, then the correct vector number for the second interrupt is returned.

Workaround: In many systems spurious interrupts represent error conditions in and of themselves. So, it is always a good design practice to eliminate potential causes of spurious interrupts during product development. Proper interrupt management can help to prevent or reduce the possibility of spurious interrupts (and the potential occurrence of this errata). The correct procedure for masking an interrupt in the INTC or inside the module is:

1. Write the interrupt level mask in the core's status register (SR[!]) to a value higher than the priority level of the interrupt you want to mask.
2. Mask the interrupt using the INTC's IMR and/or an interrupt mask register inside the module.
3. Write the original value back to the core's status register.

Even when steps are taken to remove spurious interrupts, it is still desirable to have a spurious interrupt handler to help manage unexpected events and glitches in a system. A workaround to allow for correct spurious interrupt handling is to:

1. After boot, copy the vector table to RAM
2. Modify the vector 0 and vector 64 entries so that they point to the spurious interrupt handler.

This way the system performs the same for any potential spurious interrupt vectors. Vectors 0, 64, and 24 (the correct spurious interrupt vector) should point to the same handler.

Fix plan: Currently, there are no plans to fix this.

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