

MCF54455 Chip Errata

Silicon Revision: All

Supports: MCF54450, MCF54451, MCF54452, MCF54453, MCF54454, and MCF54455

Introduction

This document identifies implementation differences between the MCF5445x processors and the description contained in the *MCF54455 ColdFire® Reference Manual*. Refer to <http://www.freescale.com/coldfire> for the latest updates.

Summary of MCF5445x Errata

The latest mask of the MCF5445x family is 2M22H.

Table 1. Summary of MCF5445x Errata

Errata	Module Affected	Date Errata Added	Revision Affected?	
			1M22H	2M22H
SECF041	SBF	9/13/07	Yes	No
SECF016	SRAM	9/13/07	Yes	No
SECF042	SBF	9/13/07	Yes	No
SECF034	PLL	9/13/07	Yes	No
SECF129	GPIO	10/9/08	Yes	Yes

Revision History

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
1		Initial revision

Rev. No.	Date	Substantive Changes
2	11/2008	Added 2M22H mask throughout. All pre-existing errata are fixed on this new mask. However, a new errata, SECF129 , was added to all masks.
3	10/2009	Changed status of SECF129 errata from 'Will be fixed.' to 'Currently, there are no plans to fix this.'

SECF041: Serial Boot with a Crystal

Errata type: Silicon

Affected component: SBF

Description: Booting using the serial configuration mode (BOOTMOD[1:0] == 11) with an external crystal can prevent the on-chip oscillator from starting properly. This is due to an uninitialized internal crystal oscillator enable signal from the chip configuration logic during the time between powering the part and the availability of all serial reset configuration data. If the on-chip oscillator is configured for external reference mode instead of crystal mode during that time, the external crystal does not operate correctly because the processor is not driving current on XTAL. Therefore, the crystal fails to drive a waveform into the device on EXTAL, and no internal clocks are generated by the oscillator to the PLL and other on-chip logic.

Workaround: Do not use serial configuration mode with an external crystal. Only parallel or default configuration modes should be attempted with a crystal, or use only an external clock source (instead of a crystal) for serial configuration mode.

Fix plan: Fixed in masks 2M22H and later.

SECF016: SRAM Simultaneous Reads

Errata type: Silicon

Affected component: V4 SRAM controller

Description: When the SRAM is enabled for core and backdoor port accesses, certain rare, but unpredictable, sequences/overlaps between core and backdoor port accesses result in incorrect read data. The core or the backdoor port access may obtain the incorrect data.

Workaround: Do not enable core and backdoor port accesses to the SRAM at the same time. The 32-kByte SRAM is controlled by RAMBAR1 with:

- Bit 0 = V (valid) — Enable direct SRAM accesses by the core
- Bit 9 = BDE (backdoor enable) — Allow access by non-core bus masters via the SRAM backdoor on the crossbar switch

Do not set V and BDE. Use one of the following settings instead:

Table 3. Available SRAM Access Modes

V	BDE	Description
0	0	No SRAM accesses allowed

V	BDE	Description
1	0	Only core accesses allowed
0	1	Only backdoor accesses allowed. Note: The core can still access the SRAM backdoor port via the crossbar switch.

Fix plan: Fixed in masks 2M22H and later.

SECF042: Serial Boot on 256-Pin Devices

Errata type: Silicon

Affected component: SBF

Description: Serial configuration mode on the 256-pin devices (MCF54450 and MCF54451) configures the device with incorrect data.

Workaround: Do not use serial configuration mode with the 256-pin devices. Only use parallel or default configuration modes.

Fix plan: Fixed in masks 2M22H and later.

SECF034: PLL Loss-of-lock at Large Voltage Differentials

Errata type: Silicon

Affected component: PLL

Description: There is a sensitivity to large differentials in IVDD and EVDD/OSCVDD in the PLL feedback path. This sensitivity can cause the PLL to lose lock and, in some cases, fail to generate output clocks.

Workaround: There are two requirements that must be met to avoid this errata:

1. Disable the PLL's loss-of-lock feature by setting bit 4 in the PLL status register (MCF_PLL_PSR |= 0x10).
2. Ensure that the IVDD, EVDD, and OSCVDD supplies are within the following limits:

Table 4. Supply Limits

Supply	Min	Max	Unit
IVDD	1.4	1.6	V
EVDD	3.0	3.45	V
OSCVDD	3.0	3.45	V

Fix plan: Fixed in masks 2M22H and later.

SECF129: GPIO Not Available on ATA Signals on MCF54452 and MCF54453

Errata type: Silicon

Affected component: GPIO

Description: The 360-TEPBGA packaged devices without an ATA interface (MCF54452 and MCF54453) do not have GPIO functionality on the following signals:

- ATA_BUFFER_EN
- ATA_CS[1:0]
- ATA_DA[2:0]
- ATA_RESET
- ATA_DMARQ
- ATA_IORDY

Workaround: Use other pins with GPIO functionality when GPIO is required.

Fix plan: Currently, there are no plans to fix this.

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