

## MCF52277 Chip Errata

Silicon Revision: All

Supports: MCF52274, MCF52277

### Introduction

This document identifies implementation differences between the MCF5227x processors and the description contained in the *MCF52277 ColdFire® Reference Manual*. Refer to <http://www.freescale.com/coldfire> for the latest updates.

### Summary of MCF5227x Errata

The latest version of the MCF5227x family is revision 1.3.

**Table 1. Summary of MCF5227x Errata**

Errata	Module Affected	Date Errata Added	Revision Affected?		
			Rev 1.1	Rev 1.2	Rev 1.3
<a href="#">SECF001</a>	Cache	11/02/07	Yes	Yes	Yes
<a href="#">SECF005</a>	Cache	11/02/07	Yes	Yes	Yes
<a href="#">SECF032</a>	LCD	11/02/07	Yes	No	No
<a href="#">SECF046</a>	Touchscreen	11/02/07	Yes	No	No
<a href="#">SECF040</a>	RTC	11/02/07	Yes	No	No
<a href="#">SECF033</a>	PLL	1/22/08	Yes	No	No
<a href="#">SECF014</a>	BDM	3/18/08	Yes	Yes	Yes
<a href="#">SECF121</a>	LCD	11/17/08	Yes	Yes	No
<a href="#">SECF122</a>	SBF	4/21/09	Yes	Yes	Yes
<a href="#">SECF126</a>	LCD	4/21/09	Yes	Yes	Yes
<a href="#">SECF150</a>	SDRAM	8/27/09	Yes	Yes	Yes

Use the table below to determine the revision using the part number and mask set markings on the device.

**Table 2. Part Number to Revision**

Orderable Part Number	Mask Set	Revision
PCF52274CLU120	M26H	Rev 1.1
MCF52274CLU120	2M26H	Rev 1.2
MCF52274CLU120	3M26H	Rev 1.3
PCF52277CVM160	M26H	Rev 1.1
MCF52277CVM160	M26H	Rev 1.1
SC52277F2CVM160	2M26H	Rev 1.2
MCF52277CVM160	3M26H	Rev 1.3

You can also use the chip identification register (CIR) to determine the silicon revision. The table below lists the CIR[PRN] field values that correspond to given revisions.

**Table 3. CIR[PRN] to Revision**

CIR[PRN] value	Revision
0	Rev 1.1
2	Rev 1.2
3	Rev 1.3

## Revision History

The table below provides a revision history for this document.

**Table 4. Document Revision History**

Rev. No.	Date	Substantive Changes
5	4/2008	Added level 2 trigger operation errata
6	12/2008	Added <a href="#">SECF121 "LCD Monochrome Mode Function Does Not Operate Correctly"</a>
7	2/2009	Updated <a href="#">SECF032, "LCD LSCLK Signal Misses Pulse Before LCD_OE Asserts"</a> . The errata is also present in any mode that has an 18-bit output. So, it affects 4bpp and 8bpp modes as well.
8	2/2009	Updated Status sections for <a href="#">SECF046, "Resolution of ASP ADC Channels"</a> , <a href="#">SECF033, "PLL Loss of Lock and Clock Jitter"</a> , and <a href="#">SECF121, "LCD Monochrome Mode Function Does Not Operate Correctly"</a>
9	5/2009	Added Rev 1.2 mask to Table 1 Added Table 2 Updated <a href="#">SECF032, "LCD LSCLK Signal Misses Pulse Before LCD_OE Asserts"</a> to <a href="#">SECF033, "PLL Loss of Lock and Clock Jitter"</a> to reflect the new Rev 1.2 mask. Added <a href="#">SECF122, "Possible SRAM Data Corruption When Booting from Internal SRAM Through the Serial Boot Facility"</a> Added <a href="#">SECF126, "Signal Multiplexing for the LCD Data Signals Does Not Function as Documented"</a>
10	6/2009	Changed workaround of <a href="#">SECF122, "Possible SRAM Data Corruption When Booting from Internal SRAM Through the Serial Boot Facility"</a> to TBD

Rev. No.	Date	Substantive Changes
11	6/2009	Added new workaround to <a href="#">SECF122, "Possible SRAM Data Corruption When Booting from Internal SRAM Through the Serial Boot Facility"</a>
12	8/2009	Added <a href="#">SECF150</a>
13	9/2009	Added new revision 1.3 device, which corrects <a href="#">SECF121</a> .

## SECF001: Incorrect Operation of Cache Freeze (CACR[CFRZ])

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	Version 2 ColdFire Cache
<b>Description:</b>	<p>The cache on the V2 ColdFire core is controlled by the cache control register (CACR). When the CACR[CFRZ] bit is set, the cache freeze function is enabled and no valid cache array entry is displaced. However, this feature does not always work as specified, sometimes allowing valid lines to be displaced when CACR[CFRZ] is enabled.</p> <p>This does not cause any corrupted accesses. However, there could be cache misses for data that was originally loaded into the cache but was subsequently deallocated, even though the CACR[CFRZ] bit was set.</p> <p>Also, incoherent cache states are possible when a frozen cache is cleared via the CACR[CINV] bit.</p>
<b>Workaround:</b>	Unfreeze the cache by clearing CACR[CFRZ] when invalidating the cache using the CACR[CINV] bit
<b>Workaround:</b>	Use the internal SRAM to store critical code/data if the system cannot handle a potential cache miss
<b>Fix plan:</b>	Currently, there are no plans to fix this.

## SECF005: Possible Cache Corruption After Clearing Cache (Setting CACR[CINV])

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	Version 2 ColdFire Cache
<b>Description:</b>	<p>The cache on the V2 ColdFire core may function as either:</p> <ul style="list-style-type: none"> <li>• a unified data and instruction cache</li> <li>• an instruction cache</li> <li>• a data cache</li> </ul> <p>The cache function and organization is controlled by the cache control register (CACR). The CACR[CINV] bit causes a cache clear. If the cache is configured as a unified cache and the CINV bit is set, the scope of the cache clear is controlled by two other bits in the CACR:</p> <ul style="list-style-type: none"> <li>• CACR[INVI] invalidates instruction cache only</li> <li>• CACR[INVD] invalidates data cache only</li> </ul> <p>If a write to the CACR is performed to clear the cache (CACR[CINV] = 1) and only a partial clear is done (CACR[INVI] or CACR[INVD] set), then cache corruption may occur.</p>

**Workaround:** All loads of the CACR that perform a cache clear operation (CACR[CINV] set) should be followed immediately by a NOP instruction. This avoids the cache corruption problem.

**Fix plan:** Currently, there are no plans to fix this.

## SECF014: Level 2 Trigger Operation Controlled by TDR[31]

**Errata type:** Silicon

**Affected component:** BDM

**Description:** The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

**Workaround:** Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 -- Level 2 trigger = PC\_condition & Address\_range & Data\_condition
- 1 -- Level 2 trigger = PC\_condition | (Address\_range & Data\_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

**Table 5. TDR[31:30] Definitions**

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor halt
10	PC_cond   (Add_range & Data_cond)	Debug interrupt
11		Reserved

**Fix plan:** Currently, there are no plans to fix this.

## SECF032: LCD LSCLK Signal Misses Pulse Before LCD\_OE Asserts

**Errata type:** Silicon

**Affected component:** LCD

**Description:** When operating in 4bpp, 8bpp, or 18bpp mode, the LSCLK signal misses a clock pulse in the clock cycle before LCD\_OE asserts. Since the missing clock pulse occurs when LCD\_OE is negated, most LCD panels operate correctly with no issue.

**Workaround:** If a continuous clock is needed even with LCD\_OE negated, then 12bpp or 16bpp modes can be used. In these modes the LSCLK does not miss the pulse.

**Fix plan:** Fixed on Rev 1.2 devices and later mask sets.

## SECF033: PLL Loss of Lock and Clock Jitter

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	PLL
<b>Description:</b>	<p>The original version of the PLL is sensitive to noise that can cause cycle-to-cycle jitter on the output clocks and, in some cases, cause the PLL to lose lock. This behavior of the PLL is related to the voltage used for the SDVDD rail and activity on the FlexBus.</p> <p>Using a nominal SDVDD of 3.3V is the worst case. FlexBus activity can trigger a loss-of-lock condition. When a loss of lock occurs, the output clock switches to the limp mode clock. Then, when lock is regained the system clocks return to using the PLL output. In addition, the output clock may also show cycle-to-cycle jitter even when the loss of lock does not occur (up to 2 ns).</p> <p>At a nominal 2.5V or 1.8V SDVDD, the PLL loss of lock does not occur. However, the PLL output clock can have cycle-to-cycle jitter. The cycle-to-cycle jitter should be less than 700 ps.</p>
<b>Workaround:</b>	When using 3.3V for SDVDD, loss-of-lock detection by the PLL can be disabled by setting bit four in the PLL status register (PSR). This prevents the output clocks from switching to the limp mode clock, but there can still be cycle-to-cycle jitter on the output clocks. However, a loss-of-lock event can occur when booting from memory on the FlexBus before there is a chance to disable the loss-of-lock detect in software.
<b>Workaround:</b>	Use 2.5V or 1.8V for the SDVDD supply. If there are no synchronous devices in the system running from a clock source other than the ColdFire device, then no workaround should be needed.
<b>Workaround:</b>	Use parallel boot, but boot the processor in limp mode. Once the loss-of-lock detect is disabled the PLL can be enabled.
<b>Workaround:</b>	Use a serial device and the serial boot facility (SBF) to configure the processor and execute code to disable the loss-of-lock detect.
<b>Workaround:</b>	Use an asynchronous non-volatile memory device for booting and disable the loss-of-lock detect in software as early as possible.
<b>Fix plan:</b>	On Rev 1.2 and later mask sets, during a loss-of-lock condition the device operates with the PLL output clock, if the PLL clock is present. The device does not switch to the limp clock, unless software programs it for limp mode operation.

## SECF040: RTC Operation in Stop Mode

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	RTC
<b>Description:</b>	On the original silicon, the RTC module stops counting when the device enters stop mode.
<b>Workaround:</b>	No workarounds
<b>Fix plan:</b>	On Rev 1.2 and later mask sets, the RTC continues to count in stop mode as long as its input clock is running. This way the RTC is able to wake the processor from stop mode.

## SECF046: Resolution of ASP ADC Channels

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	Touchscreen/ASP
<b>Description:</b>	On the original silicon, the resolution of the ADC channels that feed into the ASP block is lower than specified in the <i>MCF5227x Data Sheet</i> (approximately four bits of accuracy). The ADC logic is a new block, so the need for tuning of the circuit was expected and planned for in the silicon schedule.
<b>Workaround:</b>	No workarounds.
<b>Fix plan:</b>	The accuracy of the ADC circuit was increased on the Rev 1.2 and later mask sets. Please see the <i>MCF5227x Data Sheet</i> for the ASP ADC specifications.

## SECF121: LCD Monochrome Mode Function Does Not Operate Correctly

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	LCD
<b>Description:</b>	The LCD controller's monochrome mode does not work correctly.
<b>Workaround:</b>	Do not use monochrome mode. CSTN and TFT modes work correctly.
<b>Fix plan:</b>	Fixed on Rev 1.3 devices and later mask sets.

## SECF122: Possible SRAM Data Corruption When Booting from Internal SRAM Through the Serial Boot Facility

<b>Errata type:</b>	Silicon
<b>Affected component:</b>	SBF
<b>Description:</b>	When booting the device in SBF mode with a non-zero SBFSR[BLL] (using the SBF to copy code into the internal SRAM), attempting to execute a movec instruction will write data to the corresponding lonword address in the on-chip SRAM instead of the CPU space register.
<b>Workaround:</b>	Do not execute movec instructions when using SBF mode to boot from the internal SRAM. This means that the RAMBAR, VBR, CACR, and ACR <sub>n</sub> registers cannot be programmed. The inability to program the CPU space registers has the following effects: <ul style="list-style-type: none"><li>• The core has single cycle access to the on-chip SRAM starting at address 0x0000_0000. To avoid overlap with the on-chip SRAM, do not use the first 128 KBytes of the FlexBus memory space (0x0000_0000 - 0x3FFF_FFFF).</li><li>• The SRAM is still accessible in the 0x8000_0000 - 0x8FFF_FFFF through the SRAM's back door. Use this address range for any non-core masters that need access to the SRAM.</li><li>• Cache cannot be used.</li></ul>

In addition, the BDM functionality is impacted. BDM can be used to read and write memory and module registers. The BDM uses CPU space to read and write the PC, so run and single-step functions do not work correctly.

**Fix plan:** TBD

## SECF126: Signal Multiplexing for the LCD Data Signals Does Not Function as Documented

**Errata type:** Silicon

**Affected component:** LCD

**Description:** The signal multiplexing for the LCD\_Dn pins does not work as specified in the PAR\_LCDH and PAR\_LCDL register descriptions in the *MCF5227x Reference Manual*. Setting any of the PAR\_LDn bit fields to 10 (alternate 1 function) may affect the signal used on non-corresponding pins, as shown in the following table.

For example, if PAR\_LD0 = 10 and PAR\_LD2 = 00, the LCD\_D0 pin is configured as the PWM1 signal and LCD\_D2 is configured as LCD\_D0, not GPIO.

### NOTE

If all PAR\_LDn fields are 11, the LCD\_Dn pins function as LCD data signals and are not affected by this errata.

### NOTE

If all PAR\_LDn fields are 00, the LCD\_Dn pins function as GPIO and are not affected by this errata.

**Table 6. PAR\_LDn Affect on Pin**

PAR_LCDH or PAR_LCDL Bit Name	10 (First Priority)	11 (Second Priority)	00 (Third Priority)
PAR_LD0	LCD_D0 = PWM1 LCD_D2 = LCD_D0	LCD_D0 = LCD_D0	LCD_D0 = GPIO
PAR_LD1	LCD_D1 = PWM3 LCD_D3 = LCD_D1	LCD_D1 = LCD_D1	LCD_D1 = GPIO
PAR_LD2	LCD_D2 = LCD_D0 LCD_D4 = LCD_D2	LCD_D2 = LCD_D2	LCD_D2 = GPIO
PAR_LD3	LCD_D3 = LCD_D1 LCD_D5 = LCD_D3	LCD_D3 = LCD_D3	LCD_D3 = GPIO
PAR_LD4	LCD_D4 = LCD_D2 LCD_D8 = LCD_D4	LCD_D4 = LCD_D4	LCD_D4 = GPIO
PAR_LD5	LCD_D5 = LCD_D3 LCD_D9 = LCD_D5	LCD_D5 = LCD_D5	LCD_D5 = GPIO

PAR_LCDH or PAR_LCDL Bit Name	10 (First Priority)	11 (Second Priority)	00 (Third Priority)
PAR_LD6	LCD_D6 = PWM5 <b>LCD_D10 = LCD_D6</b>	LCD_D6 = LCD_D6	LCD_D6 = GPIO
PAR_LD7	LCD_D7 = PWM7 <b>LCD_D11 = LCDD7</b>	LCD_D7 = LCD_D7	LCD_D7 = GPIO
PAR_LD8	LCD_D8 = LCD_D4 <b>LCD_D14 = LCD_D8</b>	LCD_D8 = LCD_D8	LCD_D8 = GPIO
PAR_LD9	LCD_D9 = LCD_D5 <b>LCD_D15 = LCD_D9</b>	LCD_D9 = LCD_D9	LCD_D9 = GPIO
PAR_LD10	LCD_D10 = LCD_D6 <b>LCD_D16 = LCD_D10</b>	LCD_D10 = LCD_D10	LCD_D10 = GPIO
PAR_LD11	LCD_D11 = LCD_D7 <b>LCD_D17 = LCD_D11</b>	LCD_D11 = LCD_D11	LCD_D11 = GPIO
PAR_LD12	LCD_D12 = CANRX	LCD_D12 = LCD_D12	LCD_D12 = GPIO
PAR_LD13	LCD_D13 = CANTX	LCD_D13 = LCD_D13	LCD_D13 = GPIO
PAR_LD14	LCD_D14 = LCD_D8	LCD_D14 = LCD_D14	LCD_D14 = GPIO
PAR_LD15	LCD_D15 = LCD_D9	LCD_D15 = LCD_D15	LCD_D15 = GPIO
PAR_LD16	LCD_D16 = LCD_D10	LCD_D16 = LCD_D16	LCD_D16 = GPIO
PAR_LD17	LCD_D17 = LCD_D11	LCD_D17 = LCD_D17	LCD_D17 = GPIO

**Workaround:** Use the table above to properly select the desired signals.

**Fix plan:** Currently, there are no plans to fix this.

## SECF150: Potential Boot Failure When Using Unified SDR bus/FlexBus Mode

**Errata type:** Silicon

**Affected component:** SDRAM controller

**Description:** If the SD\_CKE signal to the SDRAM deasserts while one or more banks are active, the SDRAM enters a clock suspend state. If the SDRAM was driving the data lines before entering the clock suspend state, the buffers continue to drive.

During a reset, the processor deasserts SD\_CKE without any graceful stop period to ensure that the SDRAM banks are all in an IDLE state. In some cases, the SDRAM could be driving the data bus during and immediately after reset. This can lead to possible bus contention while reading boot code from flash.

**Workaround:** Use a split bus mode configuration with DDR SDRAM or SDR SDRAM. This creates a dedicated 16-bit port for the SDRAM on D[31:16]. In this configuration, the SDRAM does not share data lines with other devices, so bus contention is not an issue.

**Workaround:** Add a pullup resistor on the SD\_CKE signal. This allows the SDRAM memory to recognize clocks during processor startup, and should allow banks to return to the IDLE state.

**Fix plan:** Currently, there are no plans to fix this.

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