



Integrated Communications Processors

Modular AdvancedMC™ Platform for WiMAX Base Stations



A New Generation of WiMAX Base Stations

WiMAX is an emerging standard under development by the WiMAX Forum (www.wimax.org) to deliver next-generation broadband wireless technology for wide area networks. WiMAX targets higher throughput, lower latency and efficient IP backhaul compared to previous wireless network technologies. It offers a new mass deployable wireless network technology which should herald a new age of rich multimedia and real-time services.

Turning Vision into Reality with Freescale's Rapid System Development Platform

As the WiMAX market evolves from Wave1 and Wave2 towards future 802.16m standards, Freescale has developed a comprehensive hardware and software reference package which enables OEMs to quickly plug together their own systems for evaluation and development. The Rapid System Development Platform delivers a modular, programmable base station reference platform based on:

- Industry-leading processors, including networking communication processors built on Power Architecture™ technology and DSPs based on StarCore® technology
- PCI Industrial Computers Manufacturing Group (PICMG®) standard AdvancedMC (AMC)
- Layer 1 and 2 baseband enablement software for base station developments on Freescale processors

Platform Benefits

- “Jump starts” time to market
- Accelerates prototyping and development time
- Helps to lower cost of ownership
- Offers portable C-based software baseline for low latency, high throughput systems

OEM Availability

The Rapid System Development reference platform, including both hardware and software, is specifically targeted for use by OEM customers developing base station equipment solutions. The individual AdvancedMC™ platform hardware components are widely available from a combination of Freescale and Freescale Alliance Partners, and the software is available under license to OEMs.

Rapid System Development Platform Ingredients		
Function	Component	Content/Deliverables
Platform base	MicroTCA™ chassis Part #11850-013 (Schroff®)	<ul style="list-style-type: none"> • Industry-standard MicroTCA development chassis • Available direct from Schroff
Baseband Layer 2 processor board	MPC8548 AMC (PowerQUICC® processor-based AMC) Part #CWH-PPC-8548N-VE (Freescale)	<ul style="list-style-type: none"> • Board with user documentation • Linux® board support package (BSP) • Optional schematics, Orcad originals, Gerber files, layout files
Baseband Layer 1 processor board	MSC8144 StarCore® DSP AMC Part # MSC8144AMC-S (Freescale)	<ul style="list-style-type: none"> • Board with user documentation • SmartDSP-OS board support package • Optional schematics, Orcad originals, Gerber files, layout files
Layer 2 software package (under OEM license)	L2 Software	<ul style="list-style-type: none"> • Object library, source code, GCC build environment • Test harness • Documentation
Layer 1 software package (under OEM license)	L1 Software	<ul style="list-style-type: none"> • Object library, source code, CodeWarrior® build environment • Test harness • MATLAB® models • Documentation

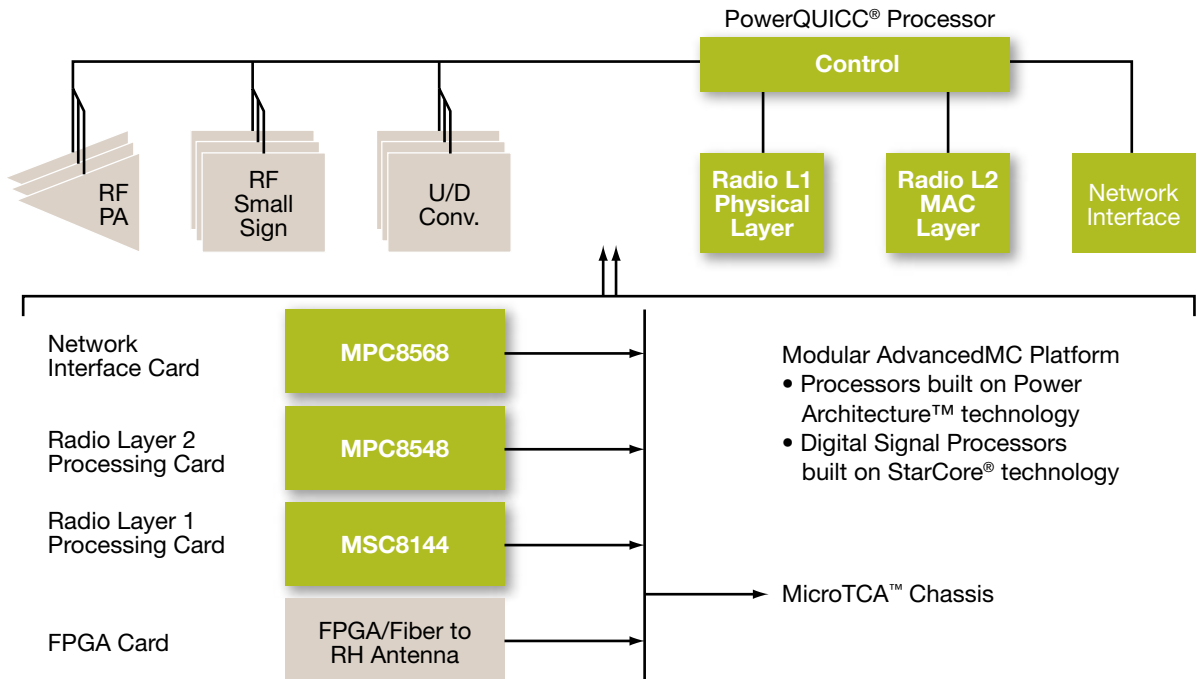
AMC Hardware Platform Details

The broadband wireless baseband processing reference hardware is based on multiple modular PICMG defined AMC modules plugged into a compact MicroTCA™ chassis. The ability to use AMC modules directly, without the need for an AdvancedTCA® or a custom carrier, enables substantial reductions in size, cost and power. The modular approach also enables individual components of the system to be upgraded or even cost reduced, as newer hardware becomes available over time. This accelerates developer timelines and streamlines support. The baseline platform focuses on the Baseband Layer 1/Layer 2 processing, but the same system can be extended by adding control, network interface and FPGA cards to provide a WiMAX “Base Station-in-a-Box” solution. The baseline hardware platform components available are shown to the right.

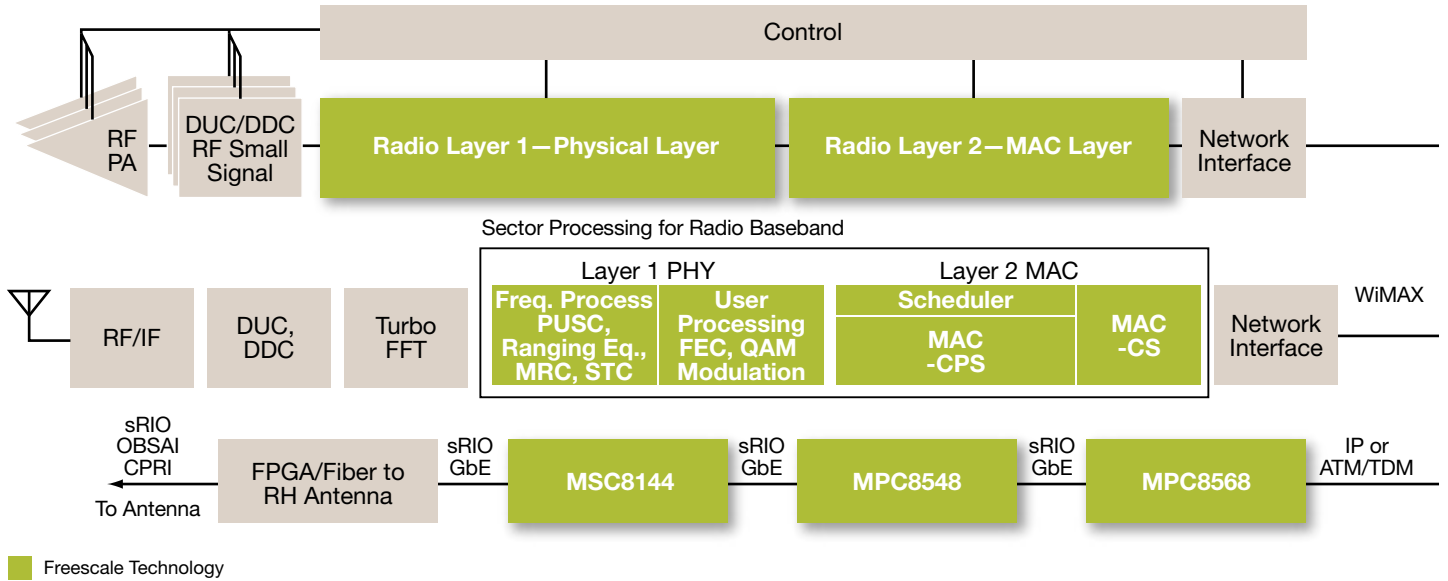
Baseline Hardware Platform Components

Function	Category	Specifications/Features
Platform base	MicroTCA™ Chassis	<ul style="list-style-type: none"> Schroff® MicroTCA development chassis Part # 11850-013 (Schroff)
Baseband Layer 2 processor card	MPC8548 AMC	<ul style="list-style-type: none"> Processor: MPC8548 up to 1.3 GHz with integrated Serial RapidIO® and Gigabit Ethernet (GbE) Operation: Stand alone or AMC plug in card Memory: DDR2 SODIMM, 16 MB ROM Fabric: Gigabit Ethernet (3 x SerDes) AMC Connectivity: B+ connector, 2 x MDI for GbE, x1/x4 Serial RapidIO IPMC: Board power up, temperature monitoring, E-keying, status LEDs Form factor: AMC single width, full height: 180.6 mm x 73.5 mm Part #CWH-PPC-8548N-VE (Freescale), RoHS version
Baseband Layer 1 PHY processor card	MSC8144 AMC	<ul style="list-style-type: none"> Processor: 4 x MSC8144 StarCore® DSPs up to 1.0 GHz with integrated Serial RapidIO and GbE Operation: Stand alone or AMC plug in card Memory: 256 MB of 32-bit wide DDR2 per MSC8144 Connectivity: <ul style="list-style-type: none"> 2 x Serial RapidIO (x4) interfaces from backplane routed to DSP farm via Serial RapidIO switch 2 x 1000BaseX Gigabit Ethernet from backplane ports via Ethernet switch 1 x Gigabit Ethernet on front plane expansion connector via Ethernet switch E1/T1 TDM connection via 8 Tx/Rx on AMC connector Boot: Stand alone (via onboard I²C) or via back plane (e.g. Serial RapidIO, Ethernet) Form factor: AMC single width, full height: 180.6 mm x 73.5 mm Part # MSC8144AMC-S (Freescale)

Modular AdvancedMC™ Mezzanine Hardware Platform Diagram



System Architecture Partitioning Diagram



System Architecture Partitioning

The base station system architecture is cleanly partitioned between separate network, Radio Layer 2 and Radio Layer 1 processors as shown above. It should be noted that for lower scale solutions—like micro-base stations—it is practical to consolidate these functions into fewer components, but the baseline reference design addresses the scaling needed for multi-sector macro-base station solutions, where each sector delivers high throughput and optimum range.

Major Architectural Block Responsibilities

Layer 1 – Physical

Performs the Physical Layer Radio User, Frequency and Time processing as well as processing of ranging data and MIMO multiple antenna techniques ready to carry the logical radio transport channels and higher layers over the air interface.

Layer 2 – Medium Access Control

Performs the MAC-CPS and Scheduler components that controls the base station and subscriber access to air interface resources. Resources are scheduled according to Quality of Service (QoS) requirements, using packet fragmentation/packing and retransmission via automatic repeat request (ARQ).

Network Interface

Performs network backhaul transport and interworking with internal interfaces. This includes processing the MAC-CS, which includes functions such as classification and header compression.

Layer 1 and Layer 2 Radio Software Architecture

Layer 1/Layer 2 real-time software subsystems combine together to offer several key baseband ingredients for an air interface conduit to mobile subscribers. The Layer 1/ Layer 2 real-time software subsystems can operate in concert, through a commonly defined architecture and Layer 1/Layer 2 interface. This interface can not only ensure efficient inter-operation of the two, but also enables advanced features and scheduling algorithms between them. The effort in the system and interface definition should translate into time to market savings for the developer, and can be considered as a baseline Layer 1/Layer 2 solution for OEMs to add differentiating intellectual property.

Layer 2—Data Plane Module Software

Freescall provides a set of OS independent modules covering the Layer 2 processing that is executed in real time. All software is delivered as a set of modules for MAC-CS, MAC-CPS and scheduler that can be ported to any RTOS. Designed for maximum real-time throughput, several optimized hardware specific software drivers can be included for optimum performance. All software is developed in ANSI-C, fully documented, flexible and extensible in design, with an emphasis on the scheduler architecture. As a design aid, the software can be delivered as an application running under User Mode Linux®. Further details are listed to the right.

Dataplane Module Software Features	
Category	Specifications/Features
Design approach	<ul style="list-style-type: none"> • Modular and portable C software modules for MAC-CS, MAC-CPS and scheduler • Sample single thread L2 data-plane processing chain • Runs under any RTOS environment, and independent of the RTOS and associated drivers performance. Achieved by using: <ul style="list-style-type: none"> ◦ Custom memory/buffer management, timer management and drivers for performance-critical hardware/coprocessor offload such as security and DMA ◦ Minimum number of software threads for data plane operation ◦ No OS specific calls in any of the data plane modules ◦ Abstraction/rerouting of trace/debug information • Control plane (not included) interaction possible through APIs to configure appropriate data-plane operation • Designed with the latest available drafts of specifications
RTOS support	<ul style="list-style-type: none"> • RTOS agnostic implementation • Example includes software ported to Linux® User Mode
API	<ul style="list-style-type: none"> • Full software abstraction between data plane/control plane and data plane/scheduler through well-defined and documented APIs
Validation/Test	<ul style="list-style-type: none"> • Software tested on <ul style="list-style-type: none"> ◦ Unit level (individual modules) ◦ Integration level (module interaction) ◦ System level (system operation, performance) • Software test environment bundled with software release
1. Medium Access Control Convergence Sub-layer (MAC-CS)	<ul style="list-style-type: none"> • Compatible to IEEE® 802.16e standard
2. Medium Access Common Part Sub-layer (MAC-CPS)	<ul style="list-style-type: none"> • Compatible to IEEE 802.16e standard • Includes downlink/uplink scheduler
3. L2/L1 interface	<ul style="list-style-type: none"> • L2/L1 interface designed for efficient integration with Freescale L1 solution
4. Framework	<ul style="list-style-type: none"> • Example integrated processing chain running under Linux: <ul style="list-style-type: none"> ◦ Demonstrates integration of L2 modules ◦ Provides known development/test environment



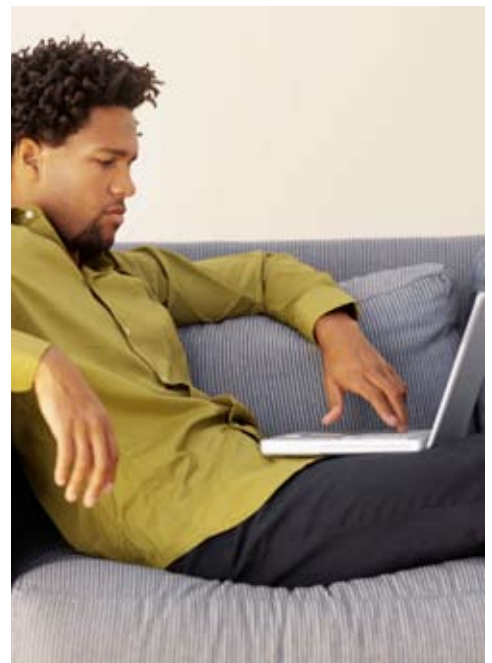
Layer 1—Real-Time Software Subsystem

The LTE Layer 1 software includes physical baseband channel processing and radio transport channel functions as defined in the 802.16d/e standards. Freescale provides a comprehensive set of kernel modules covering the Layer 1 processing for User Processing, Frequency Processing and Time Processing. The kernels are further combined into uplink and downlink chains which run real time using the SmartDSP real-time operating system as a reference. All software is developed as ANSI-C callable and fully documented.

In brief, the physical layer processing functions include:

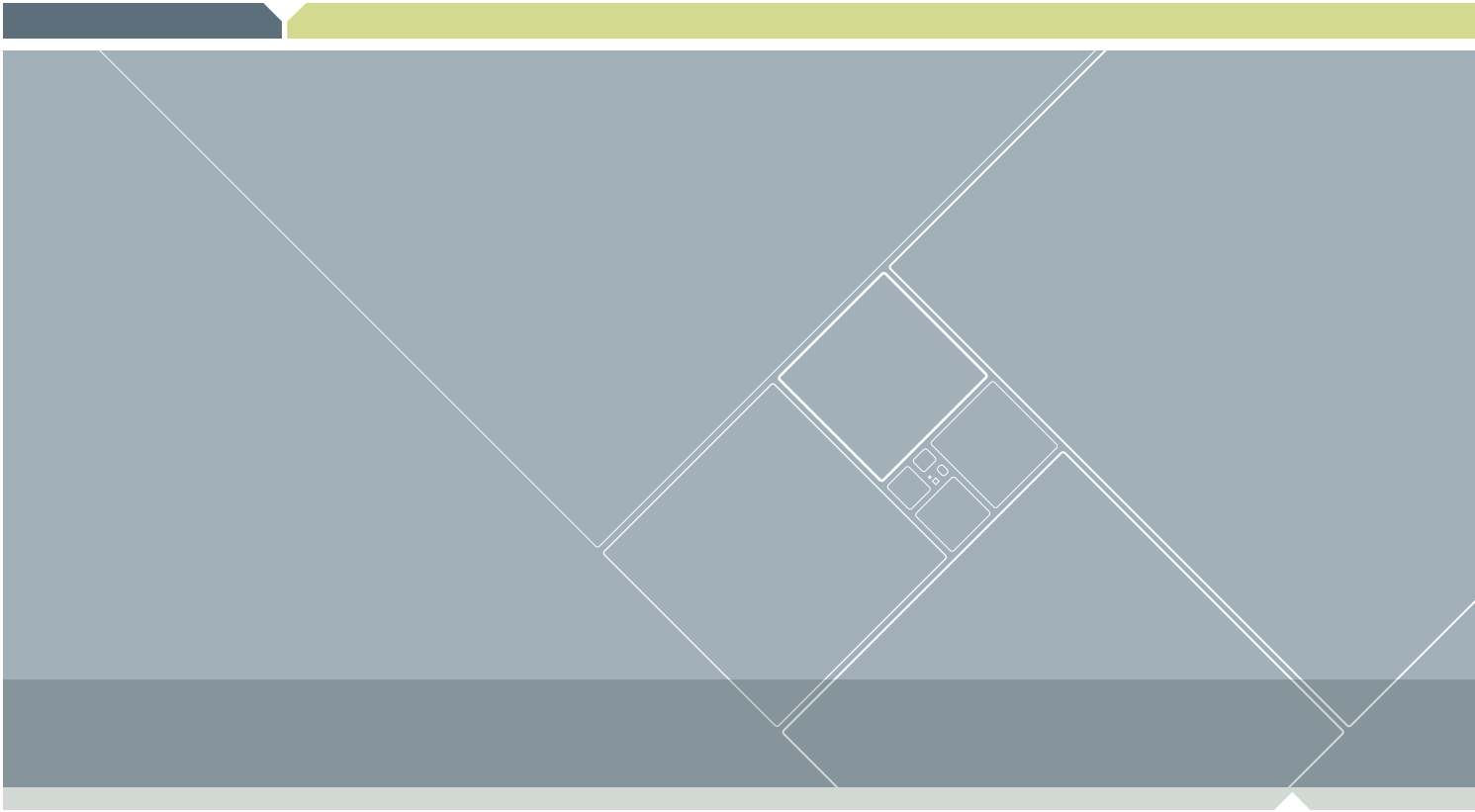
- Modulation
- Channel coding
- Transmission schemes
- Ranging
- Channel estimation
- Equalization

Further details are listed on the following page.



Real-time Software Subsystem Features

Category	Specifications/Features
Design approach	<ul style="list-style-type: none"> • Layered API software approach enables multi-level reuse eases integration with custom and IP • Modular C software modules for all subsystems—includes C wrapper for optimized real-time assembly modules • Algorithm verification with floating and fixed point simulation system • Multi-core framework allows for efficient inter-core communication and task partitioning
Features	<ul style="list-style-type: none"> • User Processing <ul style="list-style-type: none"> ◦ DL Encoding ◦ Modulation ◦ UL Decoding • Frequency Processing <ul style="list-style-type: none"> ◦ PUSC and FUSC Physical Mapping and De-Mapping ◦ STC ◦ Channel Equalizer ◦ MRC Combining ◦ Ranging • Time Processing <ul style="list-style-type: none"> ◦ FFT, IFFT, Scaling • Modular design with well defined interfaces and module interactions <ul style="list-style-type: none"> ◦ e.g. Downlink <ul style="list-style-type: none"> .. IF1Tx: L1/L2 logical interface .. IF2Tx: User to frequency processing interface .. IF3Tx: Frequency to time domain processing—remaps IFFT signal generation onto FPGA .. IF4Tx: Baseband I/Q sample interface towards the antenna FPGA ◦ Message based configuration and runtime control • 3rd Party enhancements are available for all aspects of the PHY solution
RTOS support	<ul style="list-style-type: none"> • SmartDSP OS: Integrates real-time kernels and drivers
API	<ul style="list-style-type: none"> • Full software abstraction through well-defined and documented APIs <ul style="list-style-type: none"> ◦ SBL1 API structure for reuse on function level ◦ Framework API for reuse of higher level, complete processing chains ◦ Complete subsystem reuse possible for channel types
Validation/Test	<ul style="list-style-type: none"> • Software tested on <ul style="list-style-type: none"> ◦ Unit level (individual modules) ◦ Integration level (module interaction) ◦ System level (system operation, performance) • Software test environment is part of the software delivery package
Standards reference	Compatible to IEEE® 802.16e standard
Layer 1 software packages	<ul style="list-style-type: none"> • Signal Processing Library: contains WiMAX Layer 1 signal processing chains and kernel library functions. The signal processing kernels are the basic processing units and the signal processing manager is the chain integration of a set of kernels which includes: <ul style="list-style-type: none"> ◦ Randomizer, FEC encoder and symbol mapper ◦ Slot mapping logical to physical mapping for PUSC and FUSC modes ◦ IFFT/FFT, frequency guard and CP management • MATLAB® Model Package <ul style="list-style-type: none"> ◦ Delivers: <ul style="list-style-type: none"> .. UL/DL Loopback, CC and CTC, QPSK, 16QAM, 64QAM (DL only), BER Testbench, Ranging and Fast Feedback Decode ◦ Enables test vector generation • Functional integration of uplink/downlink chains on multi-core MSC8144 <ul style="list-style-type: none"> ◦ Uses SmartDSP OS real-time operation



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