

MPC560xP and MPC564xL Compatibility

Transition from MPC5604P to MPC5643L in QFP 144 packages

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The high performance MPC56xxx MCU architecture, which includes the MPC560xP family, now adds the MPC564xL family, supporting higher functional safety levels, significantly higher performance, and enhanced peripheral modules. This application note describes common properties of, and the differences between, the MPC560xP and MPC564xL families, plus steps that allow maximize reuse of software and hardware between the two families.

The MPC560xP and the MPC564xL MCUs are both part of the microcontroller family targeted for automotive chassis applications and designed to reach a high level of compatibility. They are based on the same skeleton architecture and share a wide set of identical peripheral modules.

The MPC564xL family of devices is targeted for SIL3 and ASIL-D applications and therefore, when compared to the MPC560xP family, has additional functional safety measures implemented. The MPC564xL implements an application-independent architecture to

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Block diagrams

reach its functional safety target. This application independence allows the MPC564xL to reach a high level of compatibility with other MCUs within the chassis family, such as the MPC560xP.

NOTE:

The MPC5604P comparison is done for MPC5604P cut 2.0 and higher only.

The compatibility comparison between the two families is based on two selected devices — the MPC5604P and the MPC5643L — which are both available in a 144-pin QFP package.

For this comparison the MPC5643L is operated in lockstep mode, which allows the application to access the sphere of replication as a single logical processing channel. Decoupled parallel mode (DPM) is not discussed in this document.

1 Block diagrams

Figure 1 shows a simplified version of the MPC5643L architecture on a block diagram level. It shows the dual core architecture and other replicated IP modules as well as the Redundancy Control and Checker Units (RCCU) from a hardware perspective. Please refer to reference document [1] for a more detailed block diagram of the MPC5643L architecture.

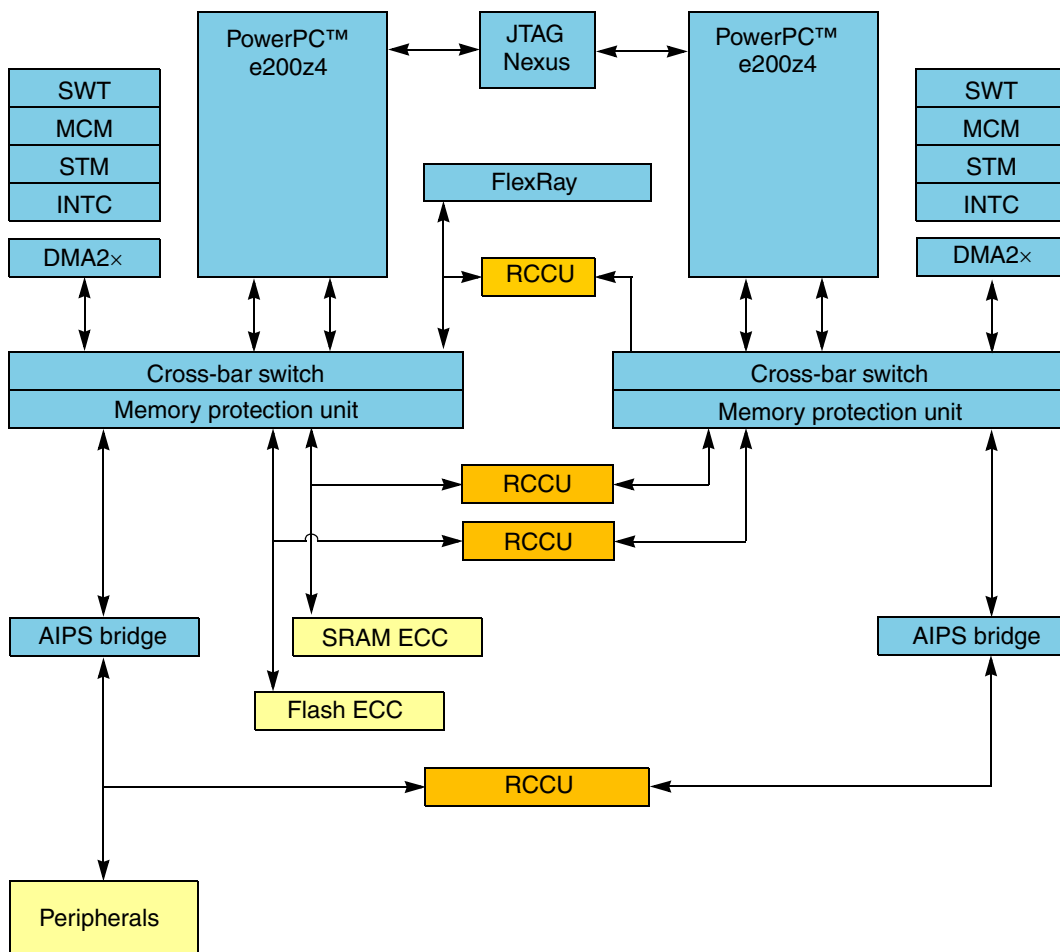


Figure 1. MPC5643L architecture block diagram hardware view

For this application note, comparing the MPC5604P and the MPC5643L in LSM, it is more relevant to compare the software view of both architectures. This is because it is the architecture that will be visible to the application software when the MPC5643L is operated in lockstep mode. This comparison is shown in Figure 2 and Figure 3 below.

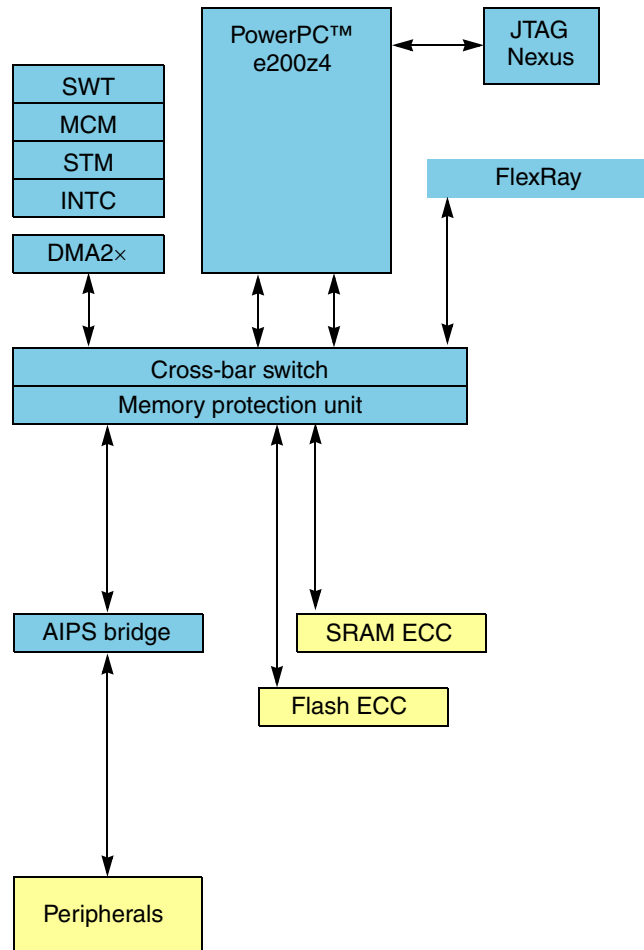


Figure 2. MPC5643L block diagram — software view in LSM

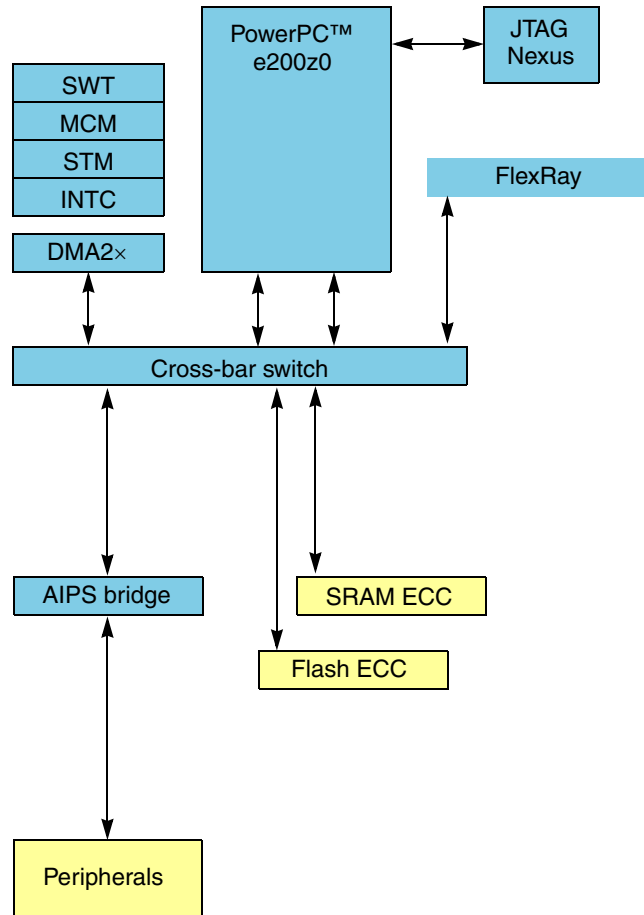


Figure 3. MPC5604P block diagram

The comparison of these two views shows that the MPC5643L sphere of replication in LSM is completely transparent for application software. In that mode, the MPC5643L can be treated and programmed as a single-core device with enhanced fault-detection capabilities.

2 Overview

Table 1 shows an overview of the feature set of the two products. A more detailed description of both the common features and of the differences is given in the next sections.

Table 1. MPC560xP and MPC564xL feature overview

Features	MPC5604P	MPC5643L
Platform architecture	Single core mode	Lockstep mode ¹ or decoupled parallel mode
CPU core	e200 z0hn2	e200 z446n3
Core bus interface	Harvard (instruction, data)	
Signal processing unit (SPE)	—	SPE 1.1
Floating point unit (FPU)	—	EFP2

