

MultiMediaCard/Secure Digital Host Controller Addendum

MC9328MX21

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1 Introduction

This document is written as an addendum to the i.MX21 Applications Processor reference manual's MultimediaCard/Secure Digital Host Controller (MMC/SDHC) chapter. This document provides suggestions and guidelines for the following:

- Hardware connectivity and IO pad configuration
- MMC/SD clocking
- Interrupt and DMA Channels for the MMC/SD host controllers
- Relationship of the STATUS and INT_CNTR registers
- Sequence of SDIO/non-SDIO interrupt handling
- Multiple MultiMediaCard support
- Card detection

SPI mode will not be discussed in this document.

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2 Hardware Connectivity

The Hardware connectivity between the MMC/SD host controller and cards is the collaboration of the MMC/SD host controller module, GPIO module, and the System Controller settings.

2.1 The SD Signal and MMC Signal

The MMC/SD host controller pin assignment is provided in [Table 1](#).

Table 1. Pin Assignment of the MMC/SD Host Controllers

SD				MMC	
Pin #	Name	Description	Other Function in SD/SDIO	Name	Description
1	DAT3	Data Line [bit-3]	Card Detect (SD and SDIO)	Reserved	Reserved for future use
2	CMD	Command/Response	–	CMD	Command/Response
3	Vss1	Supply Voltage Ground	–	Vss1	Supply Voltage Ground
4	Vdd	Supply Voltage	–	Vdd	Supply Voltage
5	CLK	Clock	–	CLK	Clock
6	Vss2	Supply Voltage Ground	–	Vss2	Supply Voltage Ground
7	DAT0	Data Line [bit-0]	–	DAT	–
8	DAT1	Data Line [bit-1]	Interrupt (SDIO only)	N/A	–
9	DAT2	Data Line [bit-2]	Read Wait (SDIO only)	N/A	–

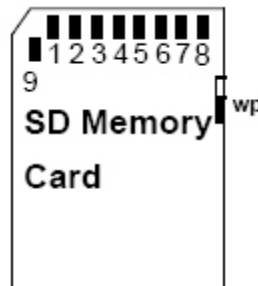


Figure 1. Physical Structure of an SD Card

2.2 The Physical Connection with i.MX21

Table 2 identifies the pin names of MMC/SDHC-1 and MMC/SDHC-2 and the associated GPIO pins.

Table 2. Pin Names of SDHC and the According GPIO Pins

Signal Name in SD Spec	MMC/SDHC1			MMC/SDHC2		
	Signal Name in i.MX21	Associated GPIO	Pull-Up/ Pull-Down	Signal Name in i.MX21	Associated GPIO	Pull-Up/ Pull-Down
CLK	SD1_CLK	PE23	N/A	SD2_CLK	PB9	N/A
CMD	SD1_CMD	PE22	Internal Pull-Up	SD2_CMD	PB8	Internal Pull-Up
DAT3	SD1_D3	PE21	Internal Pull-Up ¹	SD2_D3	PB7	Internal Pull-Up ¹
DAT2	SD1_D2	PE20	Internal Pull-Up	SD2_D2	PB6	Internal Pull-Up
DAT1	SD1_D1	PE19	Internal Pull-Up	SD2_D1	PB5	Internal Pull-Up
DAT0	SD1_D0	PE18	Internal Pull-Up	SD2_D0	PB4	Internal Pull-Up

¹ For the card detection function, the user may occasionally use an external pull-low resistor. For more details about card detection, please read Table 3 Footnote in Section 2.3, “Setting of the GPIO Pins” and Section 8, “Card Detection”.

2.3 Setting of the GPIO Pins

Every GPIO in the i.MX21 processor is multiplexed with different functional modules in i.MX21. To use the MMC/SDHC function, the user must configure the GPIO pad to be used as the primary function. To configure the function of a GPIO pad, use the registers in the GPIO module identified in Table 3.

Table 3. GPIO Register Settings for MMC/SDHC Function

Set 1 / 0	SD1_CLK	SD1_CMD	SD1_D3	SD1_D2	SD1_D1	SD1_D0
DDIR	not necessary to be configured					
OCR1 / OCR2	not necessary to be configured					
ICONFA1 / ICONFA2	not necessary to be configured					
ICONFB1 / ICONFB2	not necessary to be configured					
DR	not necessary to be configured					
GIUS	0	0	0	0	0	0
SSR	not necessary to be configured					
ICR1 / ICR2	not necessary to be configured					
IMR	not necessary to be configured					
ISR	not necessary to be configured					
GPR	0	0	0	0	0	0
PUEN	0	1	1 ¹	1	1	1

¹ According to reference [2], an internal pull-up resistor in the SD card for card detection is optional. The MMC/SDHC in i.MX21 supports this feature. When using this card detection feature, the interrupt pull-up resistor of SD_D3 must not be used (set to 0) at the card identification stage. Otherwise, continue to use the interrupt pull-up resistor (set to 1) in i.MX21. More details about card detection is discussed in Section 8, “Card Detection”.

The GIUS register is configured to use multiplexed functions.

The CPR register is configured to use the multiplexed primary function. There may be two functions multiplexed which are primary and secondary functions.

The PUEN register is configured (set to 1) to use internal pull-up resistor.

Please read sample code `SDHC_Port_Init()` in [Appendix A on page 14](#) for reference.

Details of GPIO setting can be found in General-Purpose I/O chapter in [1].

2.4 Driving Strength

In the i.MX21 processor, the user can set the driving strength for different groups of IO pads. Depending on the PCB design and the use of the GPIO, the user can meet their requirements for different connected devices. For example, the user can set the DSCR1 register value to increase or decrease the driving strength for the entire group of IO pads for MMC/SDHC-1. Once set, the driving strength of all six IO pins is changed within the group for MMC/SDHC-1 (SD1_CLK, SD1_CMD, SD1_DAT3, SD1_DAT2, SD1_DAT1 and SD1_DAT0).

Table 4. Setting Driving Strength

Location	MMC/SDHC-1		MMC/SDHC-2	
Register	DSCR1			
Field	DS_SLOW1	setting: 000 = 2mA 001 = 4mA 011 = 8mA 111 = 12mA	DS_SLOW7	setting: 000 = 2mA 001 = 4mA 011 = 8mA 111 = 12mA
Bit Number	[2:0]	–	[21:19]	–

Please read [Example 1](#) `SDHC_Port_Init()` in [Appendix A on page 14](#) for reference.

For more details about driving strength settings, please read System Control chapter in [1].

2.5 Operation Logic Voltage

Generic MMC and SD memory cards support an operating voltage of 2.0V to 3.6V. The MMC/SD host controllers in i.MX21 processors have individual operation voltage inputs; NVdd2 for MMC/SDHC-1 and NVdd5 for MMC/SDHC-2. Users can easily adjust the operating voltage inputs to meet their design requirements. For example, if NVdd2 is changed from 3.3V to 3.6V, then the logic voltage of all six IO pins for MMC/SDHC-1 are changed to 3.6V within the group (SD1_CLK, SD1_CMD, SD1_DAT3, SD1_DAT2, SD1_DAT1 and SD1_DAT0). Please note that the same voltage supply must also be provided to the Vdd (Pin 4) of the SD card.

You can change the supply voltages to NVdd2 and NVdd5 at anytime, as necessary, to change the operating voltages of the SD cards. There are no register setting changes required to change the operating voltage inputs for NVdd2 or NVdd5.

For more information read the Signal Descriptions and Pin Assignments chapter of reference [1].

