

# NXP T4240 Ver:C COVER SHEET

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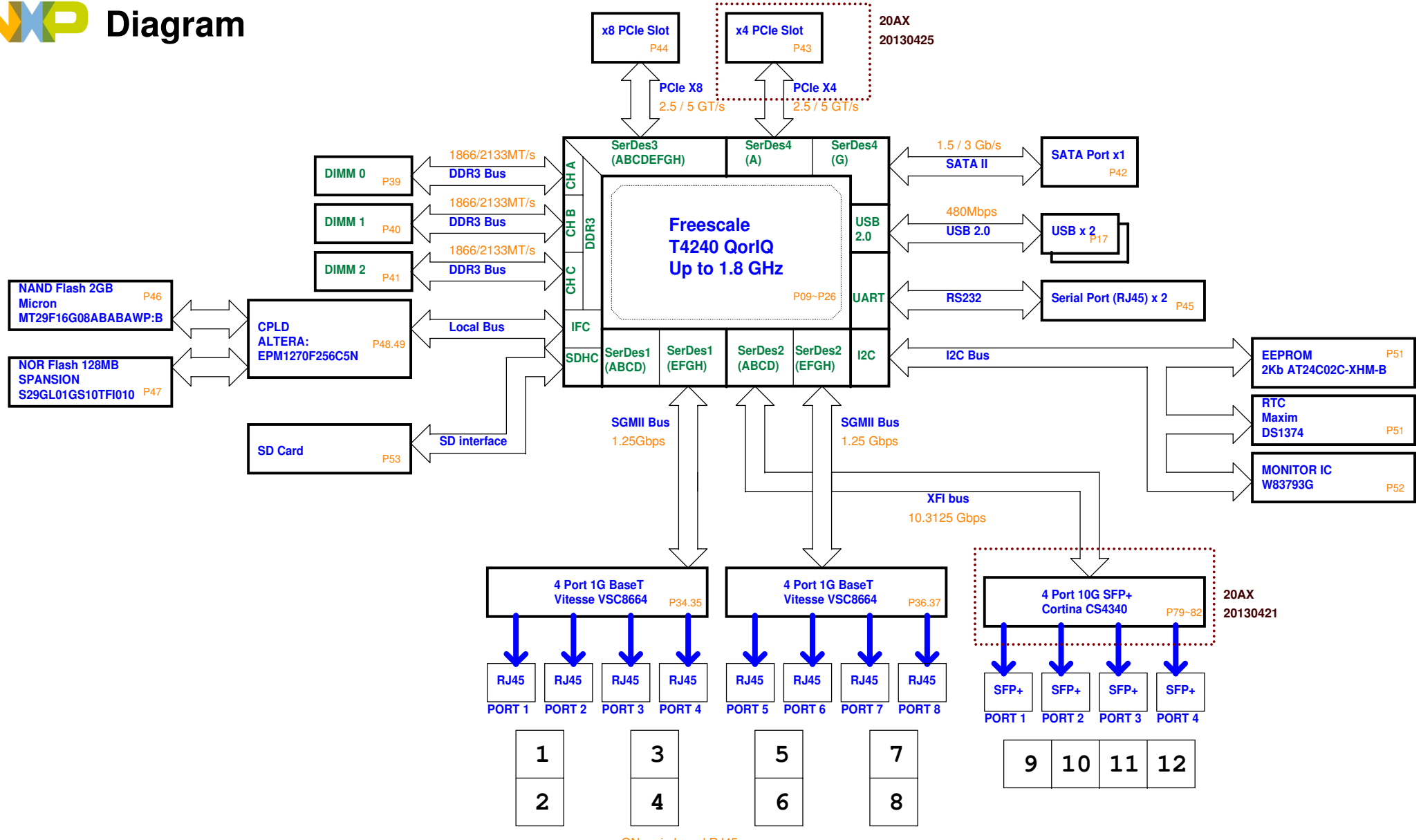
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 20130415 20130709  
 20130417 20130801  
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 This schematic is provided for reference purposes only.  
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ON main board RJ45

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power rails be applied in a specific sequence in order to ensure  
 i. For power up, these requirements are as follows:

- Bring up  $V_{DD}$ ,  $SnV_{DD}$ ,  $USB\_SV_{DD}$ ,  $FA\_VL$ ,  $V_{DD\_LP}$ ,  $USB\_HV_{DD}$ ,  $LV_{DD}$ ,  $DV_{DD}$ ,  $USB\_OV_{DD}$ ,  $OV_{DD}$ ,  $TH\_V_{DD}$ ,  $AV_{DD}$  (cores, platform, DDR),  $GnV_{DD}$ ,  $XnV_{DD}$ , and  $AV_{DD\_SDn\_PLLn}$ . Drive  $PROG\_SFP = GND$ .
  - $PORESET\_B$  input must be driven asserted and held during this step.

Items on the same line have no ordering requirement with respect to one another except for the USB power supplies per the following note.

**NOTE**

- $USB\_SV_{DD}$  supply must ramp before or after the  $USB\_HV_{DD}$  and  $USB\_OV_{DD}$  supplies have ramped. The supply set that ramp first must reach 90% of its final value before a supply from the other set can be ramped up.
- $USB\_HV_{DD}$  and  $USB\_OV_{DD}$  supplies among themselves are sequence independent.
- $USB\_HV_{DD}$  rise time (10% to 90%) has a minimum of 100 us.

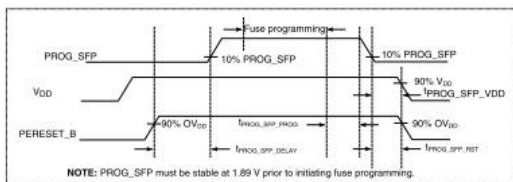
- Negate  $PORESET\_B$  input as long as the required assertion/hold time has been met per **Table 16**.

3. For secure boot fuse programming, use the following steps:

- After negation of  $PORESET\_B$ , drive  $PROG\_SFP = 1.89$  V after a required minimum delay per **Table 5**.
- After fuse programming is completed, it is required to return  $PROG\_SFP = GND$  before the system is power cycled ( $PORESET\_B$  assertion) or powered down ( $V_{DD}$  ramp down) per the required timing specified in **Table 5**. See **Security fuse processor**, for additional details.

All supplies must be at their stable values within 75 ms.

This figure provides the  $PROG\_SFP$  timing diagram.



**Figure 8. PROG\_SFP timing diagram**

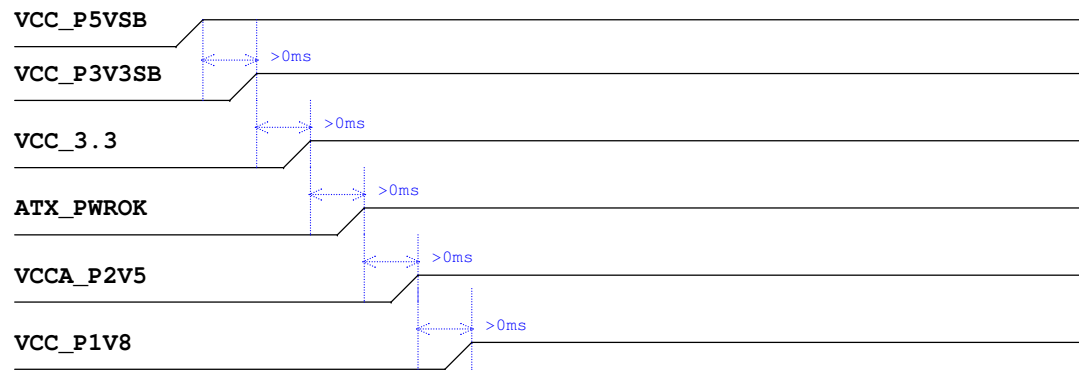
This table provides information on the power-down and power-up sequence parameters for  $PROG\_SFP$ .

**Table 5. PROG\_SFP timing<sup>5</sup>**

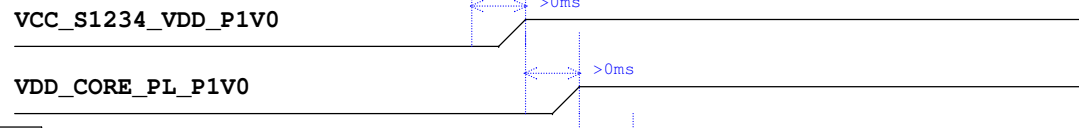
Driver type	Min	Max	Unit	Notes
tPROG_SFP_DELAY	100	-	SYSCLKs	1
tPROG_SFP_PROG	0	-	μs	2
tPROG_SFP_VDD	0	-	μs	3
tPROG_SFP_RST	0	-	μs	4

- Delay required from the deassertion of  $PORESET\_B$  to driving  $PROG\_SFP$  ramp up. Delay measured from  $PORESET\_B$  deassertion at 90%  $OV_{DD}$  to 10%  $PROG\_SFP$  ramp up.
- Delay required from fuse programming finished to  $PROG\_SFP$  ramp down start. Fuse programming must complete while  $PROG\_SFP$  is stable at 1.89 V. No activity other than that required for secure boot fuse programming is permitted while  $PROG\_SFP$  driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while  $PROG\_SFP = GND$ . After fuse programming is completed, it is required to return  $PROG\_SFP = GND$ .
- Delay required from  $PROG\_SFP$  ramp down complete to  $V_{DD}$  ramp down start.  $PROG\_SFP$  must be grounded to minimum 10%  $PROG\_SFP$  before  $V_{DD}$  is at 90%  $V_{DD}$ .
- Delay required from  $PROG\_SFP$  ramp down complete to  $PORESET\_B$  assertion.  $PROG\_SFP$  must be grounded to minimum 10%  $PROG\_SFP$  before  $PORESET\_B$  assertion reaches 90%  $OV_{DD}$ .
- Only two secure boot fuse programming events are permitted per lifetime of a device.

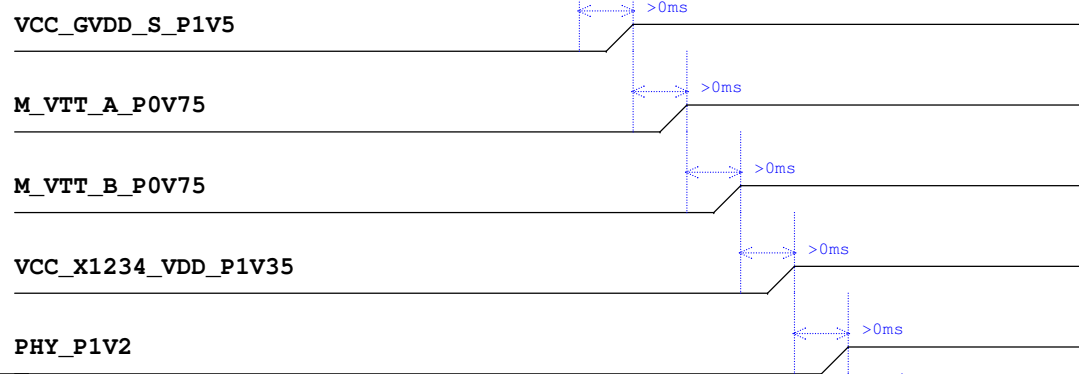
a.



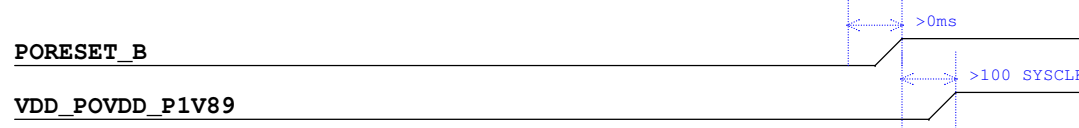
b.



c.



d.

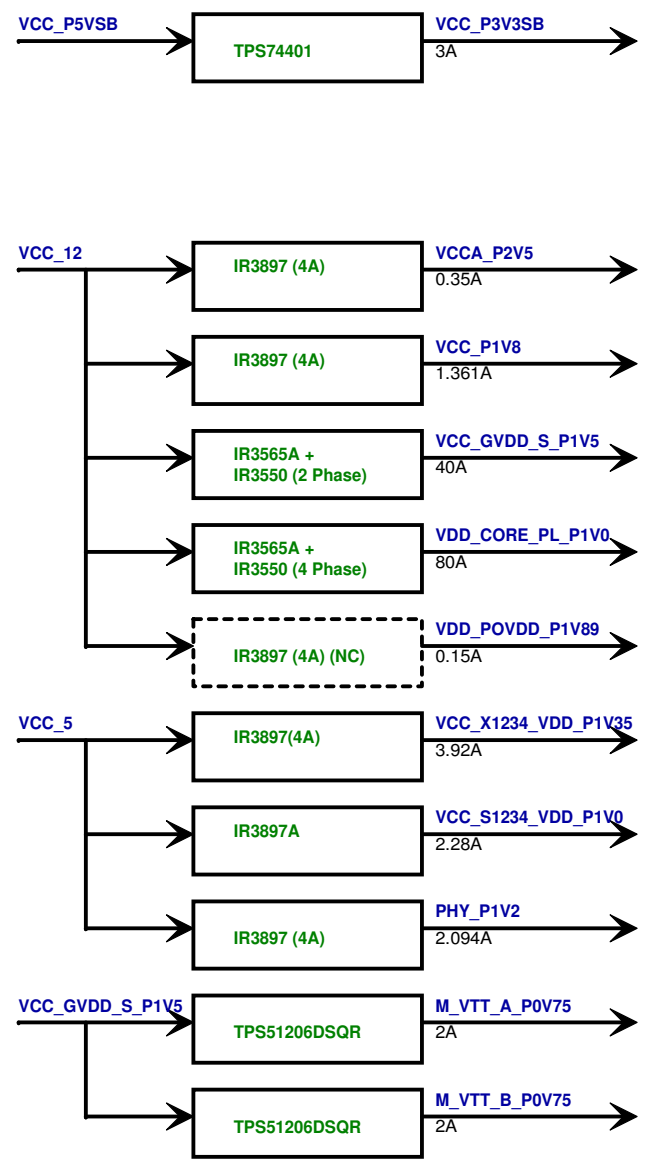


- IO rails up first like 3.3V, 2.5V, 1.8V etc.
- $V_{DD}$  ( $V_{Core}$ ),  $SV_{DD}$  (1st SERDES voltage) and all the derivatives of these voltages via filters.
- $GV_{DD}/V_{TT}/V_{ref}$  (DDR),  $XV_{DD}$  (2nd SERDES voltage).
- $PORESET\_B$ , drive  $PROG\_SFP = 1.89$  V

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		<b>Power Sequence</b>	
Title <b>Power Sequence</b>	Document Number <b>4BS05640C1X10</b>	Rev 30BX	
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# Power Delivery



VDD_CORE_PL_P1V0	80A	<b>CPU (T4240)</b>
VCC_GVDD_S_P1V5	40A (with DDR3)	1V VDD :80A
VCC_S1234_VDD	2.28A	1.5V GVDD :3.4A
VCC_X1234_VDD	3.6A	1V S[1:4]VDD :2.28A
VDD_OVDD_P1V8	0.6A	1.35V X[1:4]VDD :3.6A
VCC_DVDD	0.15A	1.8V OVDD :0.6A
		2.5V DVDD :0.15A
VCCA_P2V5	0.35A	2.5V LVDD :0.35A
VDD_USB12_VDD_3P3	0.35A	3.3V USB1/2_VDD_3P3 : 0.04A
VDD_USB12_VDD_1P0	0.04A	1.0V USB1/2_VDD_1P0 : 0.04A
VDD_USB12_VDD_1P8	0.04A	1.8V USB1/2_VDD_1P8 : 0.04A
P1V0	0.05A	1.0V FA_VDD : 0.05A
P1V0	From VDD core	1.0V VDD_LP : Derived from VDD core
P1V8_AVDD	0.05A	1.8V IRS_VDD : 0.05A
VDD_POVDD	0.15A	1.89V POVDD : 0.15A
M_VTT_A,M_VTT_B	4A (with DDR3)	0.75V MVREF :
AVDD_CGA1	0.003A	1.8V AVDD_CGA1(GroupA_PLL1) : 0.003A
AVDD_CGA2	0.003A	1.8V AVDD_CGA2(GroupA_PLL2) : 0.003A
AVDD_CGA3	0.003A	1.8V AVDD_CGA3(GroupA_PLL3) : 0.003A
AVDD_CGB1	0.003A	1.8V AVDD_CGB1(GroupB_PLL1) : 0.003A
AVDD_CGB2	0.003A	1.8V AVDD_CGB2(GroupB_PLL2) : 0.003A
AVDD_DDR1	0.003A	1.8V AVDD_DDR(DDR_PLL1) : 0.003A
AVDD_DDR2	0.003A	1.8V AVDD_DDR(DDR_PLL2) : 0.003A
AVDD_DDR3	0.003A	1.8V AVDD_DDR(DDR_PLL2) : 0.003A
AVDD_PLAT	0.003A	1.8V AVDD_PL(Platfrom_PLL) : 0.003A
AVDD_SRDS1_PLL1	0.04A	1.35V AVDD_SRDS1_PLL1 :0.04A
AVDD_SRDS1_PLL2	0.04A	1.35V AVDD_SRDS1_PLL2 :0.04A
AVDD_SRDS2_PLL1	0.04A	1.35V AVDD_SRDS2_PLL1 :0.04A
AVDD_SRDS2_PLL2	0.04A	1.35V AVDD_SRDS2_PLL2 :0.04A
AVDD_SRDS3_PLL1	0.04A	1.35V AVDD_SRDS3_PLL1 :0.04A
AVDD_SRDS3_PLL2	0.04A	1.35V AVDD_SRDS3_PLL2 :0.04A
AVDD_SRDS4_PLL1	0.04A	1.35V AVDD_SRDS4_PLL1 :0.04A
AVDD_SRDS4_PLL2	0.04A	1.35V AVDD_SRDS4_PLL2 :0.04A
VCC_GVDD_S_P1V5	40A (with T4240)	<b>DDR3 LONG-DIMM *3</b>
M_VTT_A,M_VTT_B	4A (with T4240)	1.5V VDD
		0.75V VTT
VCC_3.3	0.035A	<b>MT29F16G08ABDDAH4</b>
		3.3V : 0.035A
VCC_3.3	0.1A	<b>S29GL01GS11TFI010</b>
		3.3V : 0.1A

VCCA_P2V5	0.334A	<b>VSC8664*2</b>
VCC_3.3	0.92A	2.5V VDDIO:0.334A
P1V2	1.548A	3.3V VDD33A:0.92A
P1V2	0.546A	1.2V VDD12:1.548A
		1.2V VDD12A:0.546A
VCC_3.3	0.065A	<b>ICS8535AGI-31LF</b>
		3.3V : 0.065A
VCC_3.3	0.197A	<b>840NT4NLGI</b>
		3.3V : 0.197A
VCC_3.3	0.333A	<b>8T49N222B-101NLG</b>
		3.3V : 0.333A
VCC_3.3	0.027A	<b>ICS85108AGILF</b>
		3.3V : 0.027A
VCC_3.3	0.159A	<b>840NT4-01NLGI</b>
		3.3V : 0.159A

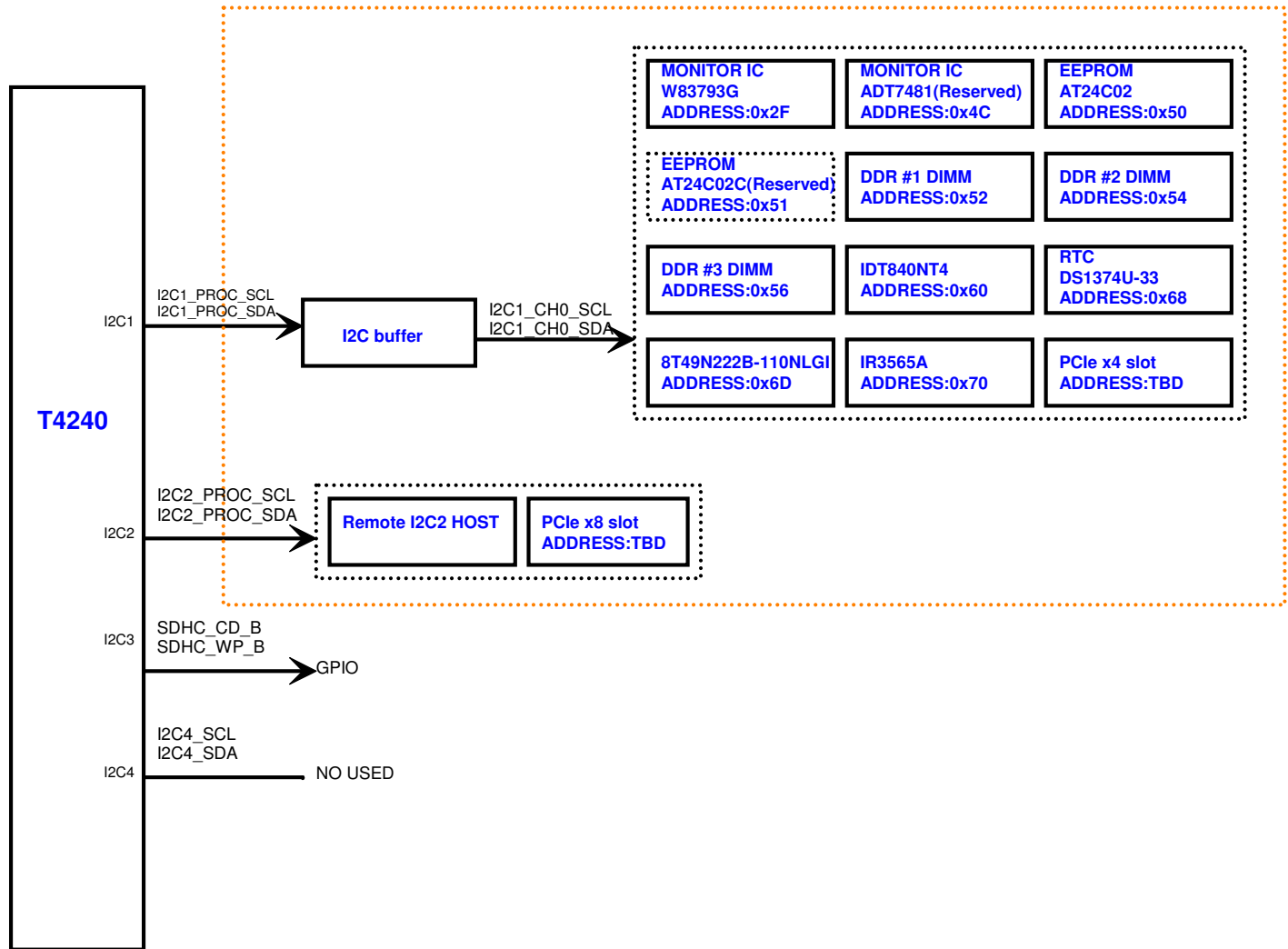
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**Power Delivery**

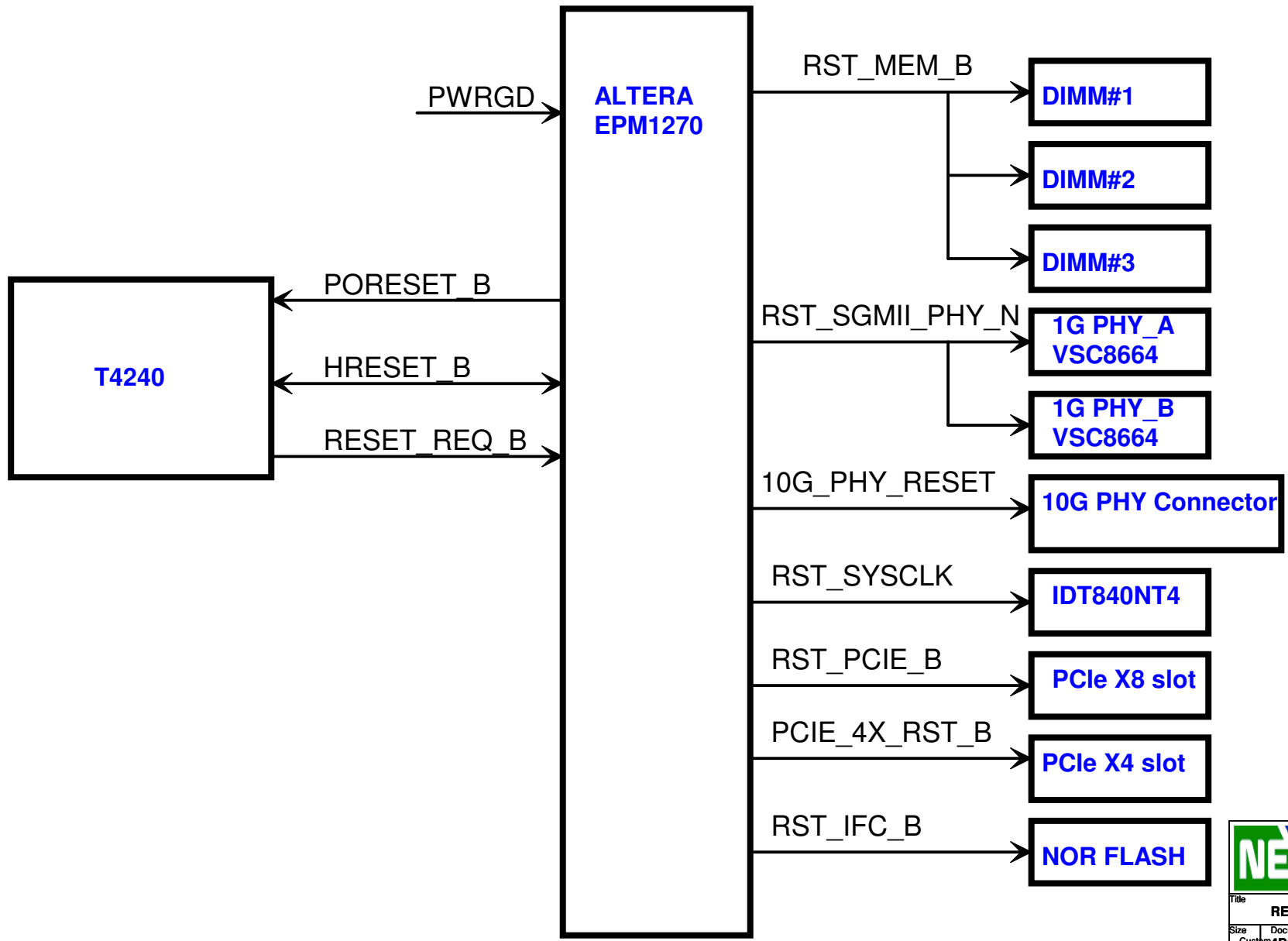
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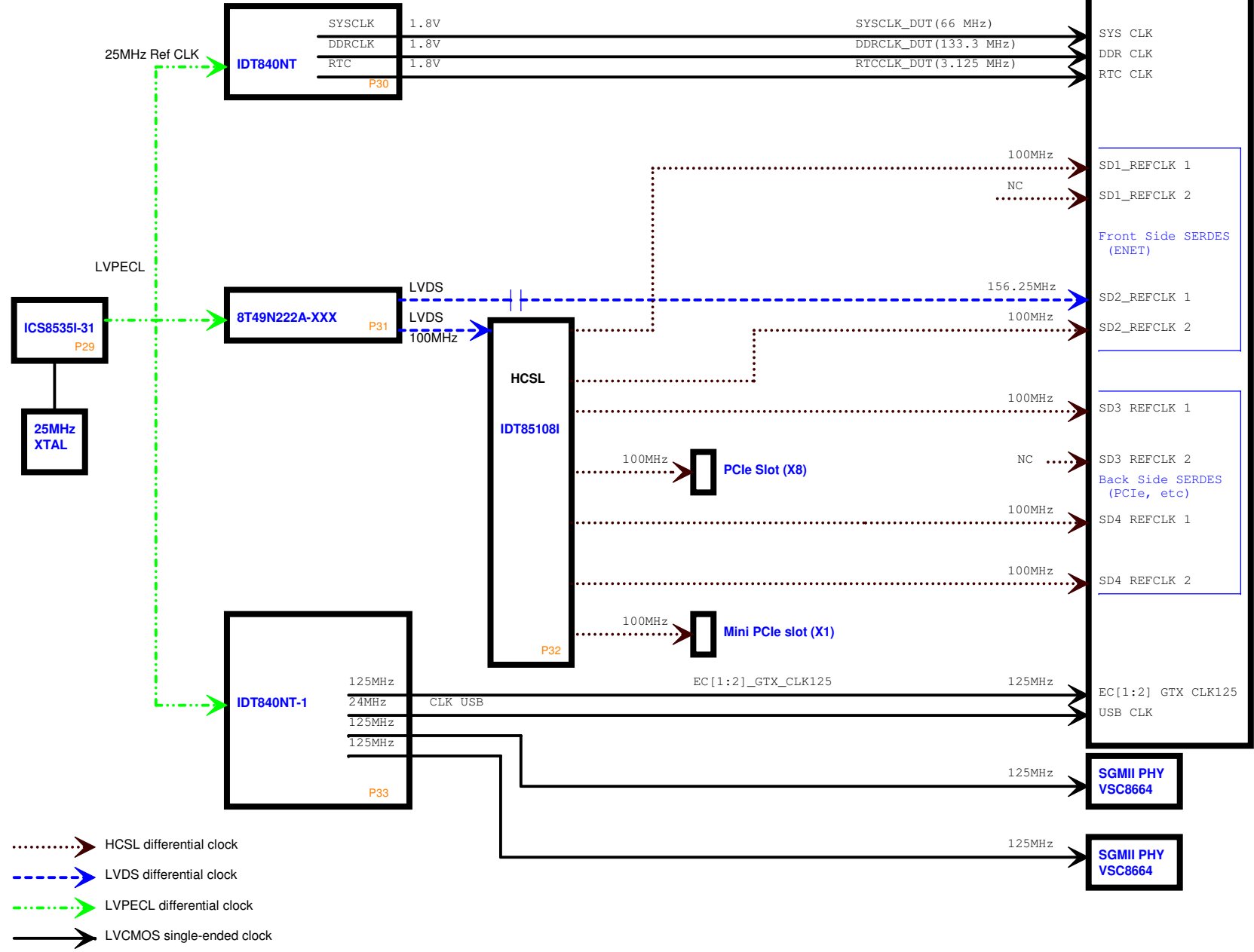
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# T4240



SD1 : 4x SGMII  
 SRDS\_PRTCL\_S1:28  
 cfg\_srds1\_prtcl :28  
 SD1\_REFCLK1:100 MHz  
 SD1\_REFCLK2:X

SD2 : 4x XFI + 4x SGMII  
 SRDS\_PRTCL\_S2:56  
 cfg\_srds2\_prtcl:56  
 SD2\_REFCLK1:156.25 MHz  
 SD2\_REFCLK2:100 MHz

SD3 : PCIe slot X8  
 SRDS\_PRTCL\_S3: 2  
 cfg\_srds3\_prtcl : 66  
 SD3\_REFCLK1:100 MHz  
 SD3\_REFCLK2:X

SD4 : miniPCIe slot X1  
 SATAII \*1  
 SRDS\_PRTCL\_S4:10  
 cfg\_srds4\_prtcl:86  
 SD4\_REFCLK1:100 MHz  
 SD4\_REFCLK2:100 MHz

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	<b>Title</b> <b>Clock map</b>	

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<b>Memory sub system</b>	
DDR3	DDR3 2.1GHz Slot X 3 UDIMM/RDIMM
NOR flash	128MB, 16-bit width
NAND flash	2GB, 8-bit width,Page size(2048 + 64 bytes)
SATA	SATA II CONNECTOR X1
SD	SD Card socket X 1
Serial Proms	NO
eMMC	NO

<b>Networking sub system</b>	
10G PHY	4 PORT SFP+
1G PHY	SGMII,Vitesse VSC8664 * 2

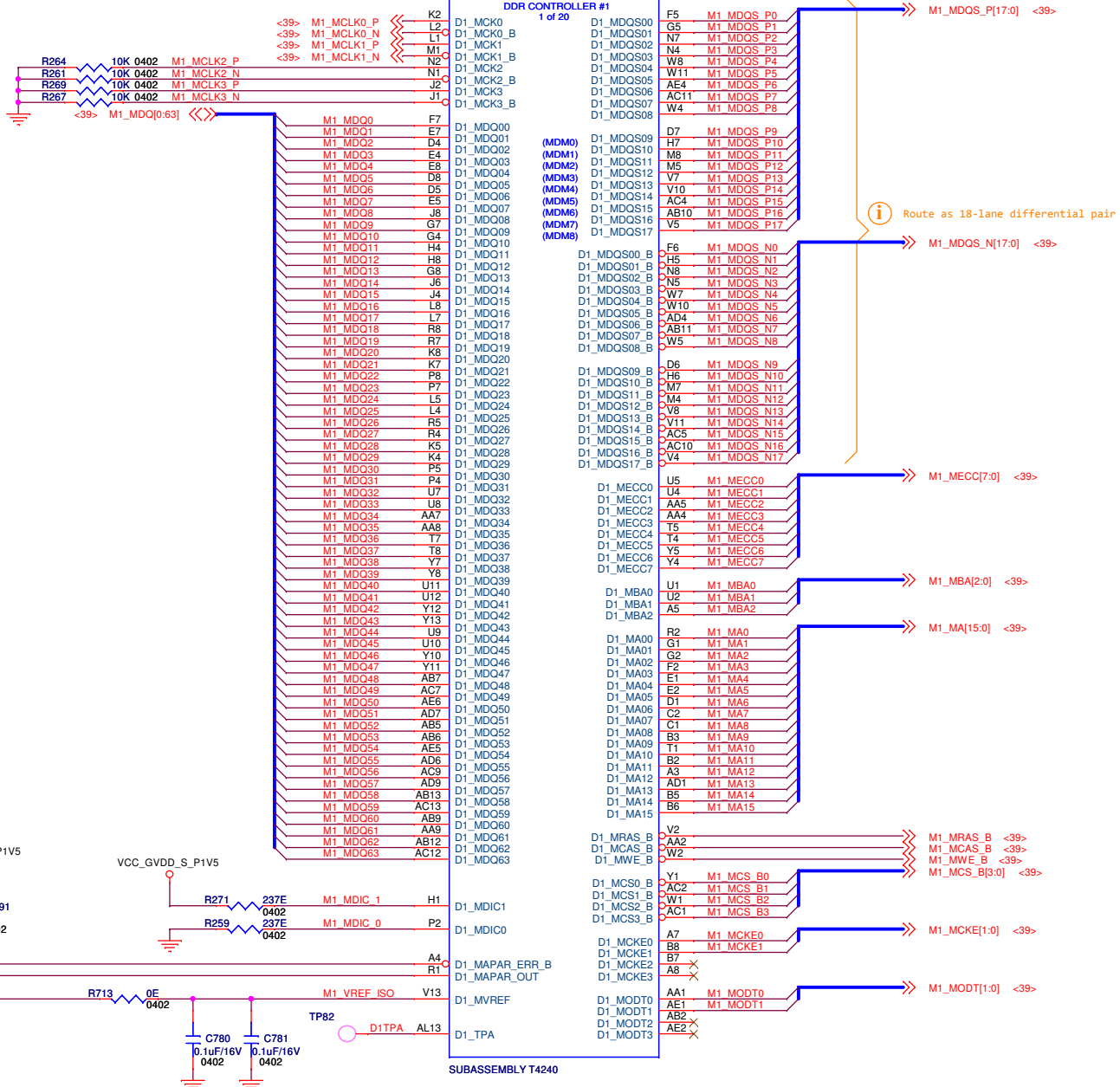
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<b>Title</b> Mem & Net sub system		
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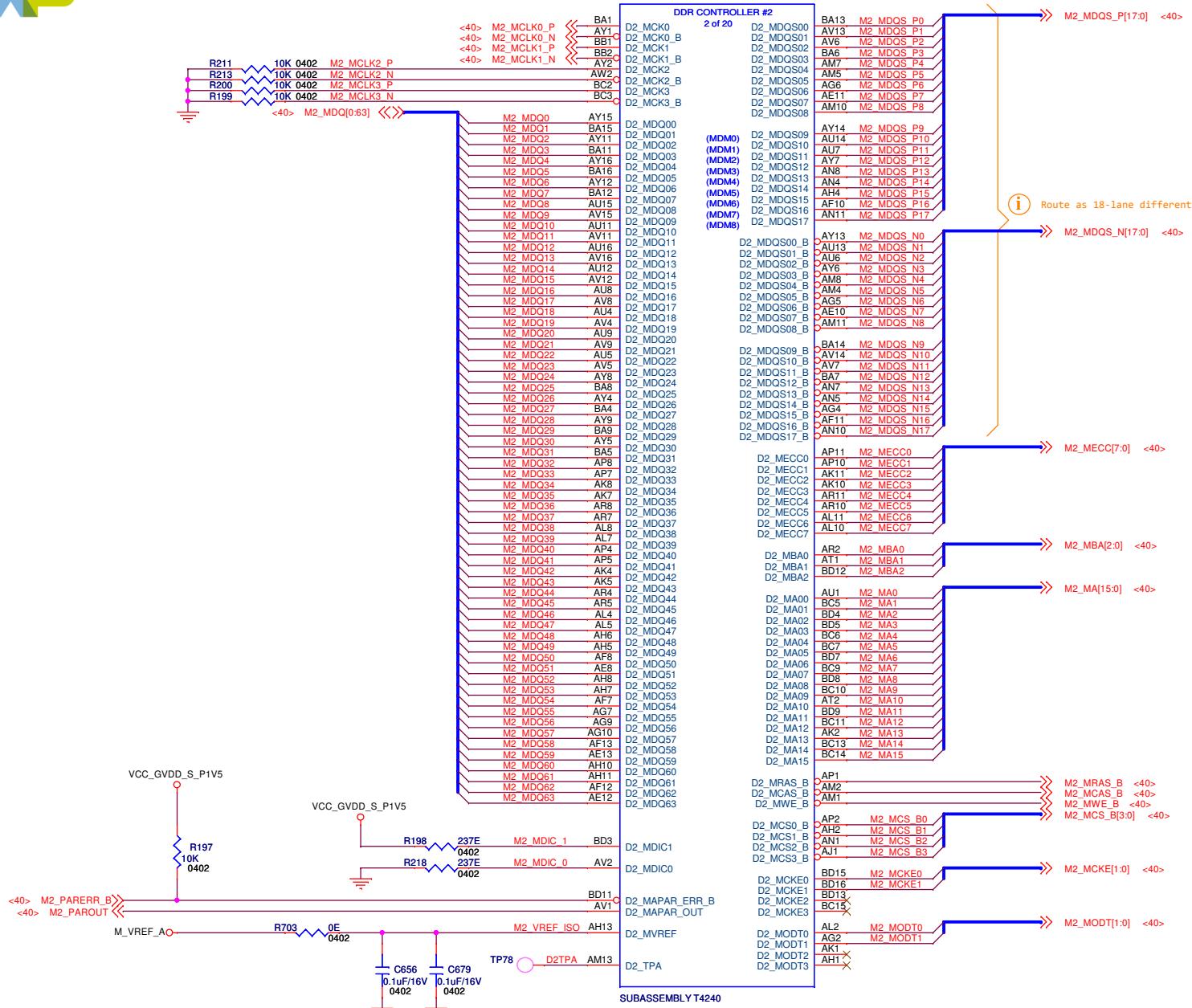
Route as 18-lane differential pair

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<b>T4240 DDR Controller #1</b>		
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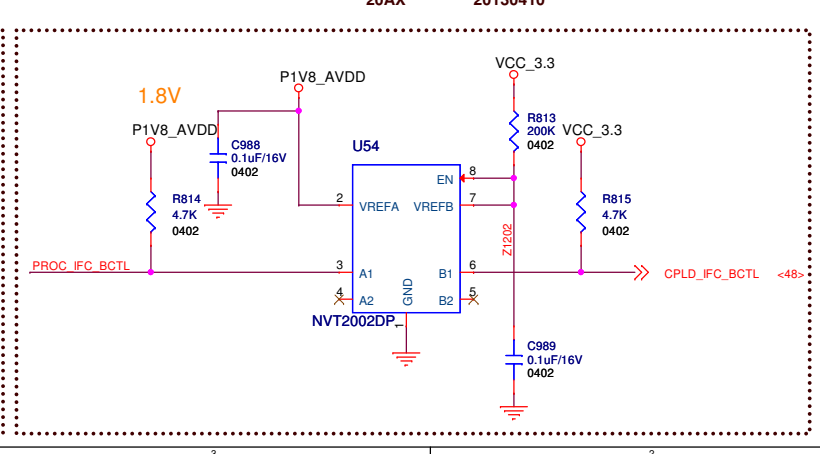
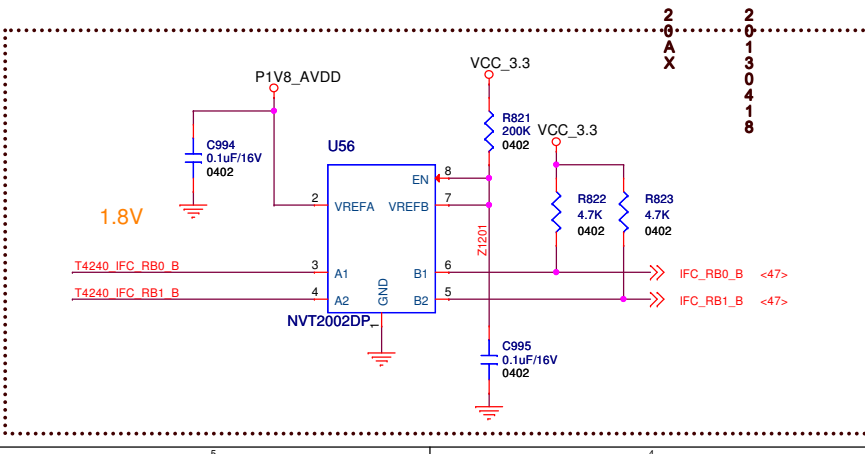
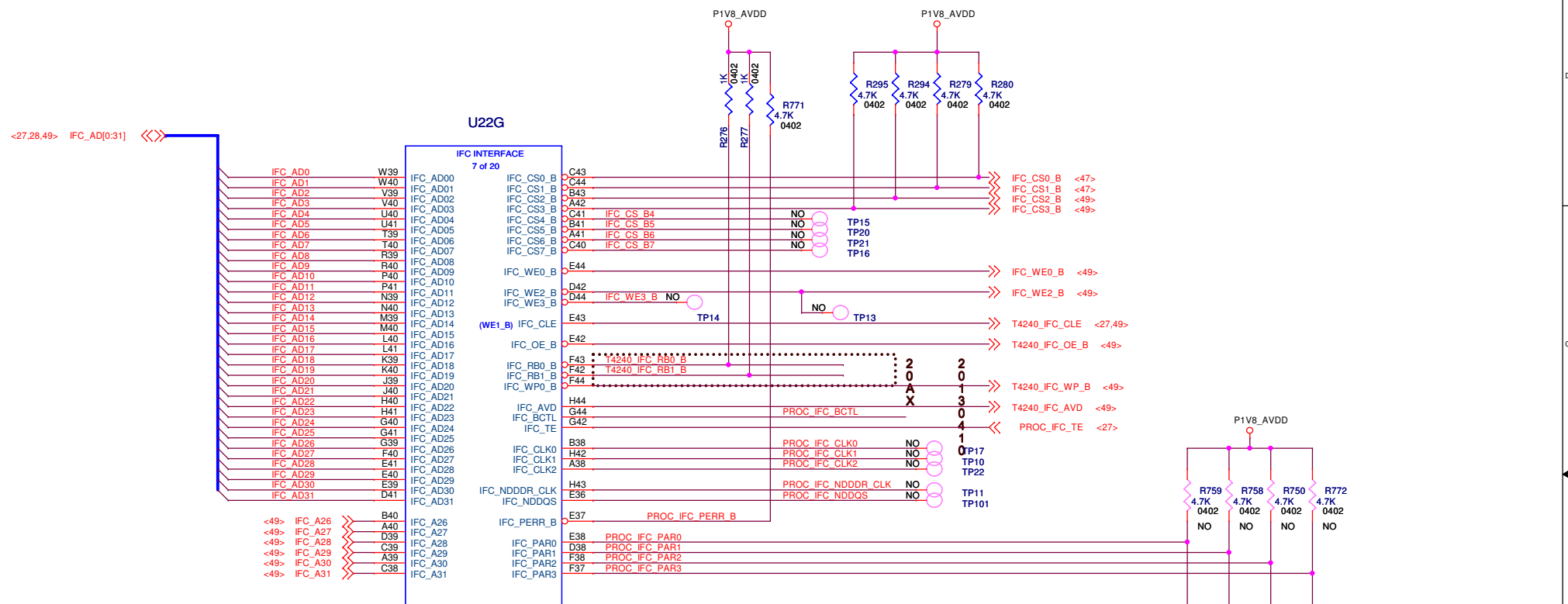


Route as 18-lane differential pair

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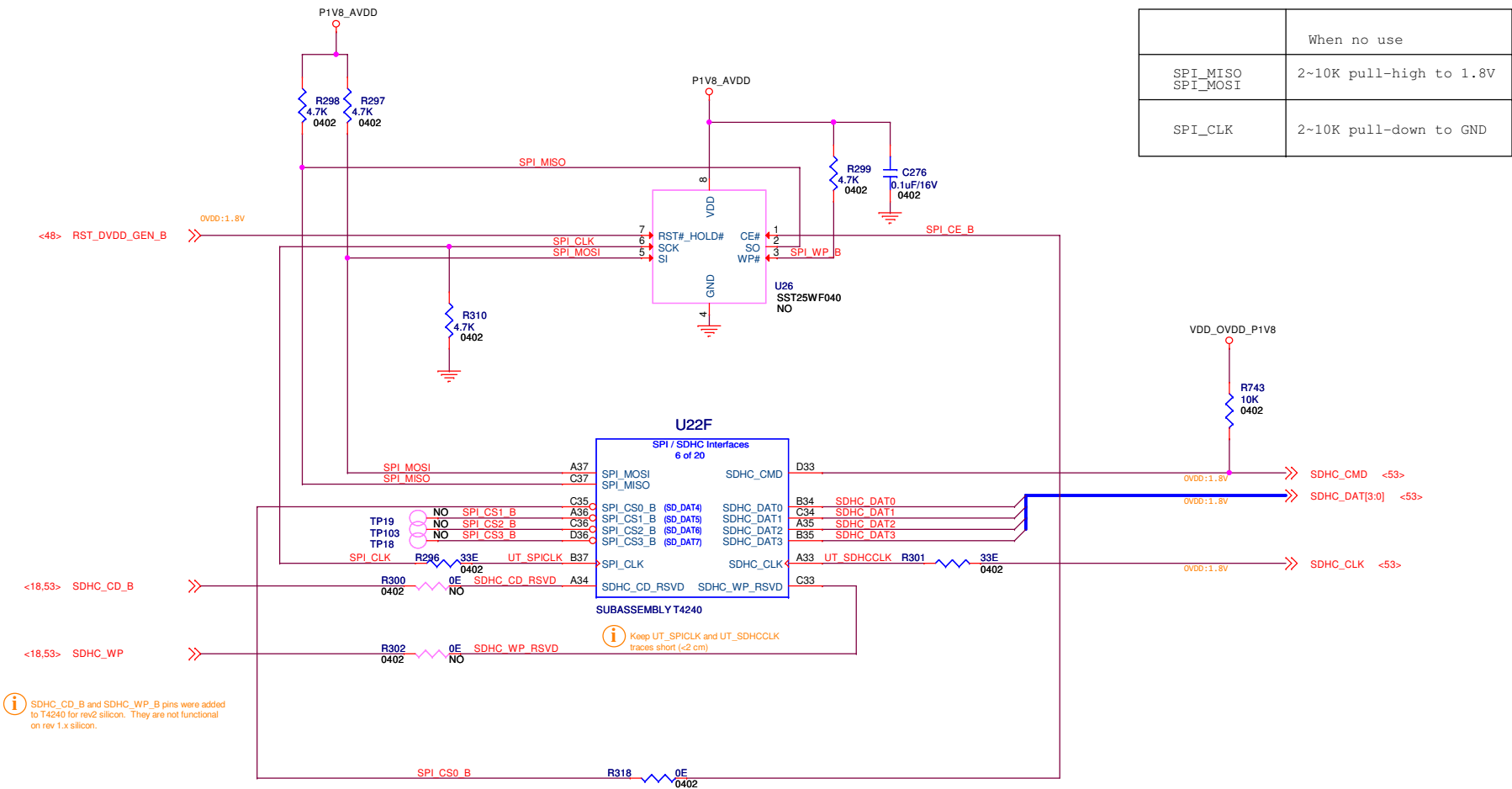
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Size	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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Title <b>T4240 Local Bus Block</b>		
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	When no use
SPI_MISO SPI_MOSI	2~10K pull-high to 1.8V
SPI_CLK	2~10K pull-down to GND

**i** SDHC\_CD\_B and SDHC\_WP\_B pins were added to T4240 for rev2 silicon. They are not functional on rev 1.x silicon.

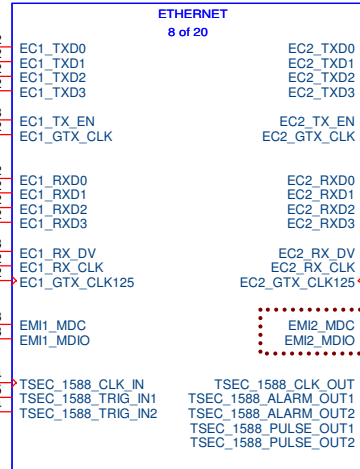
**i** Keep UT\_SPICLK and UT\_SDHCCLK traces short (<2 cm)

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		<b>Title</b> <b>T4240 SPI / SDHC Port</b>	
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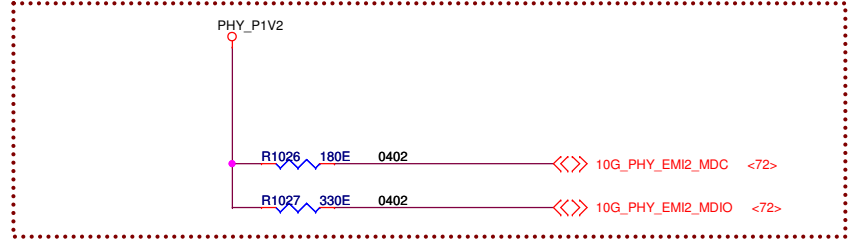
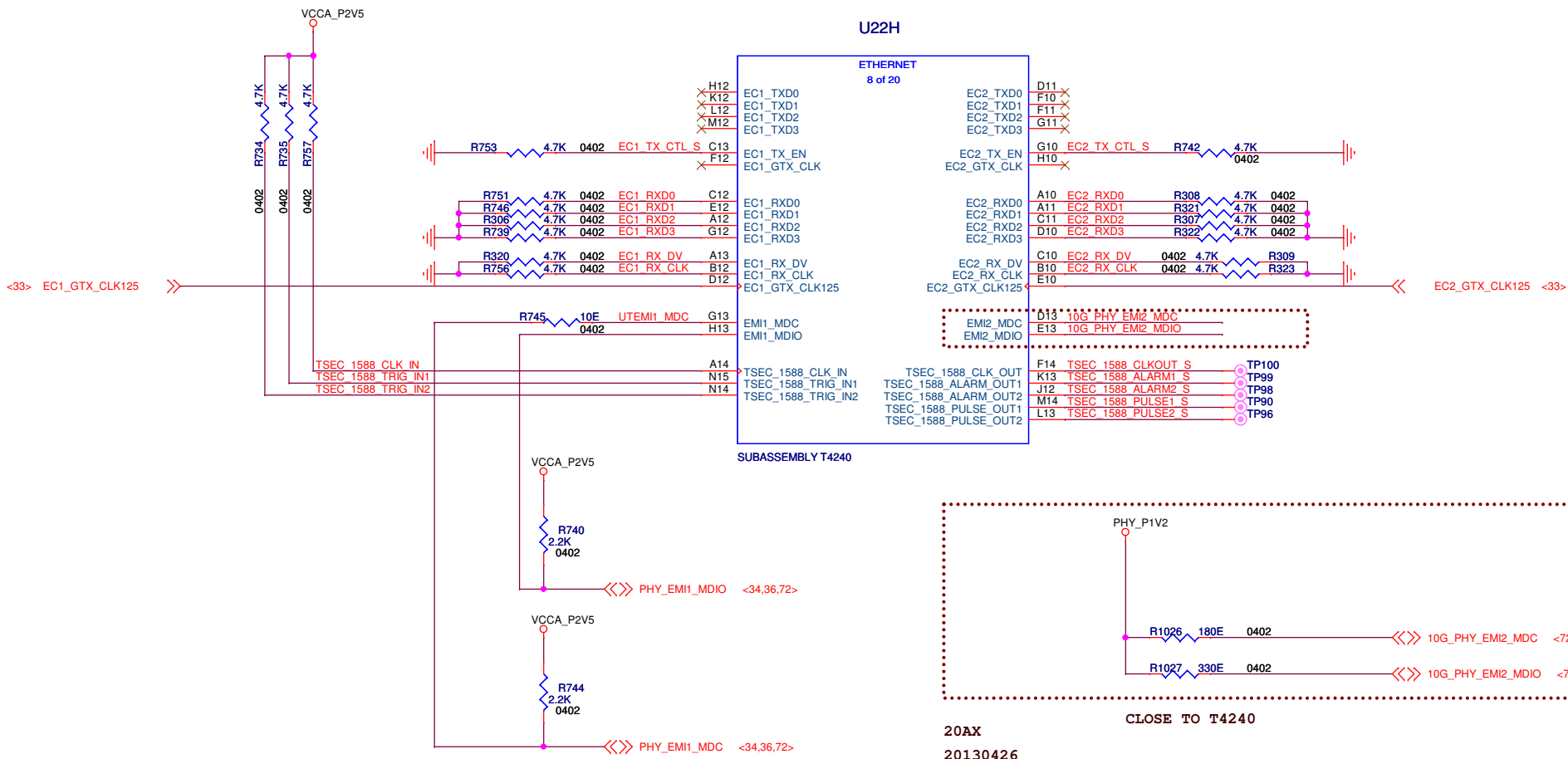


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SUBASSEMBLY T4240



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CLOSE TO T4240

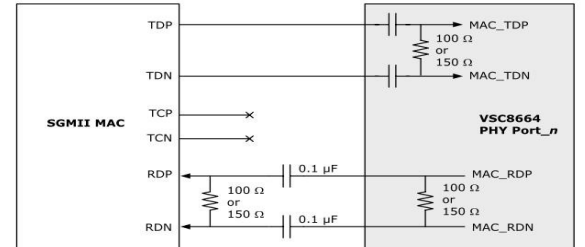
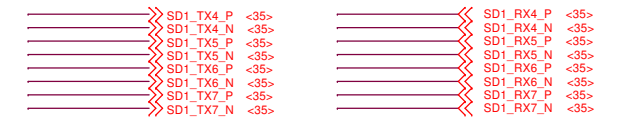
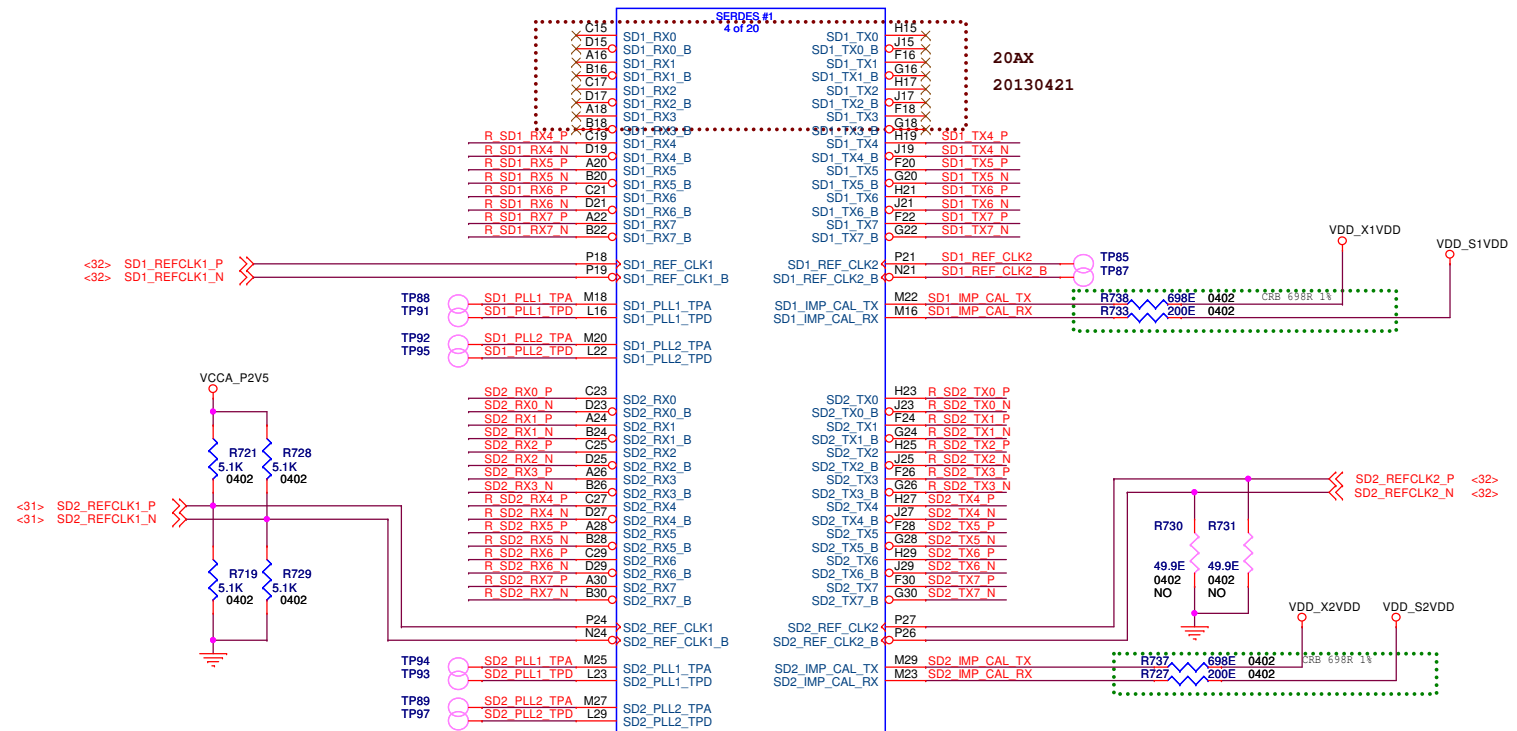
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Title <b>T4240 Ethernet Block + EMI</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
Date:	Friday, August 16, 2013	Sheet 14 of 86



# FRONT SIDE SERDES 1 & 2 (ENET)

U22D



**Coupling for SD2 Transmit line**

HOST=T4240	DEVICE=CS4340			
R SD2 TX0 P	C231	0.1uF/16V	0402	SD2 TX0 P
R SD2 TX0 N	C230	0.1uF/16V	0402	SD2 TX0 N
R SD2 TX1 P	C229	0.1uF/16V	0402	SD2 TX1 P
R SD2 TX1 N	C228	0.1uF/16V	0402	SD2 TX1 N
R SD2 TX2 P	C227	0.1uF/16V	0402	SD2 TX2 P
R SD2 TX2 N	C226	0.1uF/16V	0402	SD2 TX2 N
R SD2 TX3 P	C225	0.1uF/16V	0402	SD2 TX3 P
R SD2 TX3 N	C224	0.1uF/16V	0402	SD2 TX3 N

HOST=T4240	DEVICE=VSC8664								
R SD2 RX4 P	R536	100E	0402	NO	R SD2 RX4 P	C452	0.1uF/16V	0402	SD2 RX4 P
R SD2 RX4 N	R537	100E	0402	NO	R SD2 RX4 N	C451	0.1uF/16V	0402	SD2 RX4 N
R SD2 RX5 P	R538	100E	0402	NO	R SD2 RX5 P	C454	0.1uF/16V	0402	SD2 RX5 P
R SD2 RX5 N	R539	100E	0402	NO	R SD2 RX5 N	C453	0.1uF/16V	0402	SD2 RX5 N
R SD2 RX6 P	R539	100E	0402	NO	R SD2 RX6 P	C455	0.1uF/16V	0402	SD2 RX6 P
R SD2 RX6 N	R539	100E	0402	NO	R SD2 RX6 N	C456	0.1uF/16V	0402	SD2 RX6 N
R SD2 RX7 P	R539	100E	0402	NO	R SD2 RX7 P	C458	0.1uF/16V	0402	SD2 RX7 P
R SD2 RX7 N	R539	100E	0402	NO	R SD2 RX7 N	C457	0.1uF/16V	0402	SD2 RX7 N

HOST=T4240	DEVICE=VSC8664								
R SD1 RX4 P	R532	100E	0402	NO	R SD1 RX4 P	C444	0.1uF/16V	0402	SD1 RX4 P
R SD1 RX4 N	R533	100E	0402	NO	R SD1 RX4 N	C443	0.1uF/16V	0402	SD1 RX4 N
R SD1 RX5 P	R533	100E	0402	NO	R SD1 RX5 P	C446	0.1uF/16V	0402	SD1 RX5 P
R SD1 RX5 N	R534	100E	0402	NO	R SD1 RX5 N	C445	0.1uF/16V	0402	SD1 RX5 N
R SD1 RX6 P	R534	100E	0402	NO	R SD1 RX6 P	C447	0.1uF/16V	0402	SD1 RX6 P
R SD1 RX6 N	R535	100E	0402	NO	R SD1 RX6 N	C448	0.1uF/16V	0402	SD1 RX6 N
R SD1 RX7 P	R535	100E	0402	NO	R SD1 RX7 P	C450	0.1uF/16V	0402	SD1 RX7 P
R SD1 RX7 N	R535	100E	0402	NO	R SD1 RX7 N	C449	0.1uF/16V	0402	SD1 RX7 N

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Title		
T4240 SerDes 1 & 2		
Size	Document Number	Rev
Customer	4BS05640C1X10	30BX
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# BACK SIDE SERDES 3 & 4 (PCIe / SATA)

U22E

SERDES #2 5 of 20		SERDES #2 5 of 20	
SD3_RX0_P	BB18	SD3_RX0	AU18
SD3_RX0_N	BA18	SD3_RX0_B	AT18
SD3_RX1_P	BD19	SD3_RX1	AW19
SD3_RX1_N	BC19	SD3_RX1_B	AV19
SD3_RX2_P	BE20	SD3_RX2	AU20
SD3_RX2_N	BA20	SD3_RX2_B	AT20
SD3_RX3_P	BD21	SD3_RX3	AW21
SD3_RX3_N	BC21	SD3_RX3_B	AV21
SD3_RX4_P	BE22	SD3_RX4	AU22
SD3_RX4_N	BA22	SD3_RX4_B	AT22
SD3_RX5_P	BD23	SD3_RX5	AW23
SD3_RX5_N	BC23	SD3_RX5_B	AV23
SD3_RX6_P	BE24	SD3_RX6	AU24
SD3_RX6_N	BA24	SD3_RX6_B	AT24
SD3_RX7_P	BD25	SD3_RX7	AW25
SD3_RX7_N	BC25	SD3_RX7_B	AV25

<32> SD3\_REFCLK1\_P  
<32> SD3\_REFCLK1\_N

AL21	SD3_REF_CLK1	AL24	SD3_REFCLK2_P
AL22	SD3_REF_CLK1_B	AM24	SD3_REFCLK2_N
AN21	SD3_PLL1_TPA	AN25	SD3_IMP_CAL_TX
AP19	SD3_PLL1_TPD	AN19	SD3_IMP_CAL_RX
AN23	SD3_PLL2_TPA		
AP25	SD3_PLL2_TPD		

PCIE X4

SD4_RX0_P	BB26	SD4_RX0	AU26
SD4_RX0_N	BA26	SD4_RX0_B	AT26
SD4_RX1_P	BD27	SD4_RX1	AW27
SD4_RX1_N	BC27	SD4_RX1_B	AV27
SD4_RX2_P	BE28	SD4_RX2	AU28
SD4_RX2_N	BA28	SD4_RX2_B	AT28
SD4_RX3_P	BD29	SD4_RX3	AW29
SD4_RX3_N	BC29	SD4_RX3_B	AV29
SD4_RX4_P	BE30	SD4_RX4	AU30
SD4_RX4_N	BA30	SD4_RX4_B	AT30
SD4_RX5_P	BD31	SD4_RX5	AW31
SD4_RX5_N	BC31	SD4_RX5_B	AV31
SD4_RX6_P	BE32	SD4_RX6	AU32
SD4_RX6_N	BA32	SD4_RX6_B	AT32
SD4_RX7_P	BD33	SD4_RX7	AW33
SD4_RX7_N	BC33	SD4_RX7_B	AV33

SATA

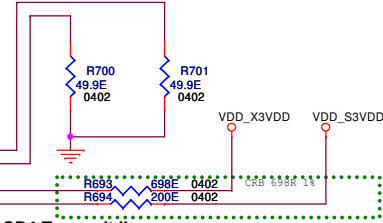
SATA

<32> SD4\_REFCLK1\_P  
<32> SD4\_REFCLK1\_N

AL27	SD4_REF_CLK1	AL29	SD4_REFCLK2_P
AM27	SD4_REF_CLK1_B	AL29	SD4_REFCLK2_N
AN28	SD4_PLL1_TPA	AN32	SD4_IMP_CAL_TX
AP26	SD4_PLL1_TPD	AN26	SD4_IMP_CAL_RX
AN30	SD4_PLL2_TPA		
AP32	SD4_PLL2_TPD		

SUBASSEMBLY T4240

### Coupling for SD4 Transmit line



### Coupling for SD3 Transmit line

SD3_TX0_P	C76	0.1uF/16V	0402	SD3_TXC0_P
SD3_TX0_N	C78	0.1uF/16V	0402	SD3_TXC0_N
SD3_TX1_P	C79	0.1uF/16V	0402	SD3_TXC1_P
SD3_TX1_N	C80	0.1uF/16V	0402	SD3_TXC1_N
SD3_TX2_P	C81	0.1uF/16V	0402	SD3_TXC2_P
SD3_TX2_N	C82	0.1uF/16V	0402	SD3_TXC2_N
SD3_TX3_P	C88	0.1uF/16V	0402	SD3_TXC3_P
SD3_TX3_N	C90	0.1uF/16V	0402	SD3_TXC3_N
SD3_TX4_P	C95	0.1uF/16V	0402	SD3_TXC4_P
SD3_TX4_N	C96	0.1uF/16V	0402	SD3_TXC4_N
SD3_TX5_P	C103	0.1uF/16V	0402	SD3_TXC5_P
SD3_TX5_N	C108	0.1uF/16V	0402	SD3_TXC5_N
SD3_TX6_P	C118	0.1uF/16V	0402	SD3_TXC6_P
SD3_TX6_N	C126	0.1uF/16V	0402	SD3_TXC6_N
SD3_TX7_P	C147	0.1uF/16V	0402	SD3_TXC7_P
SD3_TX7_N	C149	0.1uF/16V	0402	SD3_TXC7_N

SD3_TXC0_P	<44>
SD3_TXC0_N	<44>
SD3_TXC1_P	<44>
SD3_TXC1_N	<44>
SD3_TXC2_P	<44>
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SD3_TXC3_P	<44>
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SD3_TXC7_N	<44>

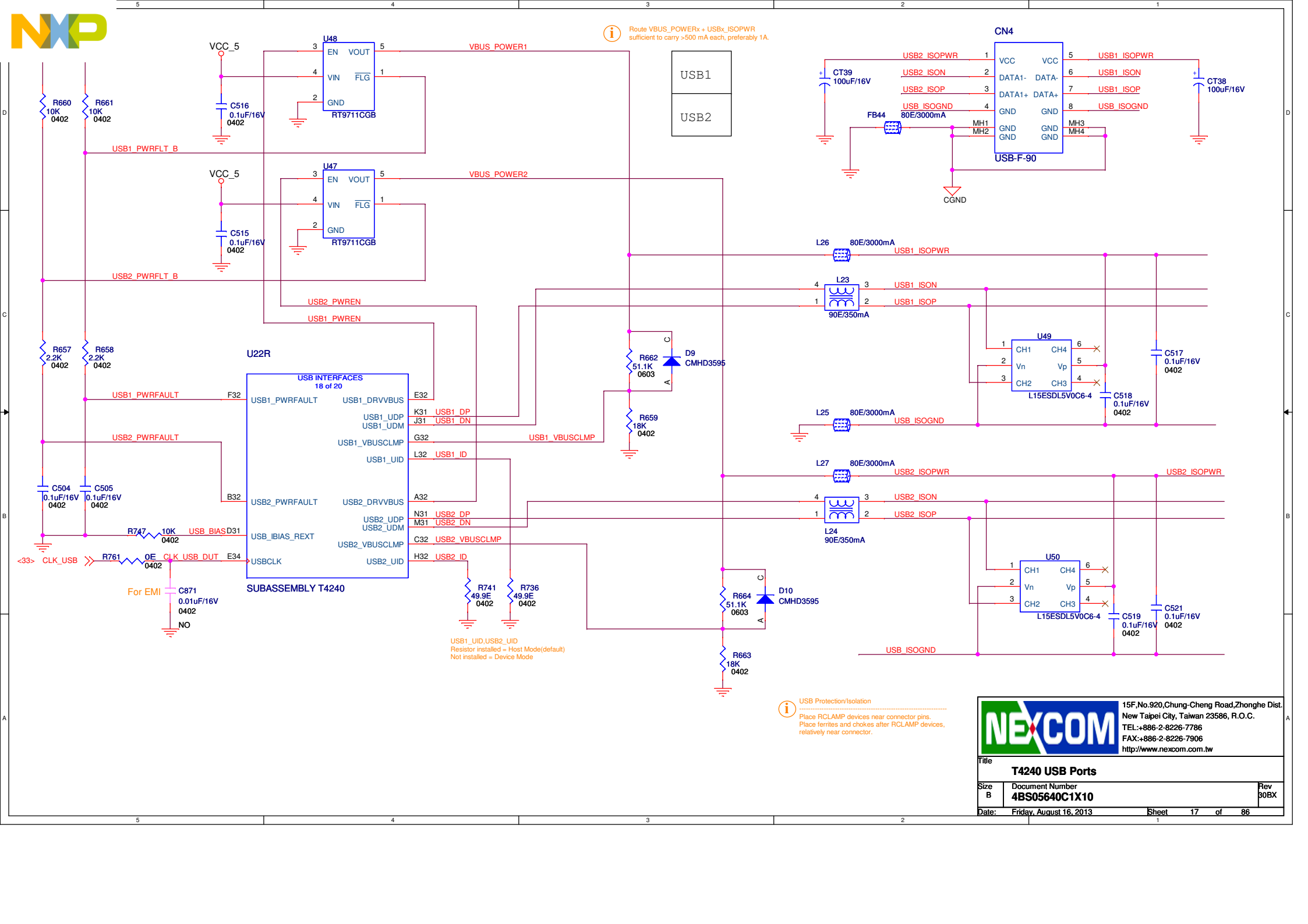
20AX  
20130421

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SD3_RX0_N	<44>
SD3_RX1_P	<44>
SD3_RX1_N	<44>
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SD3_RX4_N	<44>
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SD3_RX5_N	<44>
SD3_RX6_P	<44>
SD3_RX6_N	<44>
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SD3_RX7_N	<44>

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Title <b>T4240 SerDes 3 &amp; 4</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
Date:	Friday, August 16, 2013	Sheet 16 of 86



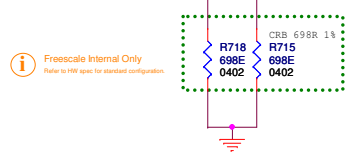
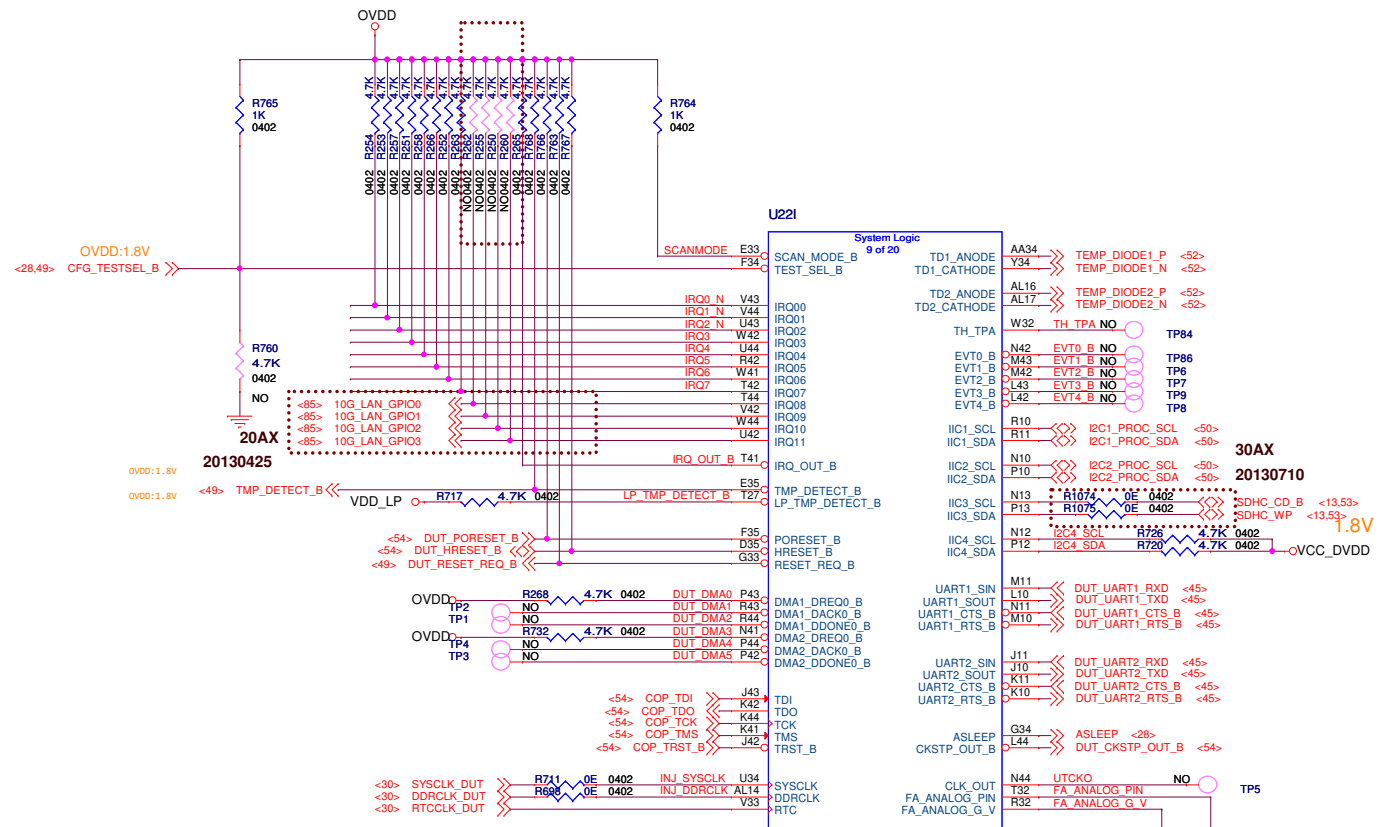
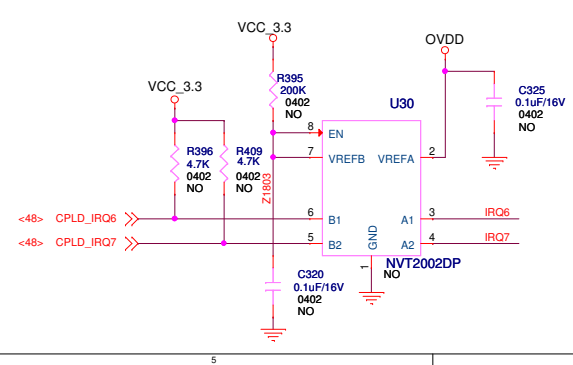
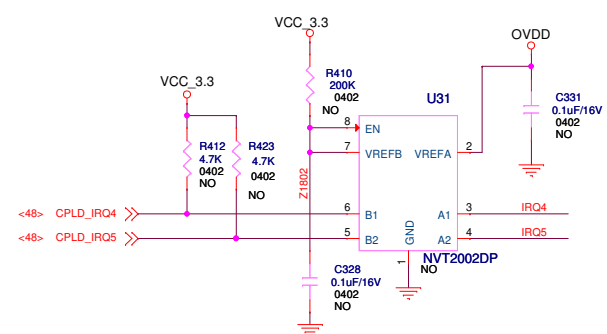
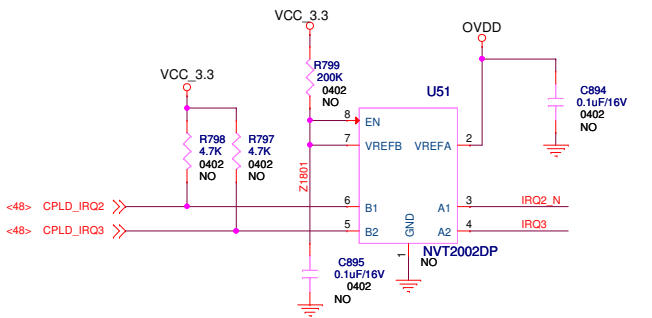
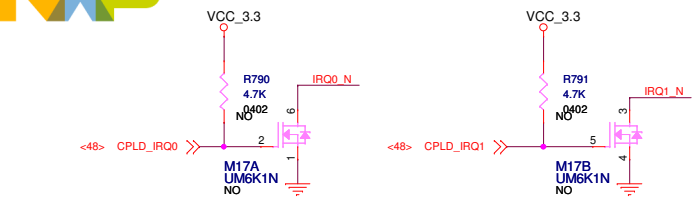


Route VBUS\_POWERx + USBx\_ISOPWR sufficient to carry >500 mA each, preferably 1A.

USB Protection/Isolation  
Place RCLAMP devices near connector pins.  
Place ferrites and chokes after RCLAMP devices, relatively near connector.

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Title <b>T4240 USB Ports</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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Title			T4240 System Block		
Size	Document Number		Rev		
Customer	4BS05640C1X10		808X		
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U22T

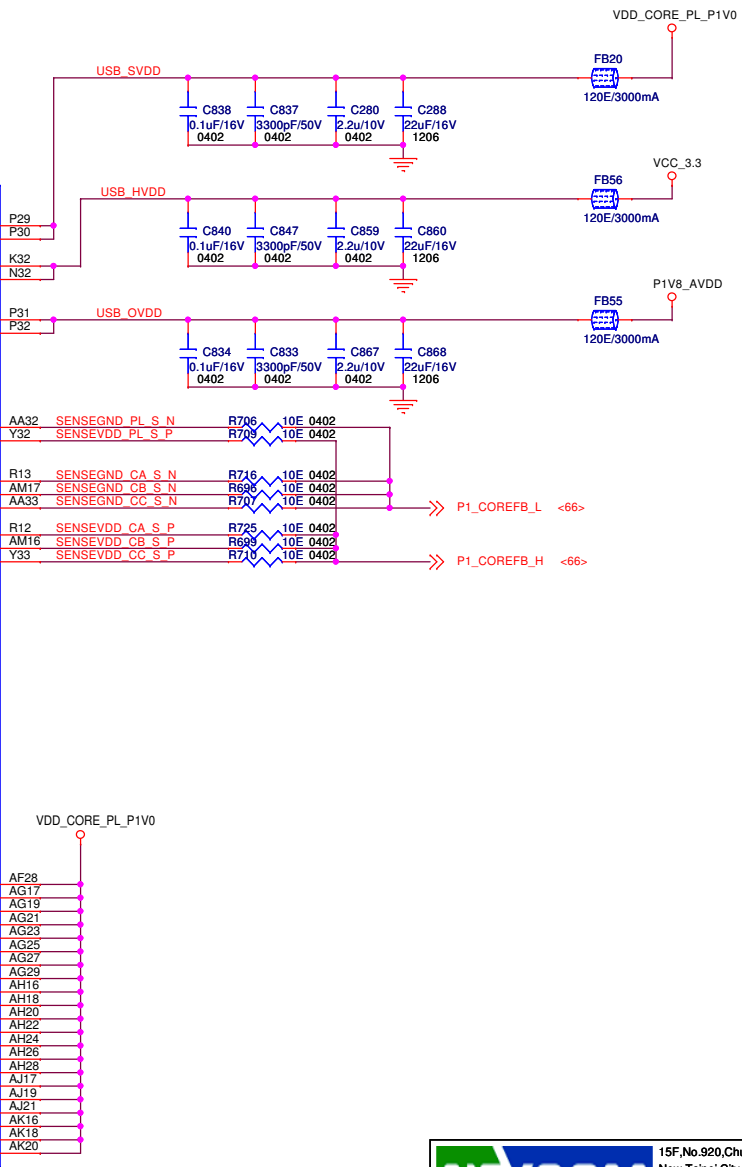
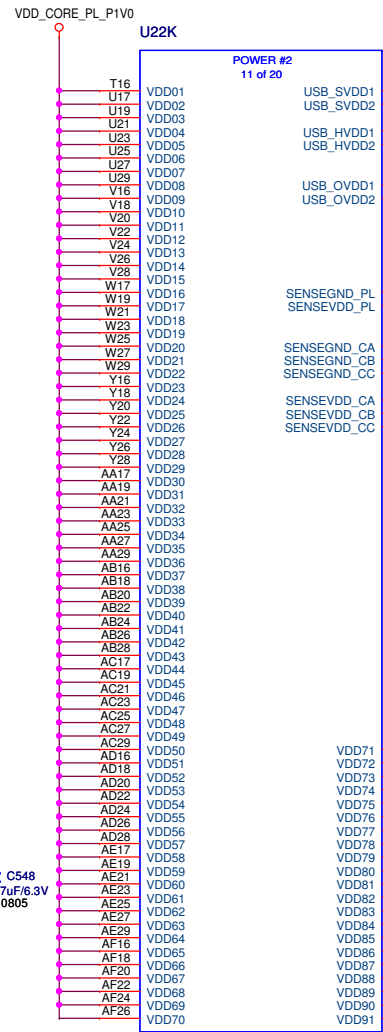
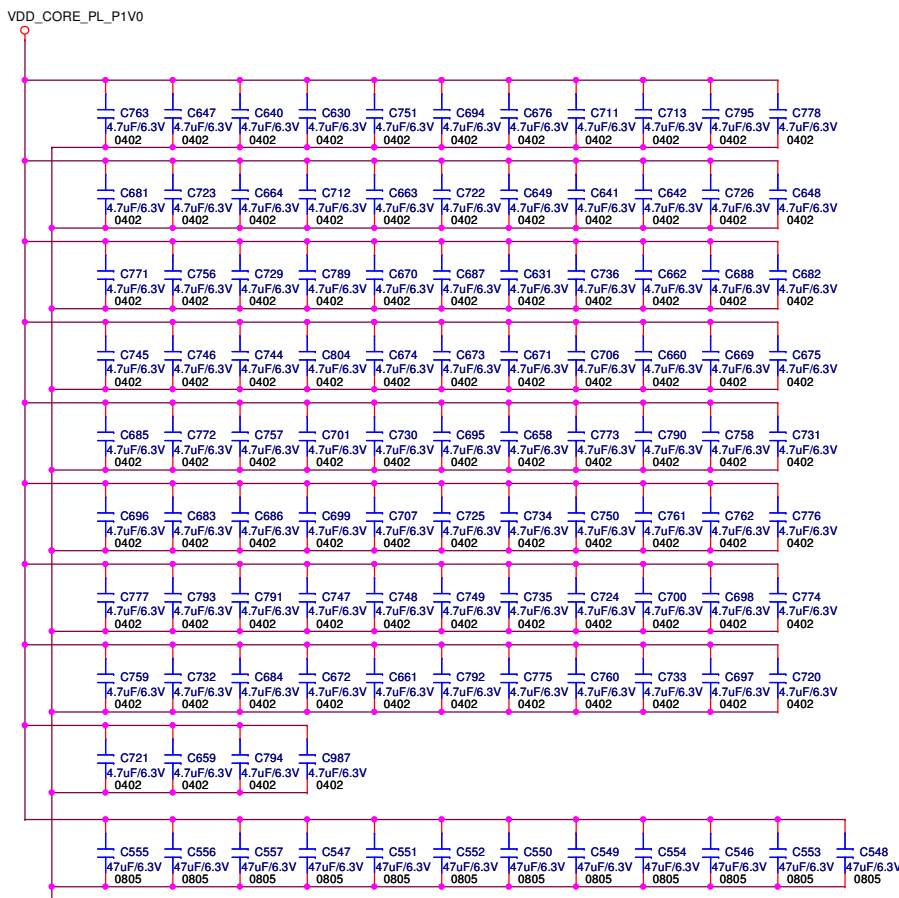
<49> ORIENT\_ERR\_B <<

**i** NOTE: NC\_DET pin is normally NC and floating.  
If the device is mis-installed in any other rotation,  
a GND pad will be at the C42 pin location and the  
ORIENT\_ERR\_B signal will be asserted low.

C42	NC_DET	NC Pins #1	20 of 20
<del>G35	<del>NC01	<del>NC65	<del>AG32
<del>G36	<del>NC02	<del>NC66	<del>AH32
<del>G37	<del>NC03	<del>NC67	<del>AJ32
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SUBASSEMBLY T4240

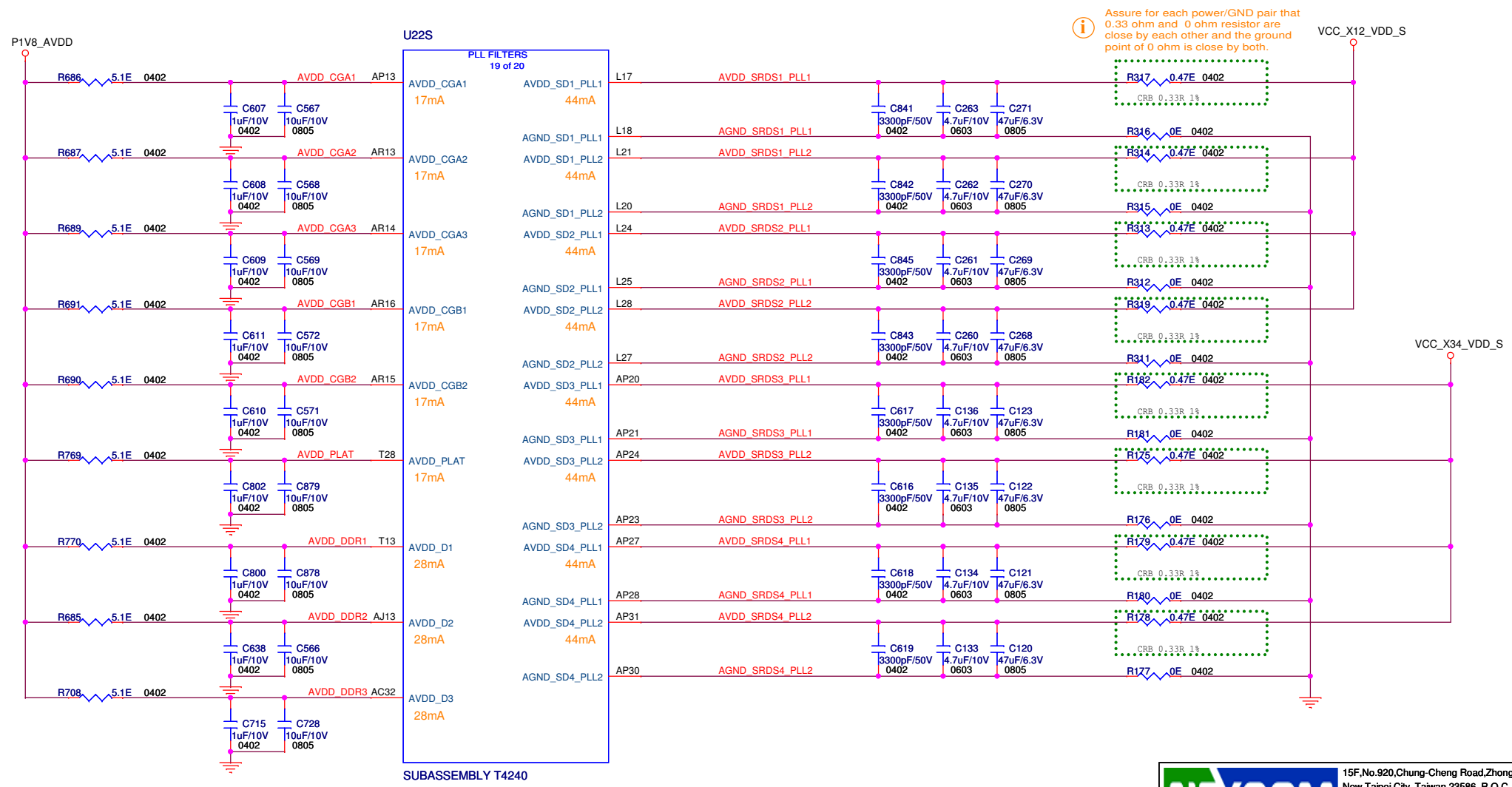
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		Title <b>T4240 NC #1 / Rotation Det</b>	
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX	
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SUBASSEMBLY T4240

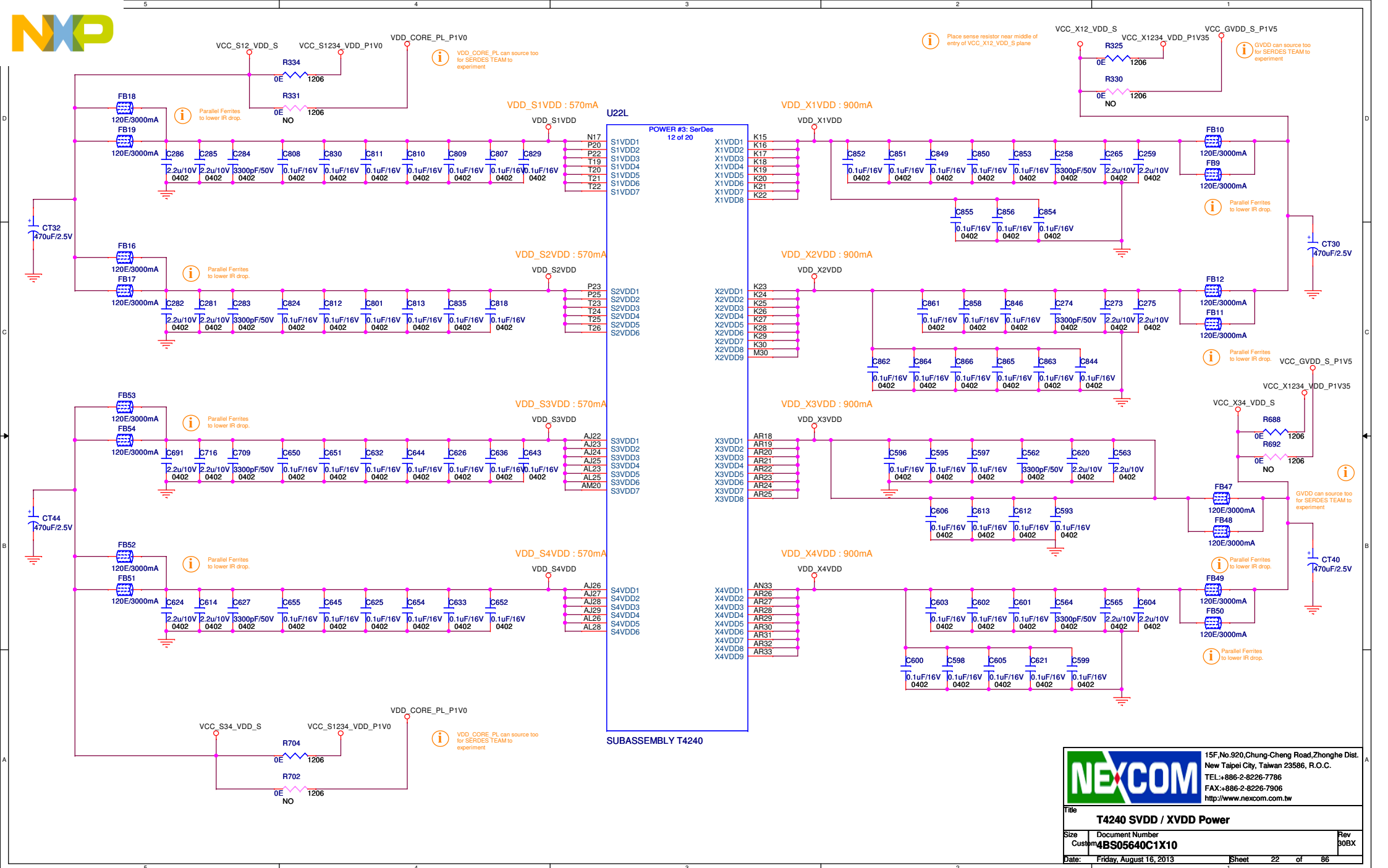
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Title <b>T4240 VDD Power</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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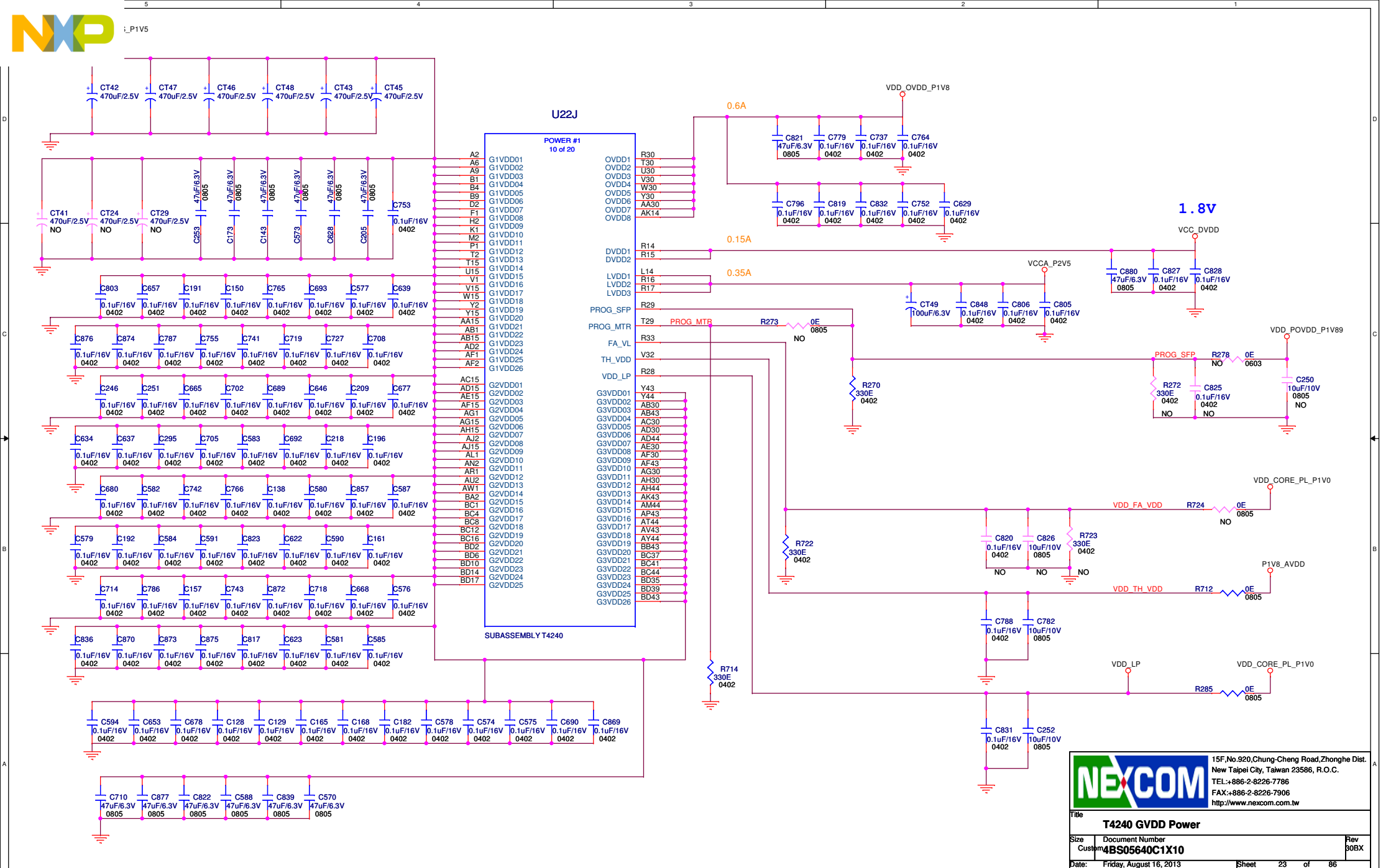
**i** Assure for each power/GND pair that 0.33 ohm and 0 ohm resistor are close by each other and the ground point of 0 ohm is close by both.

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Title <b>T4240 PLL Filters</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
Date:	Friday, August 16, 2013	Sheet 21 of 86



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Title		
<b>T4240 SVDD / XVDD Power</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
Date:	Friday, August 16, 2013	Sheet 22 of 86



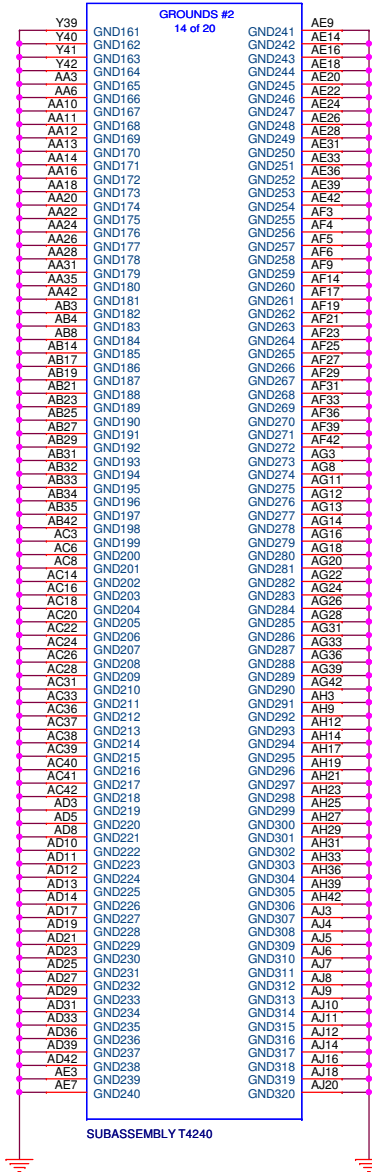
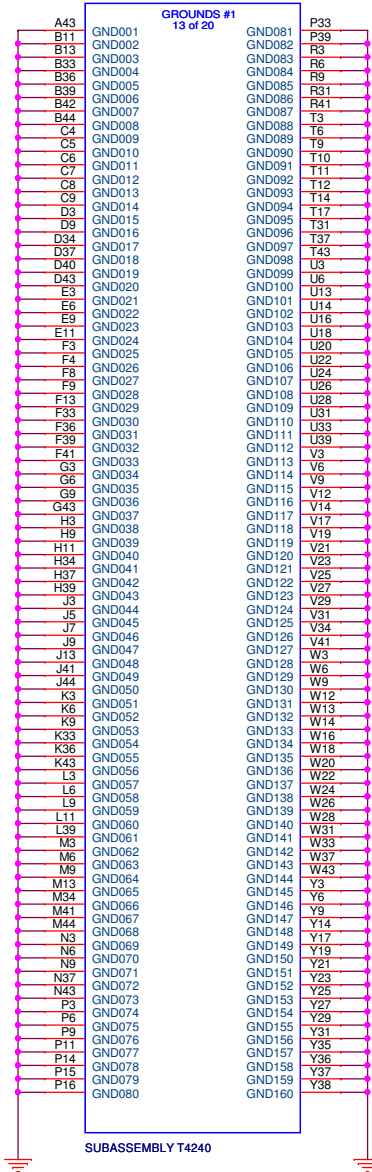
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Title		
<b>T4240 GVDD Power</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
Date:	Friday, August 16, 2013	Sheet 23 of 86



U22M

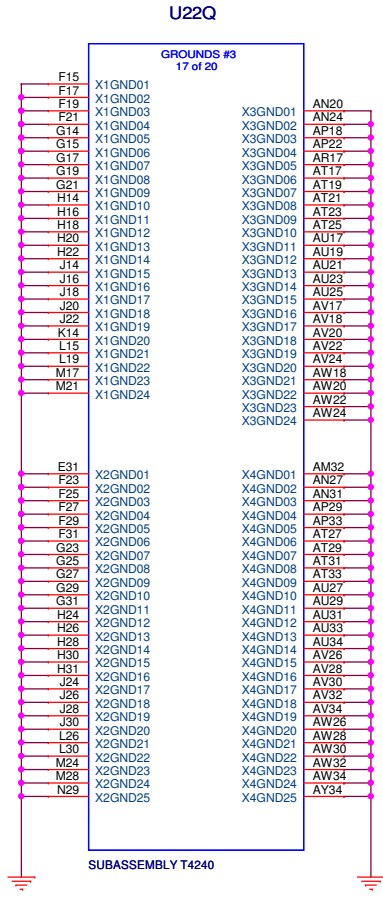
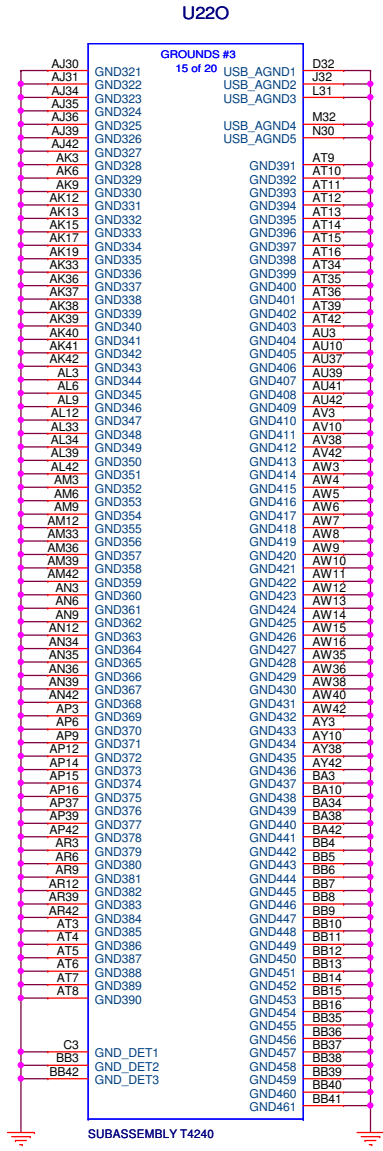
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Title		
<b>T4240 Grounds #1</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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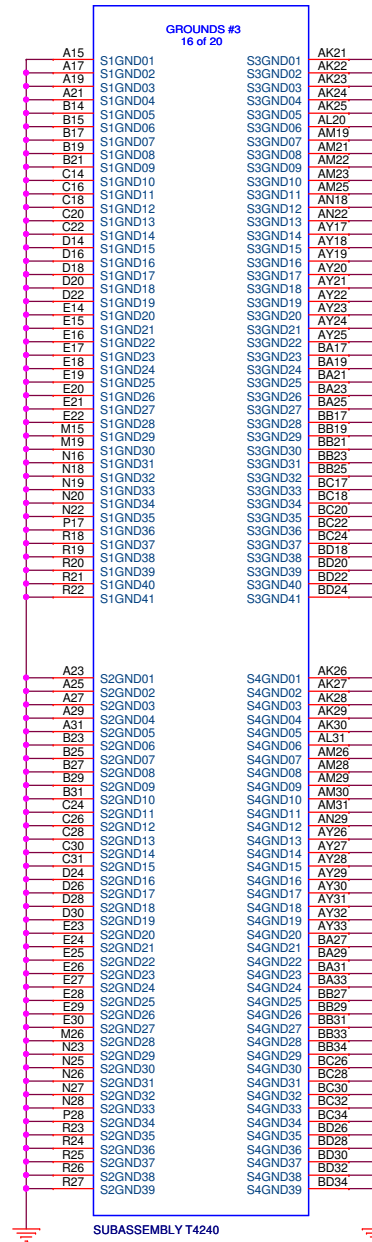




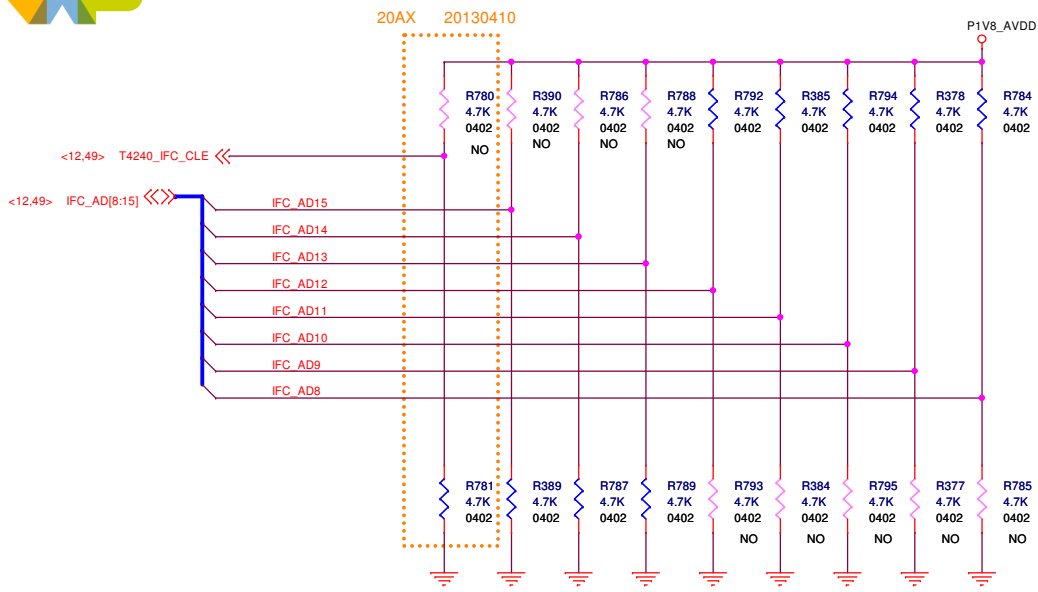
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Title		
<b>T4240 Grounds #2</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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U22P



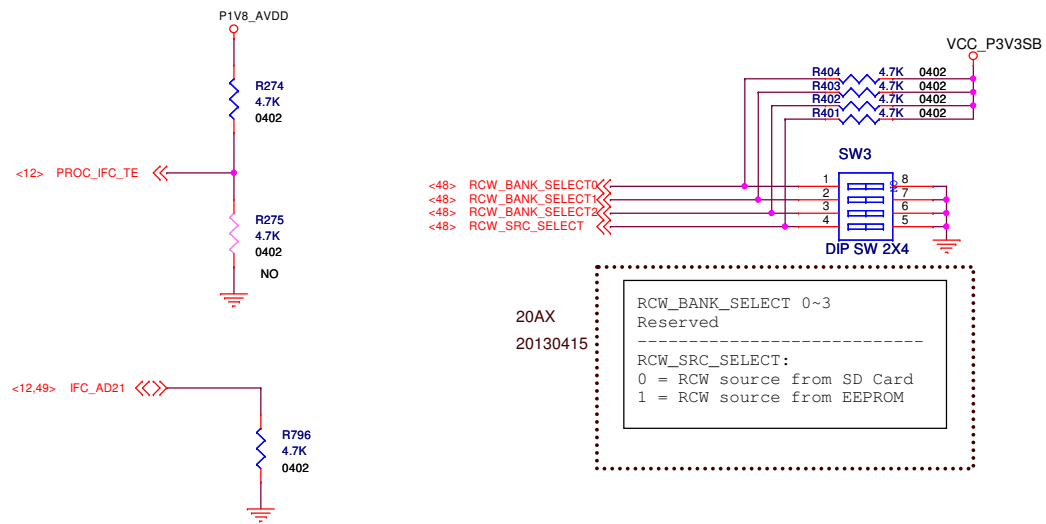
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		Title <b>T4240 Grounds #3</b>	
Size	Document Number	Rev	
Customer	<b>4BS05640C1X10</b>	30BX	
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cfg\_rcw\_src[0:8] : IFC\_AD[8:15], IFC\_CLE

0_0100_1000 <sup>1</sup>	I2C1 normal addressing (supports ROMs up to 256 bytes)	← Default
--------------------------	--	-----------

0_0100_0000 <sup>1</sup>	SD/MMC (eSDHC)
--------------------------	----------------



20AX  
20130415

RCW\_BANK\_SELECT 0~3  
Reserved

RCW\_SRC\_SELECT:  
0 = RCW source from SD Card  
1 = RCW source from EEPROM

Table 4-25. IFC External Transceiver Enable Polarity Select

Functional Signals	Reset Configuration Name	Value (Binary)	IFC External Transmitter Polarity
IFC_TE	cfg_ifc_te	0	IFC drives logic 1 for TE assertion
		1	IFC drives logic 0 for TE assertion

← Default

Table 4-23. DRAM Type Select

Functional Signals	Reset Configuration Name	Value (Binary)	DRAM Type
IFC_AD[21]	cfg_dram_type	0	DDR3 technology (1.5 V)
		1	DDR3L technology (1.35 V)

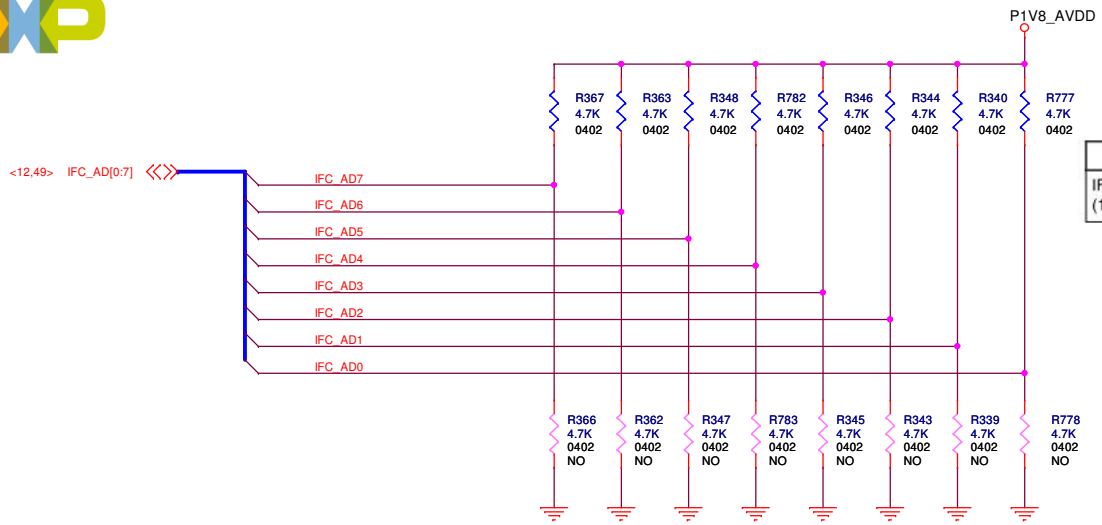
← Default

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Title: **STRAP PIN I**

Size: Document Number  
Customer: **4BS05640C1X10** Rev: 30BX

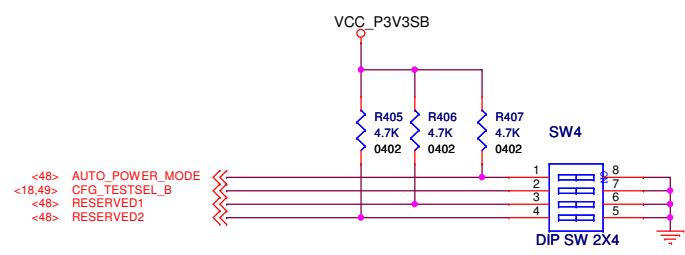
Date: Friday, August 16, 2013 Sheet 27 of 86



**Table 4-22. General-Purpose Input**

Functional Signals	Reset Configuration Name	Value (Binary)	General Purpose Input
IFC_AD[0:7] Default (1111_1111)	cfg_gpinput[0:7]	all	Application-defined

Default



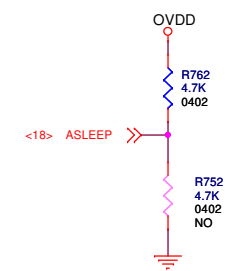
AutoPower Mode  
 0 = Always power up  
 1 = Normal power on/off (default)

CFG\_TESTSEL\_B  
 0 = T4160 Mode  
 1 = T4240 Mode (default)

RESERVED1:  
 Reserved

RESERVED2:  
 Reserved

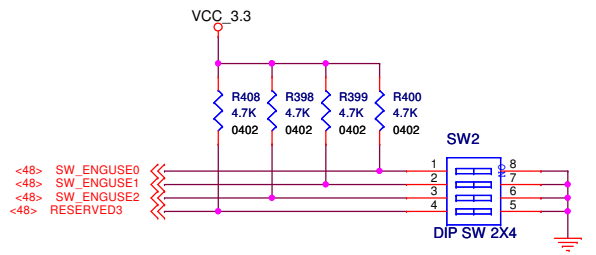
20AX 20130801



**Table 4-24. SerDes XVDD Voltage Select**

Functional Signals	Reset Configuration Name	Value (Binary)	XVDD Voltage
ASLEEP Default (1)	cfg_xvdd_sel	0	1.5 V
		1	1.35 V

Default



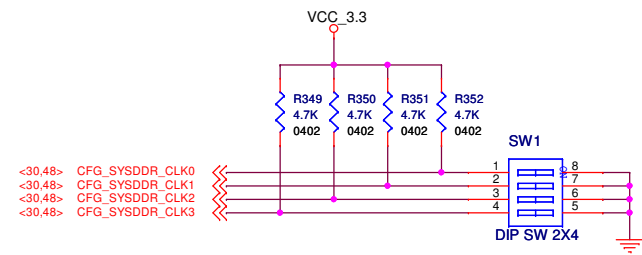
ENG-USE  
 > 1111 = Reserved

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**Output Frequency Reference Table**

XTAL (MHz)	FSEL[3:0]	SYSCLK QA & QB (MHz)	DDRCLK QC (MHz)
25	0000	66.67	66.67
25	0001	66.67	100
25	0010	66.67	125
25	0011	66.67	133.33
25	0100	100	66.67
25	0101	100	100
25	0110	100	125
25	0111	100	133.33
25	1000	125	66.67
25	1001	125	100
25	1010	125	125
25	1011	125	133.33
25	1100	133.33	66.67
25	1101	133.33	100
25	1110	133.33	125
25	1111	133.33	133.33

Default

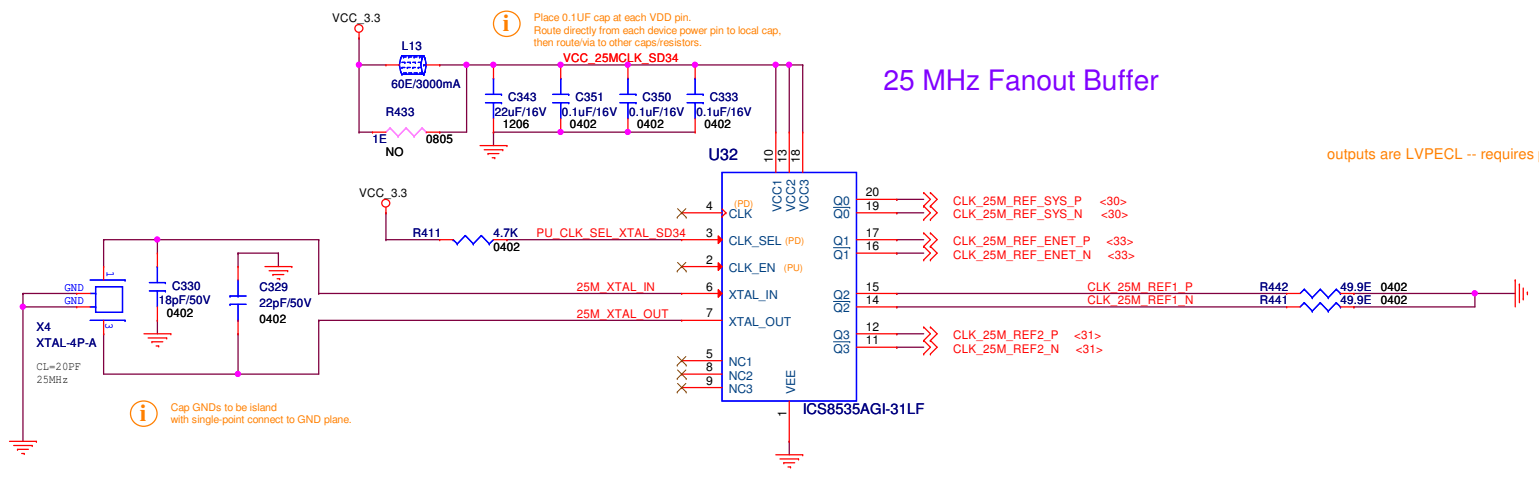


<30.48> CFG\_SYSDDR\_CLK0  
 <30.48> CFG\_SYSDDR\_CLK1  
 <30.48> CFG\_SYSDDR\_CLK2  
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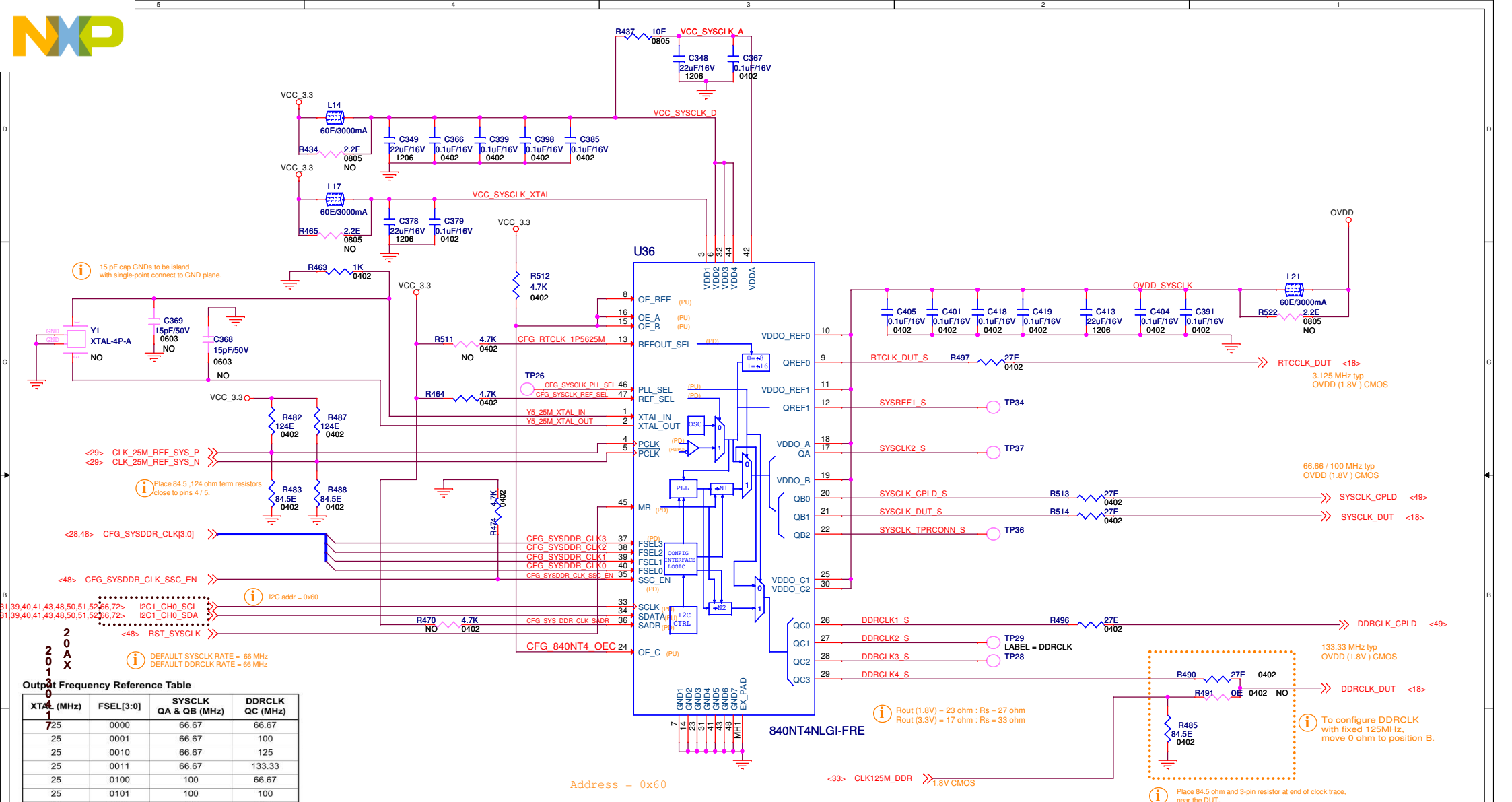
Title: **STRAP PIN II**

Size: Document Number  
 Customer: **4BS05640C1X10** Rev: 30BX

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Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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15 pF cap GNDs to be island with single-point connect to GND plane.

Place 84.5, 124 ohm term resistors close to pins 4 / 5.

I2C addr = 0x60

DEFAULT SYSCLK RATE = 66 MHz  
DEFAULT DDRCLK RATE = 66 MHz

Output Frequency Reference Table

XTAL (MHz)	FSEL[3:0]	SYSCLK QA & QB (MHz)	DDRCLK QC (MHz)
75	0000	66.67	66.67
75	0001	66.67	100
25	0010	66.67	125
25	0011	66.67	133.33
25	0100	100	66.67
25	0101	100	100
25	0110	100	125
25	0111	100	133.33
25	1000	125	66.67
25	1001	125	100
25	1010	125	125
25	1011	125	133.33
25	1100	133.33	66.67
25	1101	133.33	100
25	1110	133.33	125
25	1111	133.33	133.33

Address = 0x60

Rout (1.8V) = 23 ohm : Rs = 27 ohm  
Rout (3.3V) = 17 ohm : Rs = 33 ohm

Place 84.5 ohm and 3-pin resistor at end of clock trace, near the DUT.

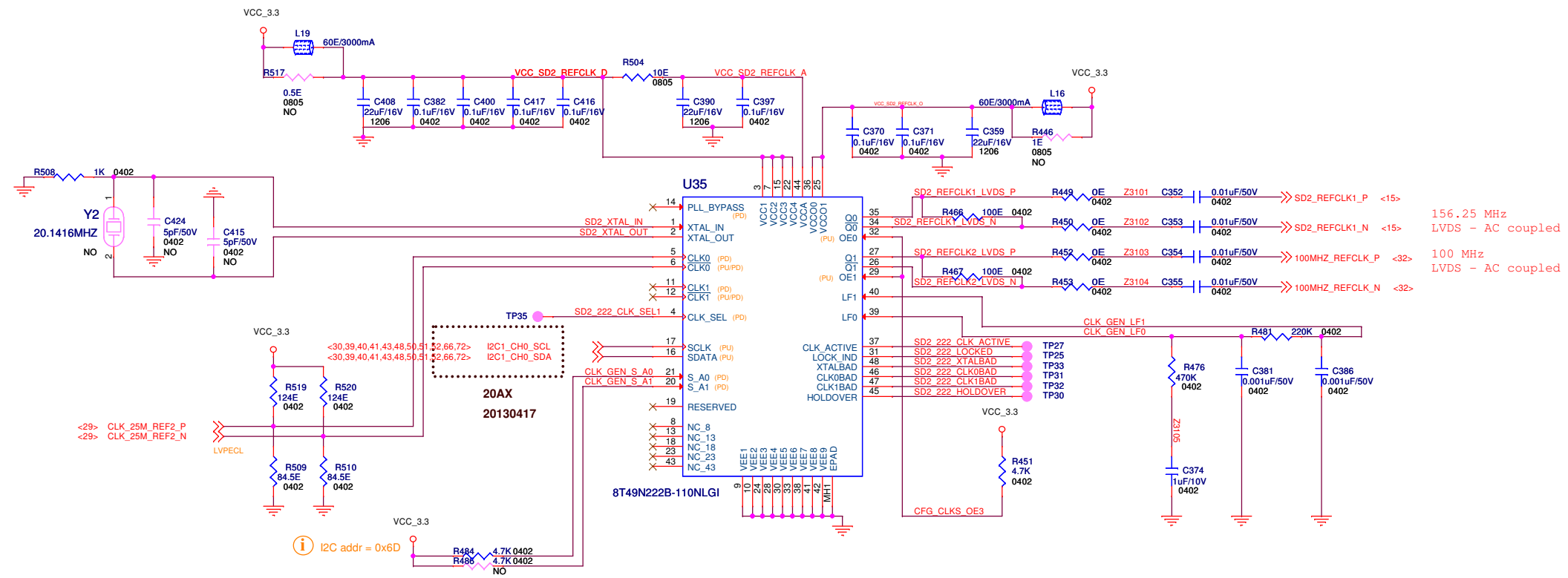
To configure DDRCLK with fixed 125MHz, move 0 ohm to position B.

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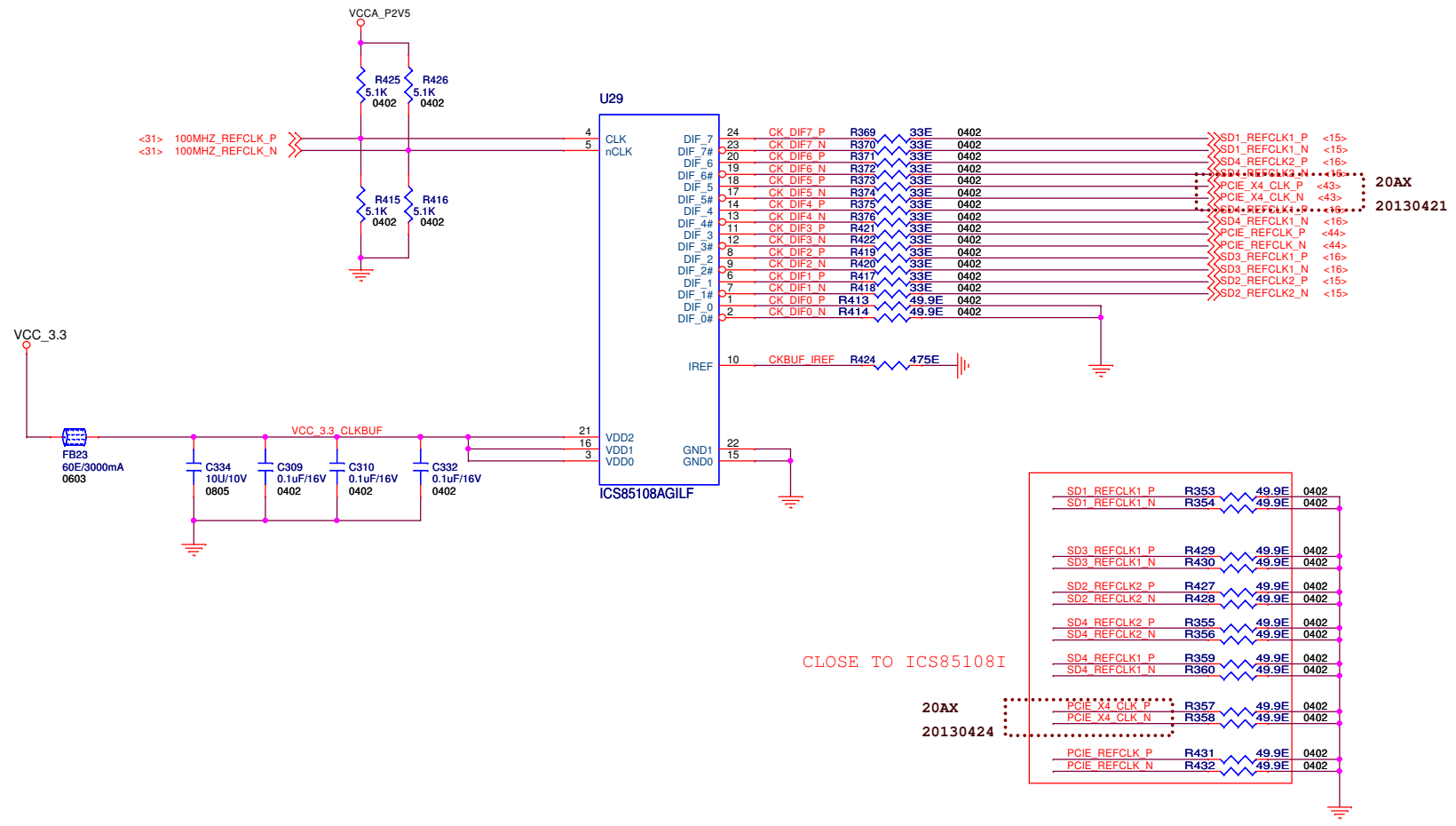
Title <b>SYSCLK_DDRCLK</b>		
Size	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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# SD2 SERDES REFCLKs



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Title: <b>SERDES_Clock_SD2</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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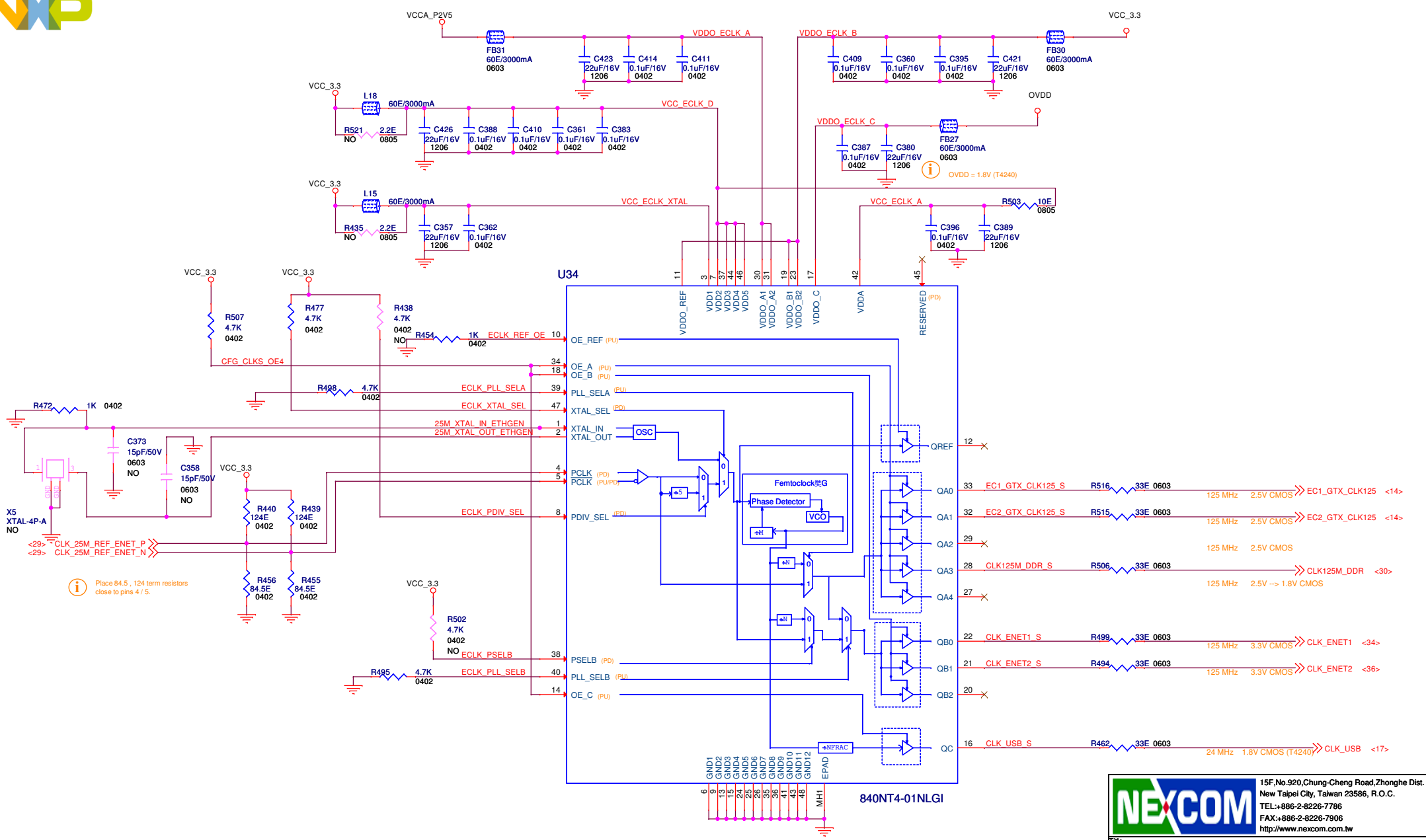
CLOSE TO ICS85108I

20AX  
20130424

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Title		
1 TO 8 CLOCK BUF		
Size	Document Number	Rev
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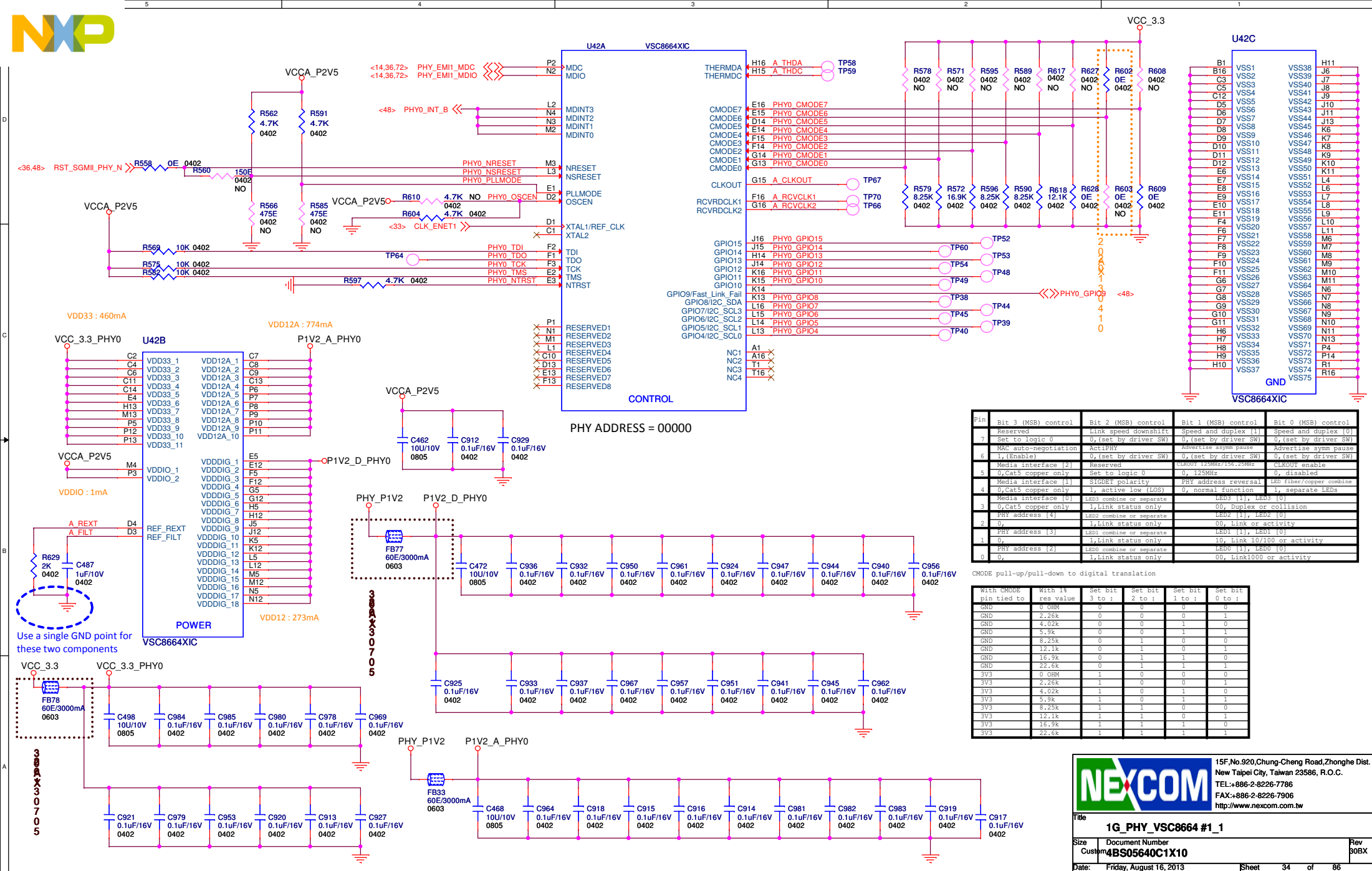




**i** Place 84.5... 124 term resistors close to pins 4 / 5.

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Title <b>ENet_and_USB_Clocks</b>		
Size	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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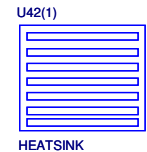
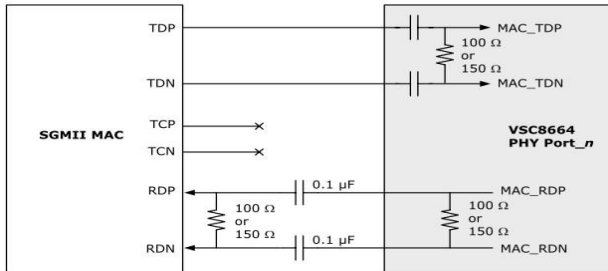
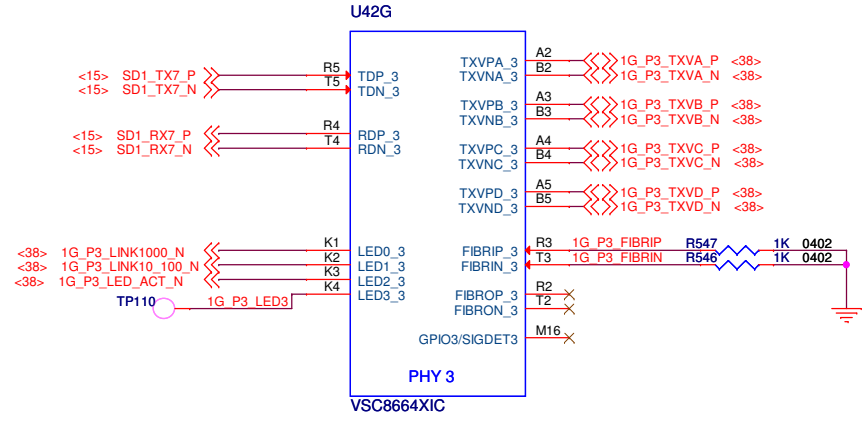
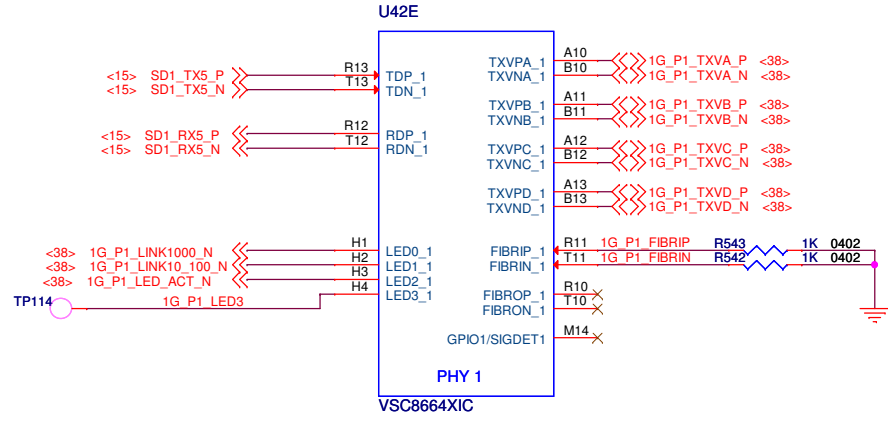
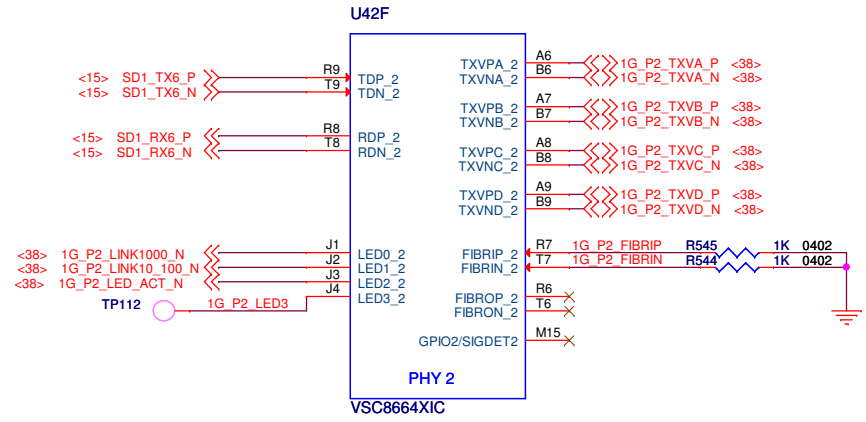
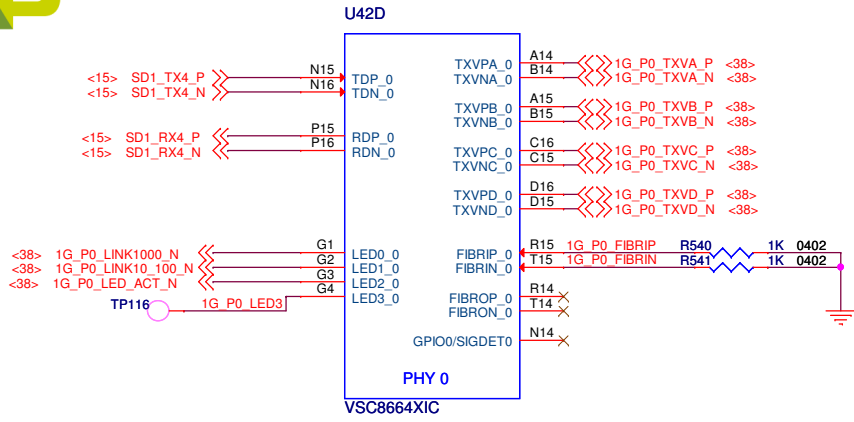
PHY ADDRESS = 00000

Pin	Bit 3 (MSB) control	Bit 2 (MSB) control	Bit 1 (MSB) control	Bit 0 (MSB) control
7	Reserved	Link speed downshift	Speed and duplex [1]	Speed and duplex [0]
6	Set to logic 0	0, (set by driver SW)	0, (set by driver SW)	0, (set by driver SW)
5	MAC auto-negotiation	Advertise asym pause	Advertise sym pause	Advertise sym pause
4	0, Cat5 copper only	0, (set by driver SW)	0, (set by driver SW)	0, (set by driver SW)
3	Media interface [2]	Reserved	0, 125MHz	0, disabled
2	Media interface [1]	SIGBET polarity	PHY address reversal	LED fiber/copper combine
1	0, Cat5 copper only	1, active low (LOS)	0, normal function	1, separate LEDs
0	Media interface [0]	LED3 combine or separate	LED3 [1], LED3 [0]	0, Duplex or collision
PHY address [4]	LED2 combine or separate	LED2 [1], LED2 [0]	0, link or activity	0, link or activity
PHY address [3]	LED1 combine or separate	LED1 [1], LED1 [0]	1, link status only	10, Link 10/100 or activity
PHY address [2]	LED0 combine or separate	LED0 [1], LED0 [0]	1, link status only	00, Link1000 or activity

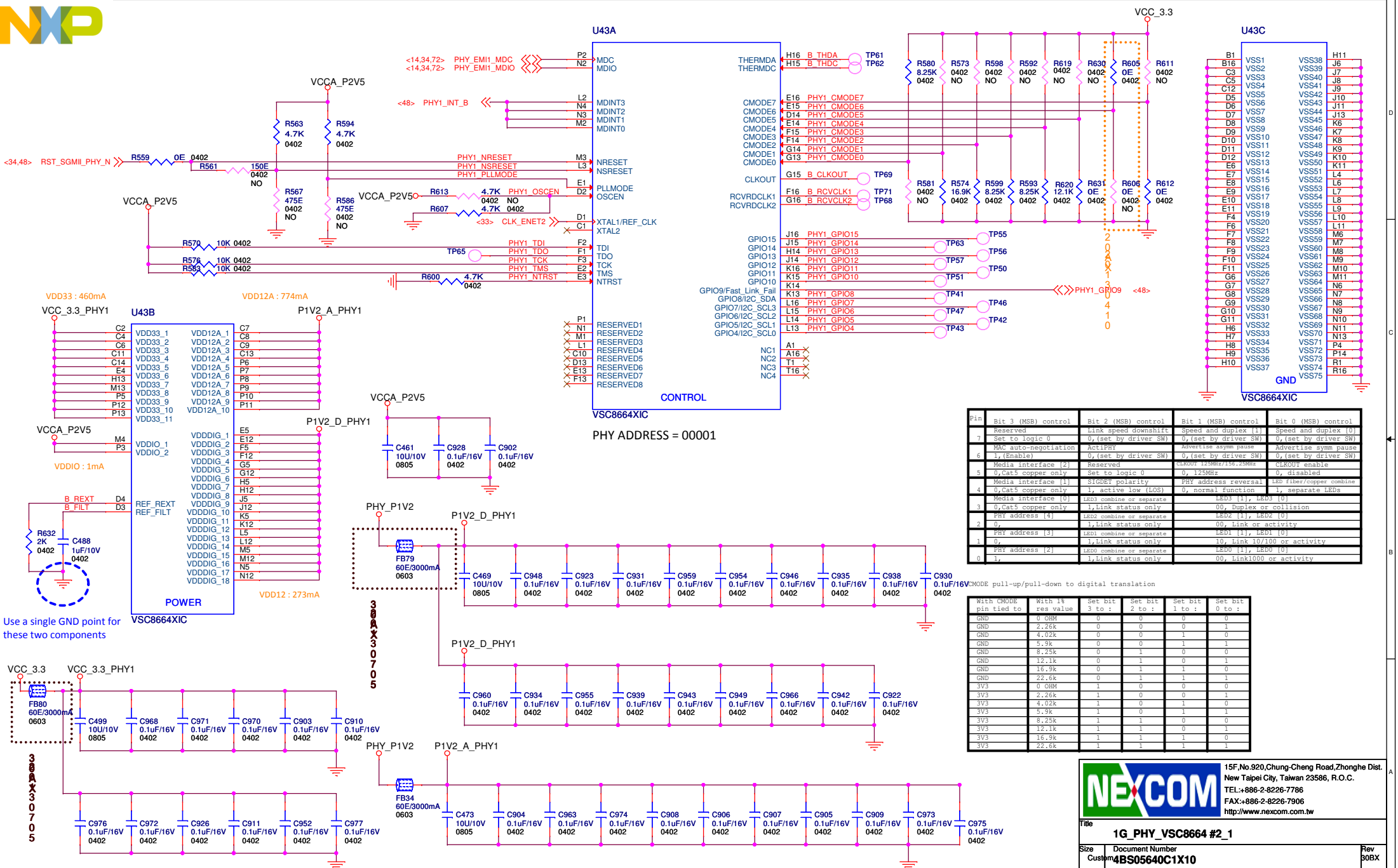
CMODE pull-up/pull-down to digital translation

With CMODE pin tied to	With 1% res value	Set bit 3 to 0	Set bit 2 to 1	Set bit 1 to 0	Set bit 0 to 1
GND	0 OHM	0	0	0	0
GND	2.26k	0	0	0	1
GND	4.02k	0	0	1	0
GND	5.9k	0	0	1	1
GND	8.25k	0	1	0	0
GND	12.1k	0	1	0	1
GND	16.9k	0	1	1	0
GND	22.6k	0	1	1	1
3V3	0 OHM	1	0	0	0
3V3	2.26k	1	0	0	1
3V3	4.02k	1	0	1	0
3V3	5.9k	1	0	1	1
3V3	8.25k	1	1	0	0
3V3	12.1k	1	1	0	1
3V3	16.9k	1	1	1	0
3V3	22.6k	1	1	1	1

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Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX	
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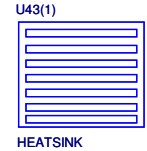
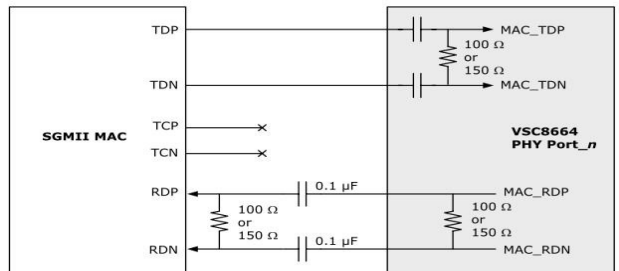
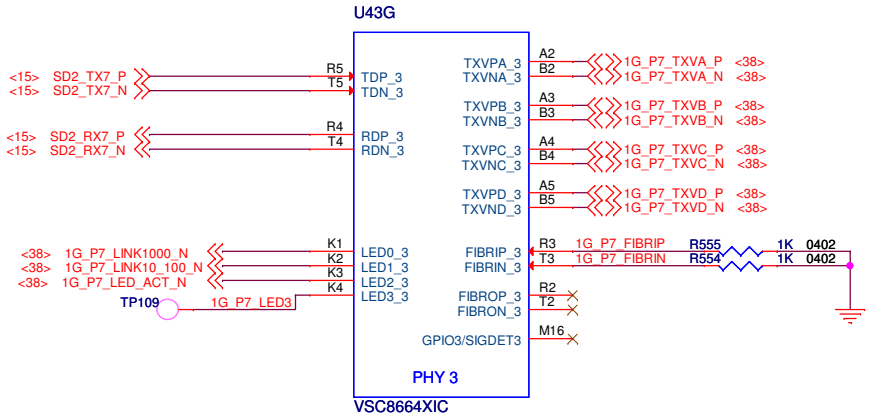
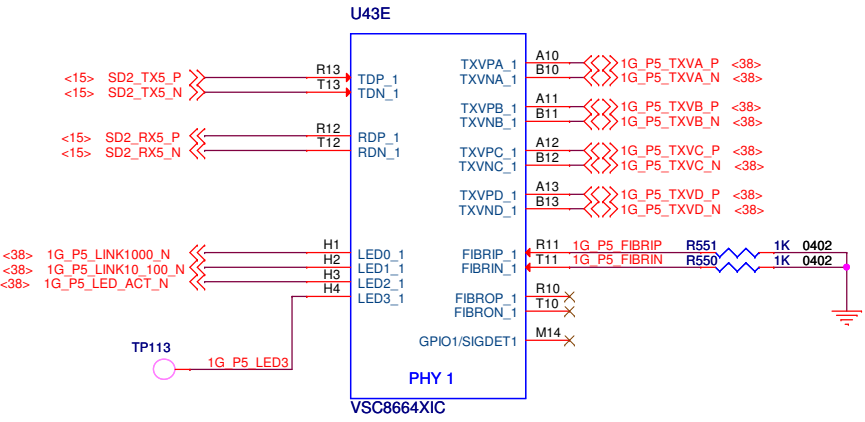
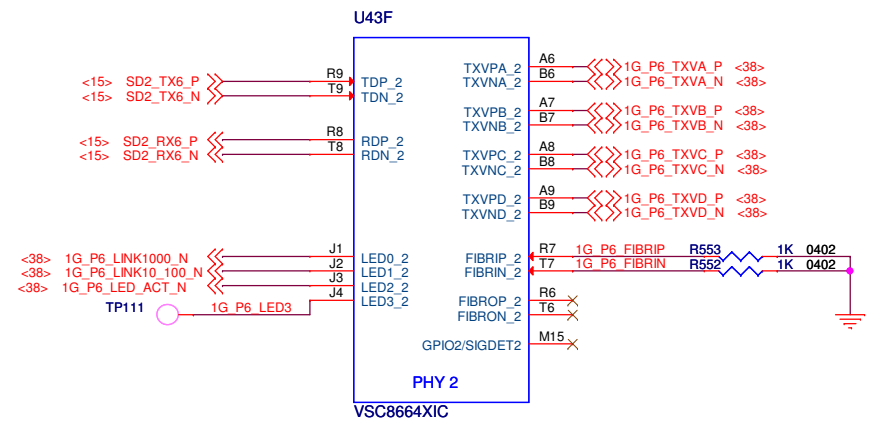
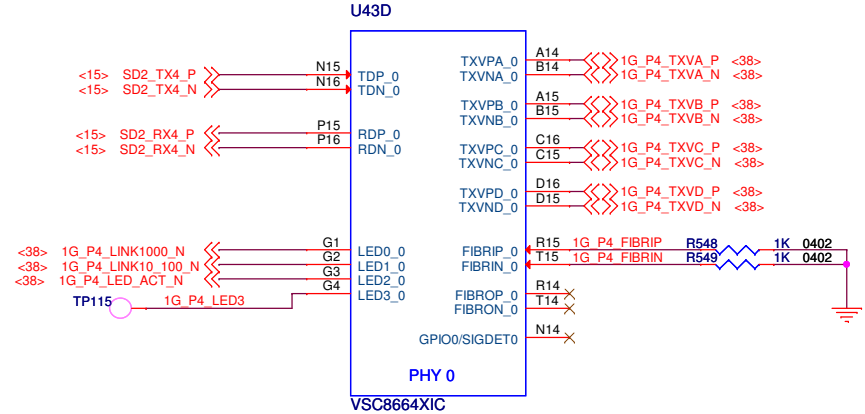


Pin	Bit 3 (MSB) control	Bit 2 (MSB) control	Bit 1 (MSB) control	Bit 0 (MSB) control
Reserved	Reserved	Link speed downshift	Speed and duplex [1]	Speed and duplex [0]
7	Set to logic 0	0, (set by driver SW)	0, (set by driver SW)	0, (set by driver SW)
6	MAC auto-negotiation	ActiPHY	Advertise asym pause	Advertise sym pause
5	1, (Enable)	0, (set by driver SW)	0, (set by driver SW)	0, (set by driver SW)
4	Media interface [2]	Reserved	clk0/en enable	clk0/en enable
3	0, Cat5 copper only	Set to logic 0	0, 125MHz	0, disabled
2	Media interface [1]	SIGDET polarity	PHY address reversal	LED fiber/copper combine
1	0, Cat5 copper only	1, active low (LOS)	0, normal function	1, separate LEDs
0	Media interface [0]	LED3 combine or separate	LED3 [1], LED3 [0]	0, Duplex or collision
3	0, Cat5 copper only	1, Link status only	0, Duplex or collision	LED3 [1], LED3 [0]
2	PHY address [4]	LED2 combine or separate	LED2 [1], LED2 [0]	0, Link or activity
1	PHY address [3]	LED1 combine or separate	LED1 [1], LED1 [0]	1, Link or activity
0	PHY address [2]	LED0 combine or separate	LED0 [1], LED0 [0]	0, Link1000 or activity

With CMODE pin tied to	With 1k res value	Set bit 3 to:	Set bit 2 to:	Set bit 1 to:	Set bit 0 to:
GND	0 OHM	0	0	0	0
GND	2.26k	0	0	1	1
GND	4.02k	0	0	1	0
GND	5.9k	0	0	1	1
GND	8.25k	0	1	0	0
GND	12.1k	0	1	0	1
GND	16.9k	0	1	1	0
GND	22.6k	0	1	1	1
3V3	0 OHM	1	0	0	0
3V3	2.26k	1	0	0	1
3V3	4.02k	1	0	1	0
3V3	5.9k	1	0	1	1
3V3	8.25k	1	1	0	0
3V3	12.1k	1	1	0	1
3V3	16.9k	1	1	1	0
3V3	22.6k	1	1	1	1

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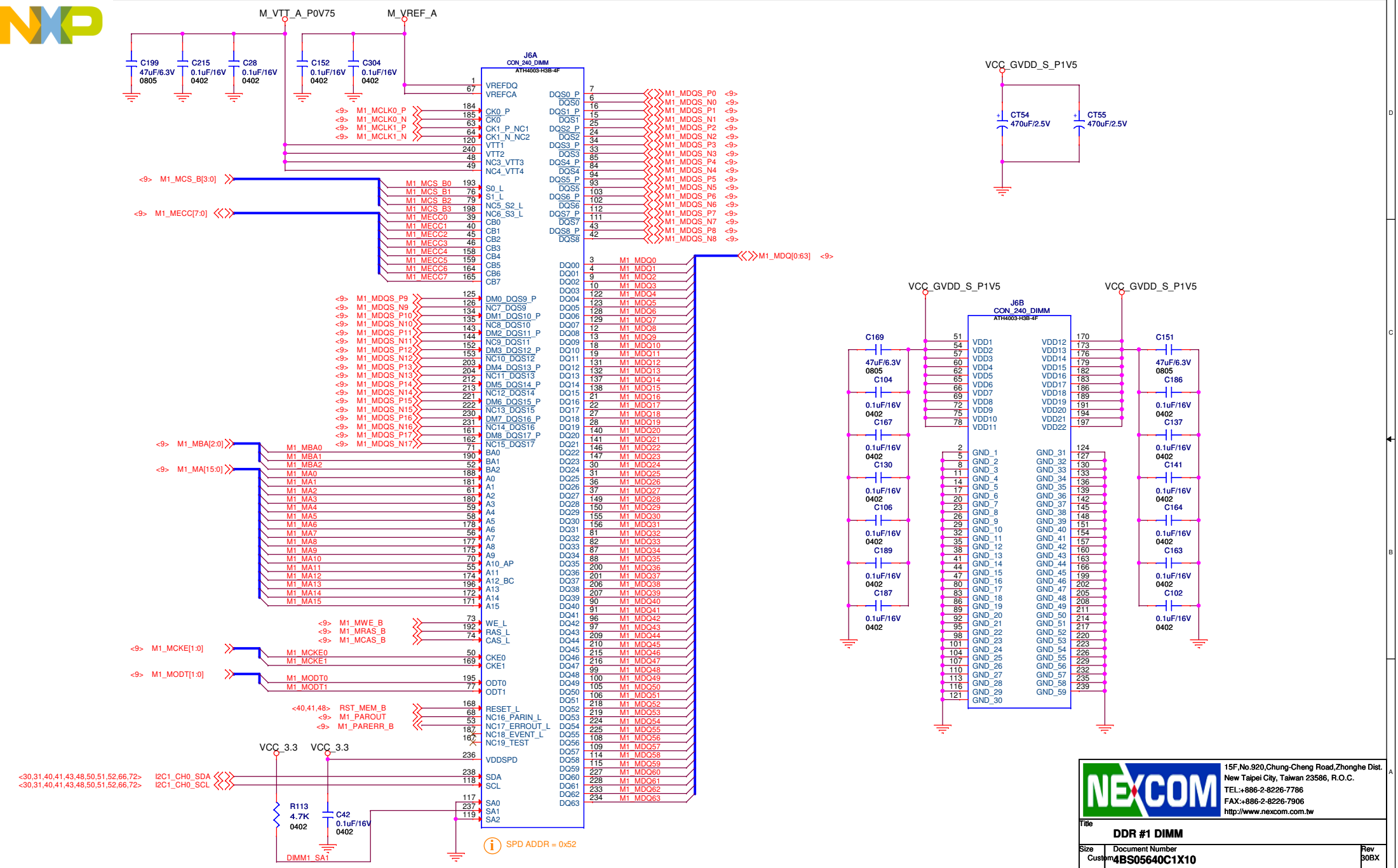
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 Size: Document Number  
 Customer: 4BS05640C1X10  
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		Title <b>1G_PHY_VSC8664 #2_2</b>	
Size B	Document Number <b>4BS05640C1X10</b>		Rev 30BX
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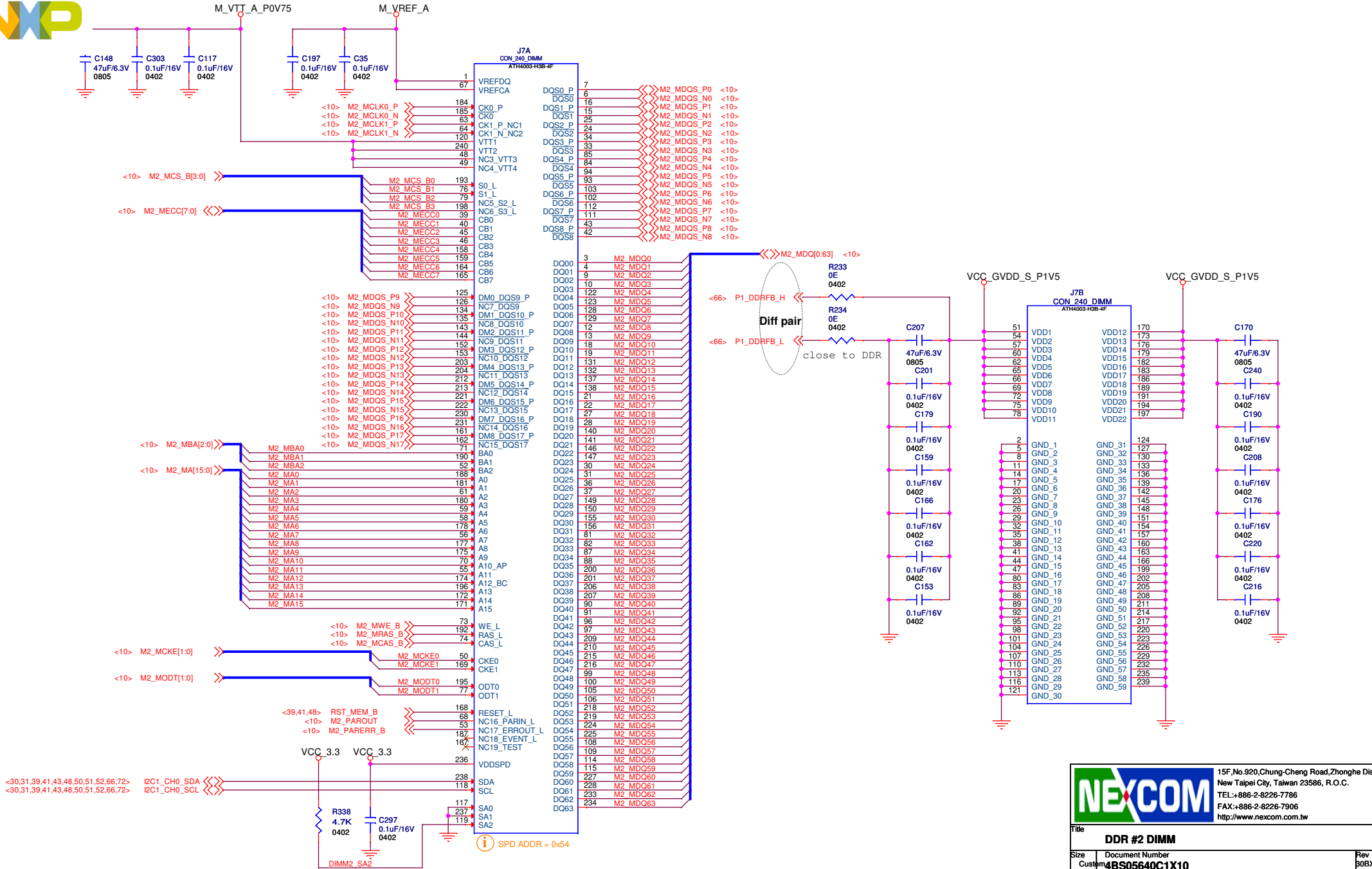




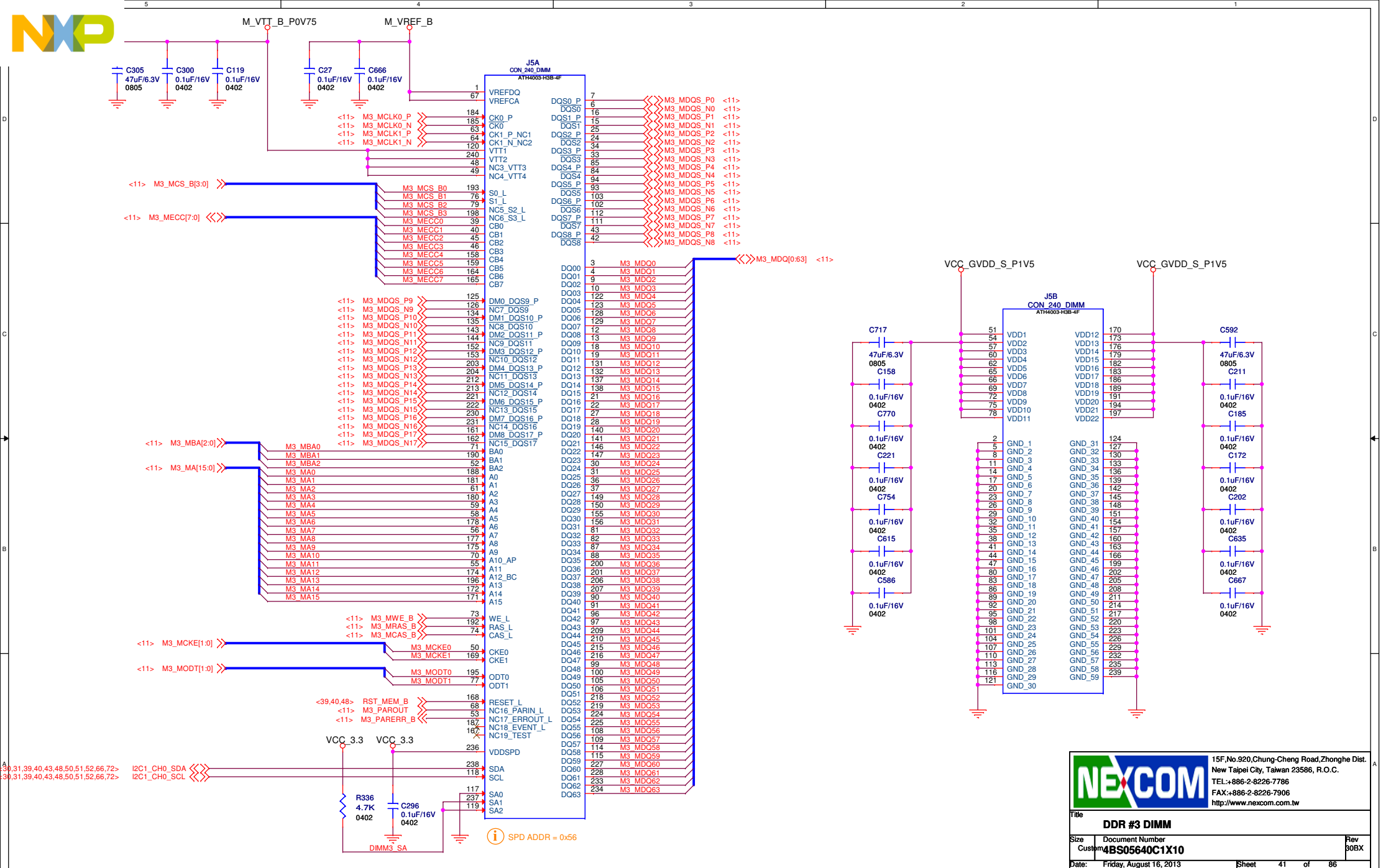
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Title		
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SPD ADDR = 0x52



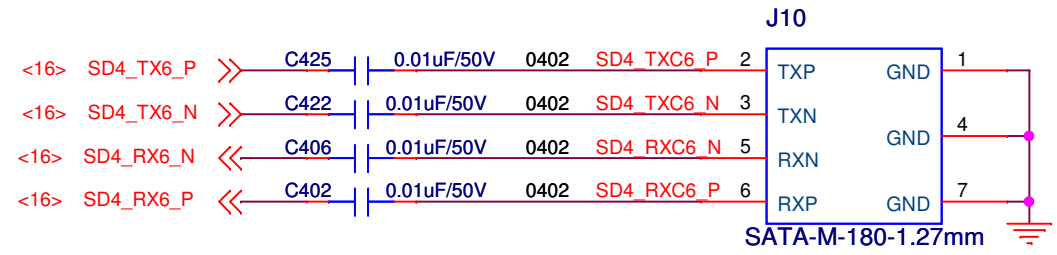





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<b>DDR #3 DIMM</b>		
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Customer	<b>4B05640C1X10</b>	30BX
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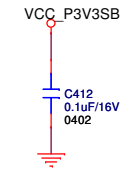
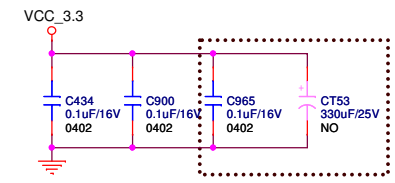
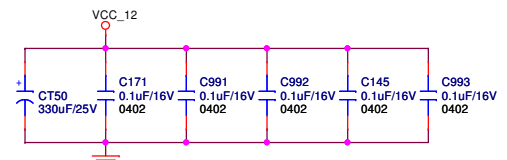
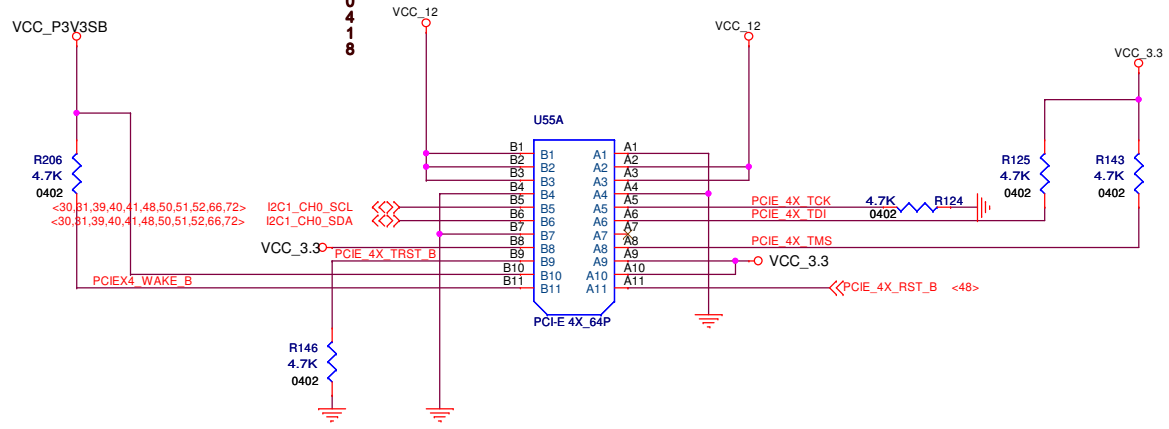
SATA PORT



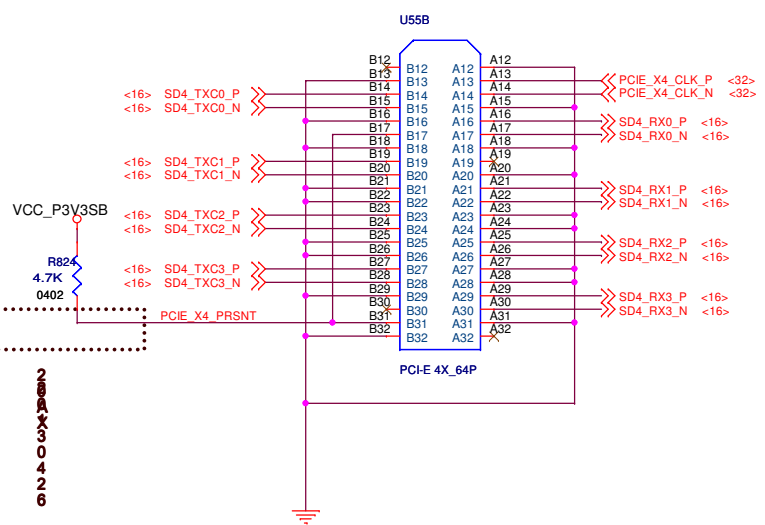
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		Title <b>SATA</b>	
Size A	Document Number <b>4BS05640C1X10</b>		Rev 30BX
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5 2 2  
0 0  
A X  
3  
0 4  
1 8



2  
0  
A  
3  
0 4  
2 6



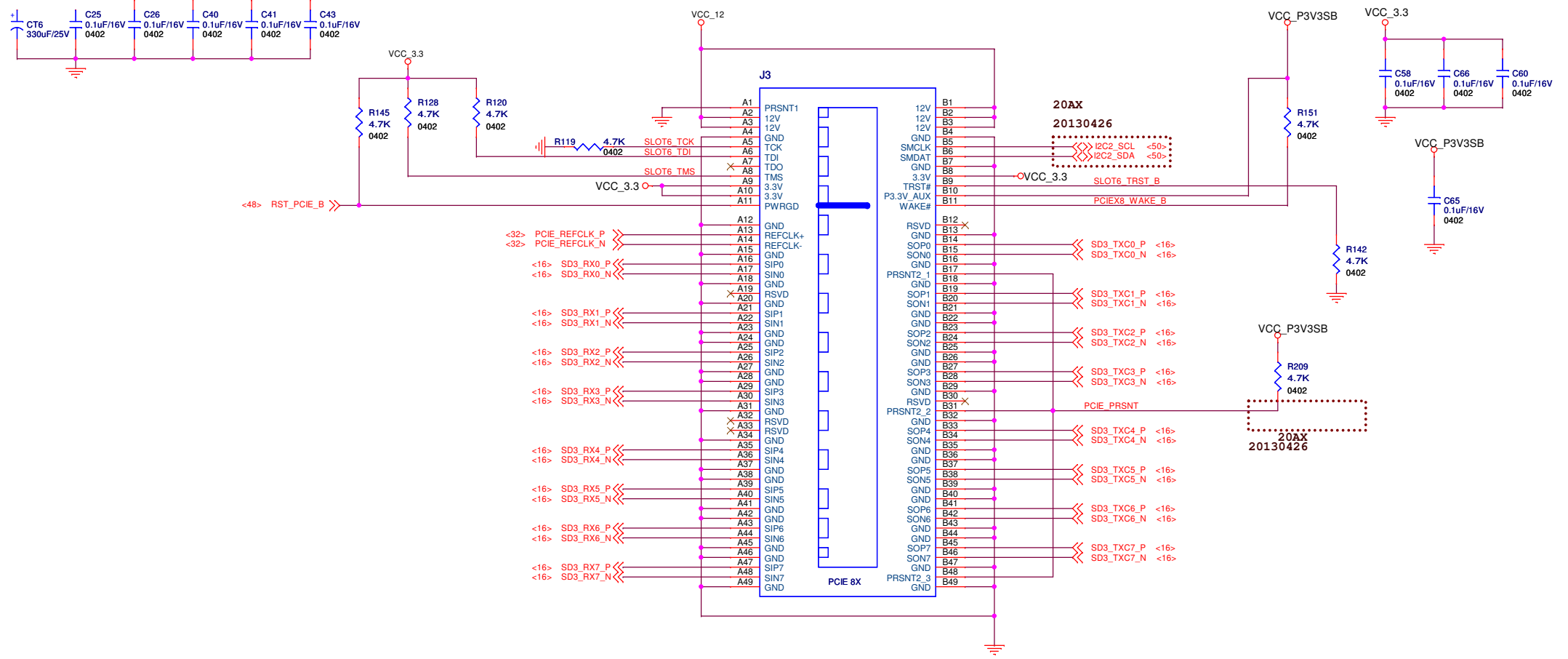
2  
0  
A  
3  
0 4  
2 6

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Customer	<b>4BS05640C1X10</b>	30BX
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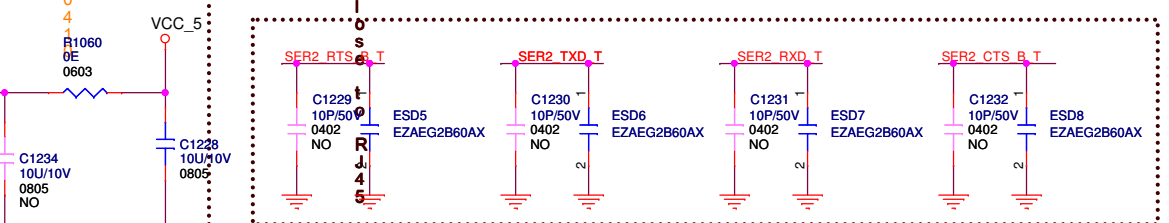
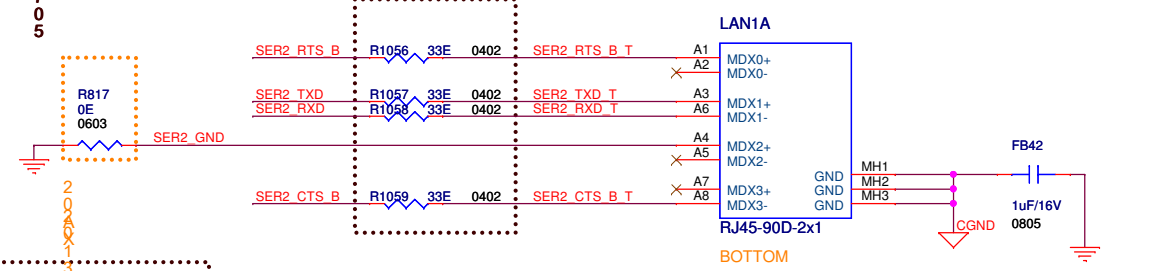
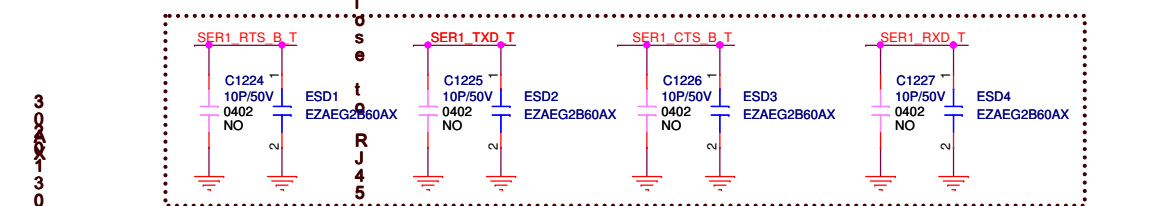
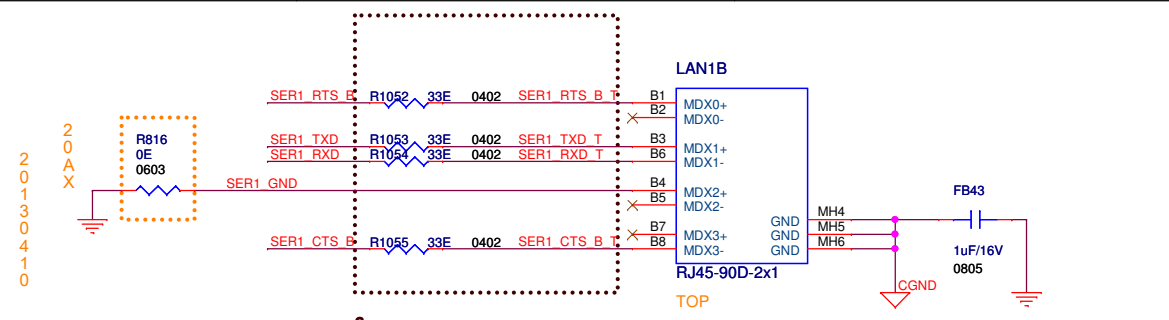
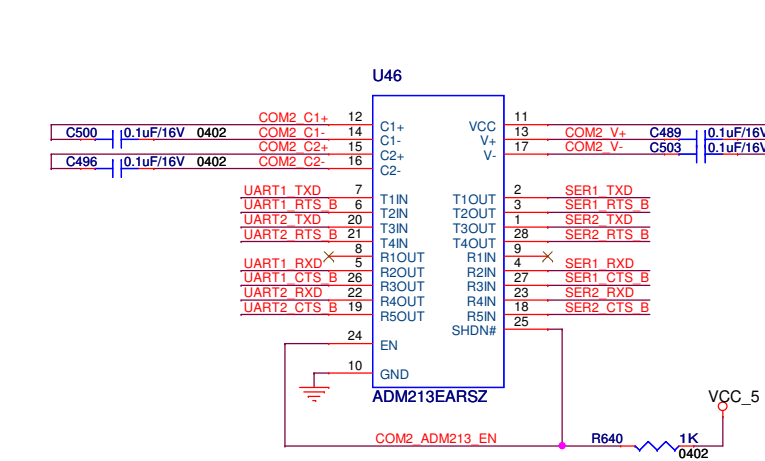
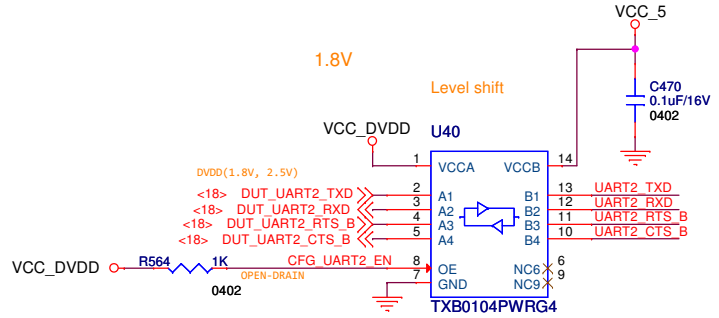
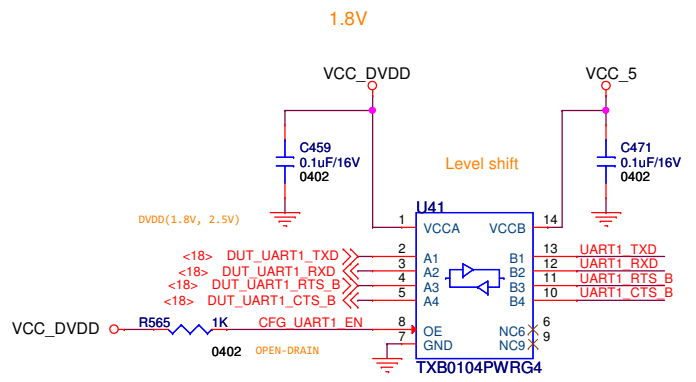


VCC\_12 : 2100mA  
VCC\_3.3 : 3000mA



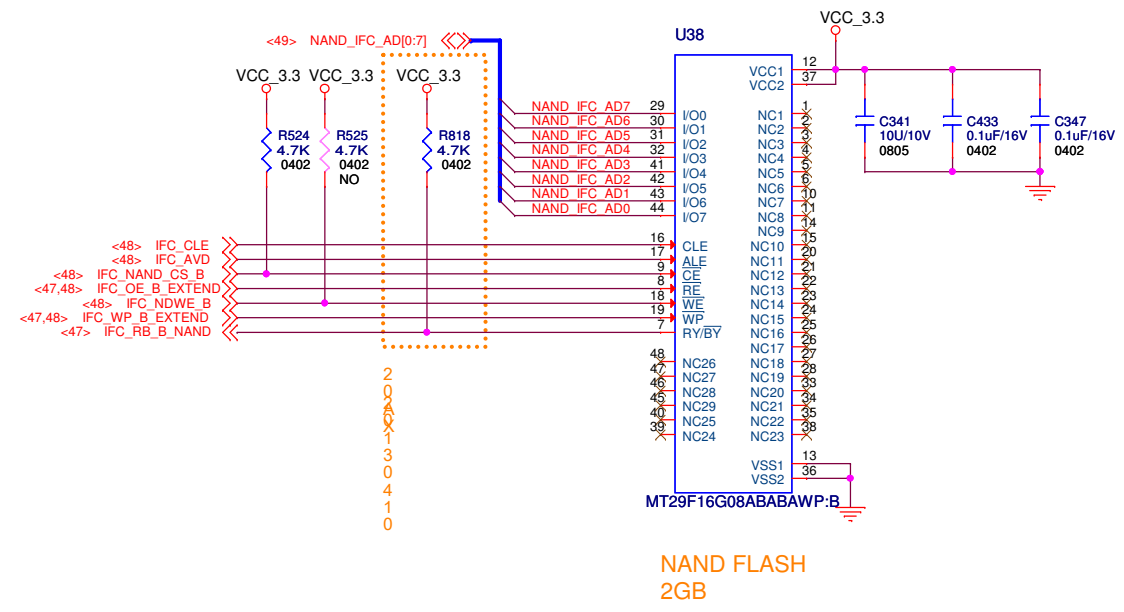
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Title <b>PCIe slot X8</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
Date:	Friday, August 16, 2013	Sheet 44 of 86



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Title		
<b>UART</b>		
Size	Document Number	Rev
B	<b>4BS05640C1X10</b>	30BX
Date:	Friday, August 16, 2013	Sheet 45 of 86

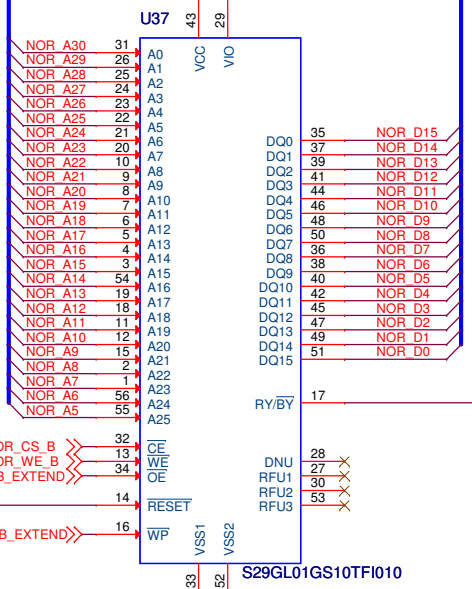


NAND FLASH  
2GB

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		Title <b>NANDFlash</b>	
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX	
Date: Friday, August 16, 2013		Sheet 46 of 86	



<49> NOR\_D[0:15] <<>  
<49> NOR\_A[5:30] <>>







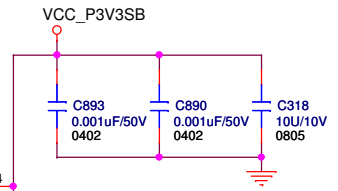
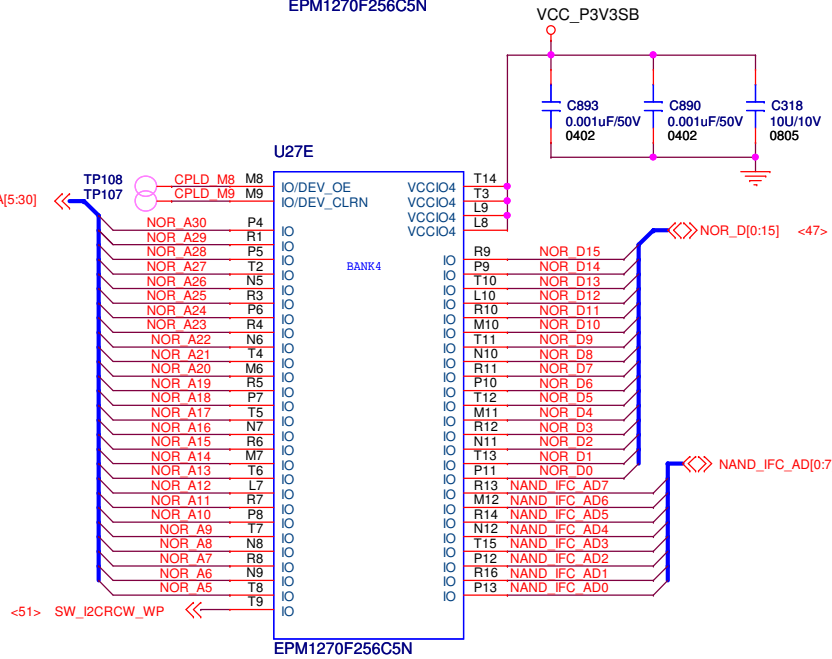
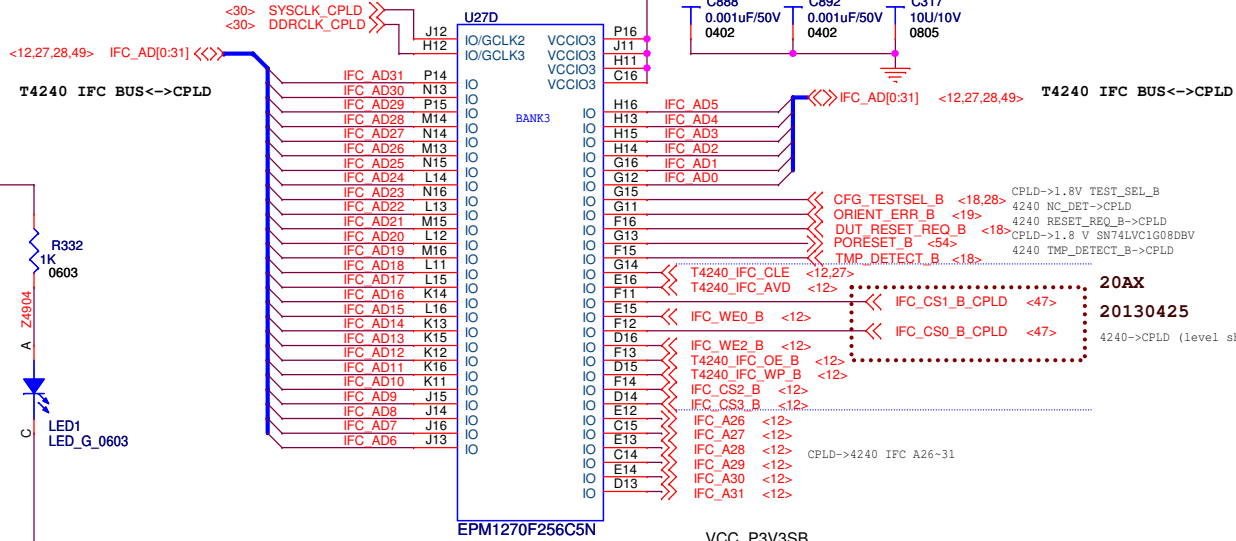
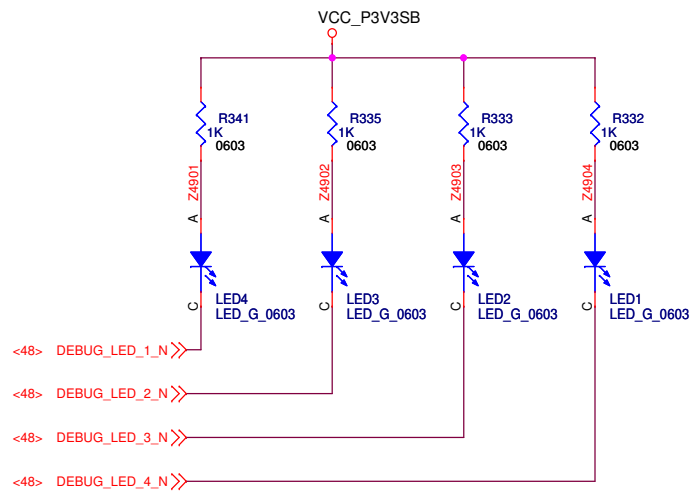
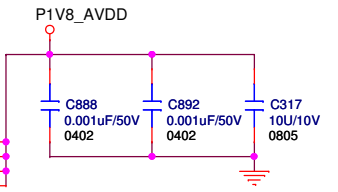
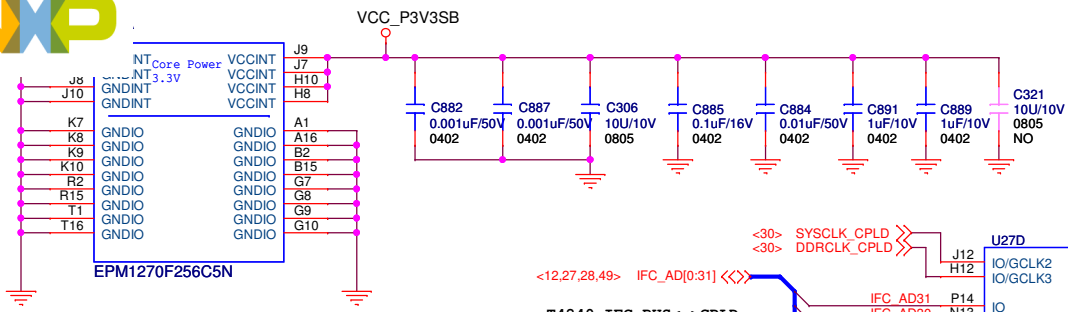


Table 2-7. MAX II MultiVolt I/O Support (Note 1)

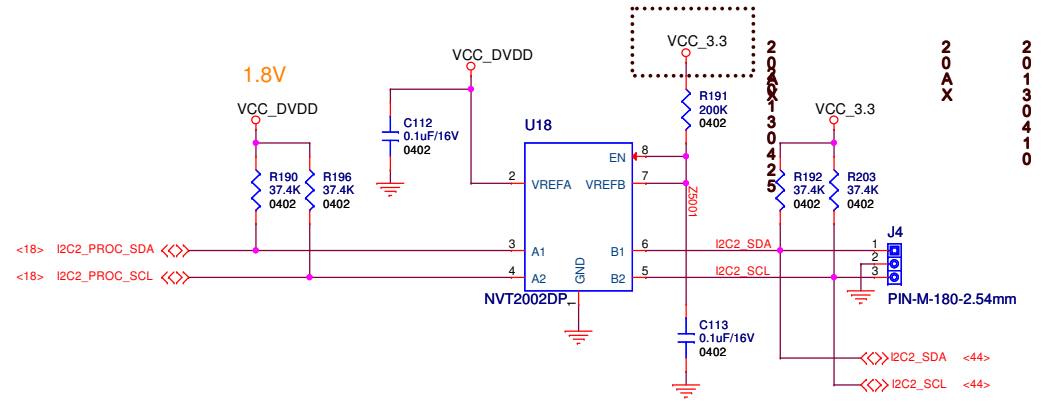
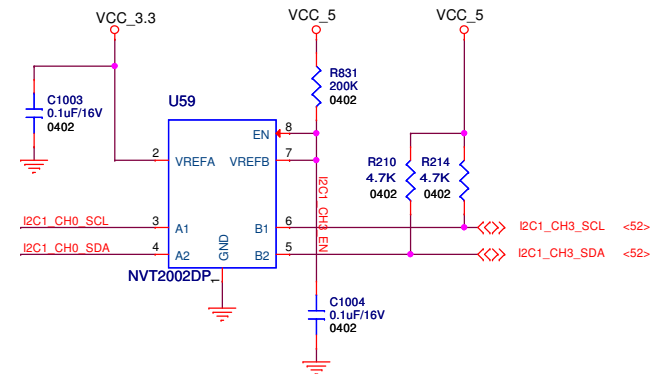
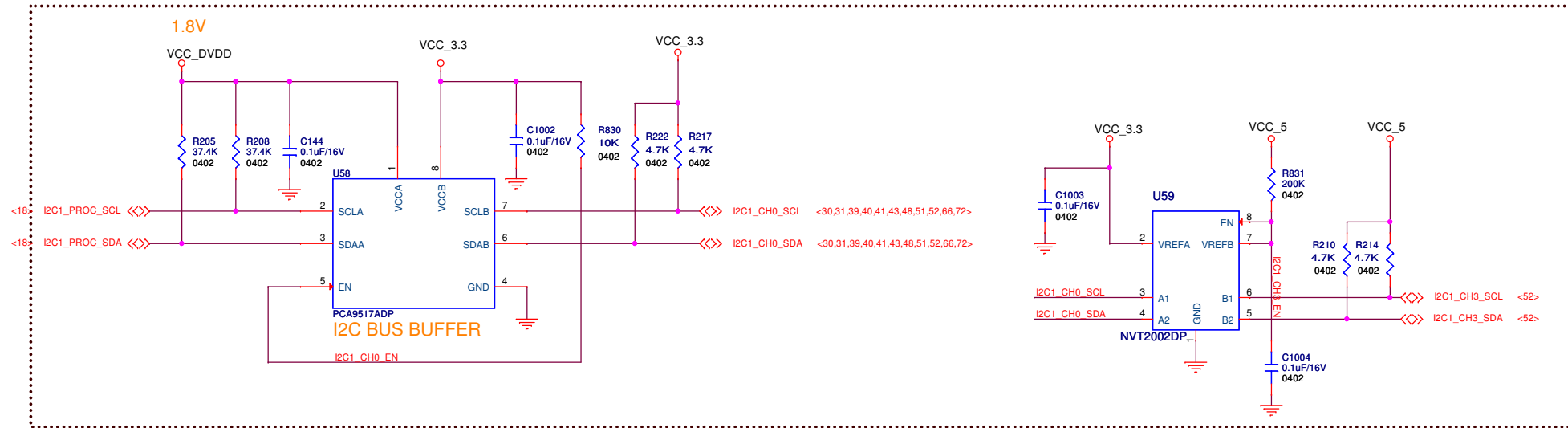
VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ (2)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (3)	✓ (3)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓ (7)

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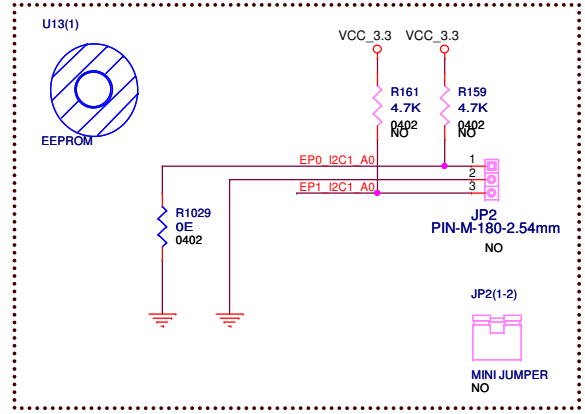
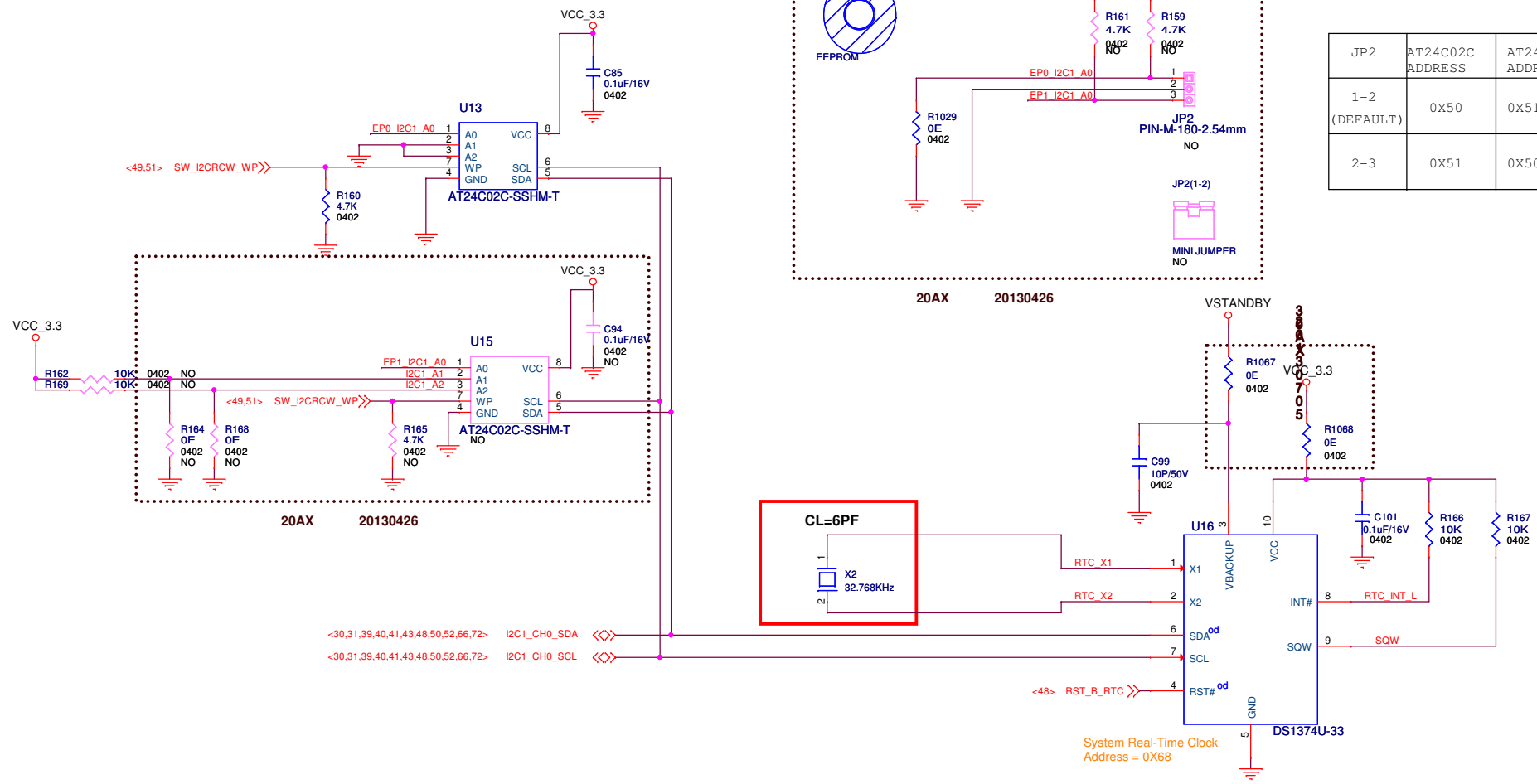
**CPLD PART2**

Size: Document Number  
Customer: 4BS05640C1X10 Rev: 30BX

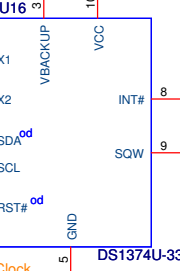
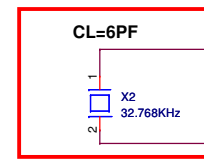
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Title: <b>I2C Bus buffer</b>		
Size: 4BS05640C1X10	Document Number: 4BS05640C1X10	Rev: 30BX
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JP2	AT24C02C ADDRESS	AT24C02C ADDRESS
1-2 (DEFAULT)	0X50	0X51
2-3	0X51	0X50



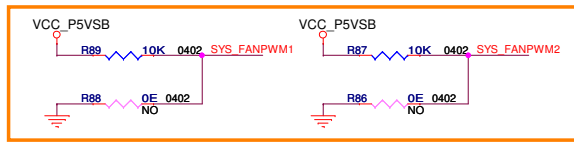
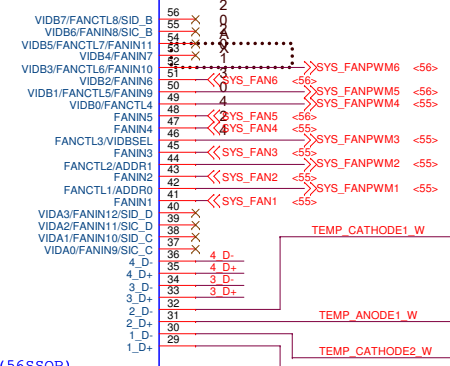
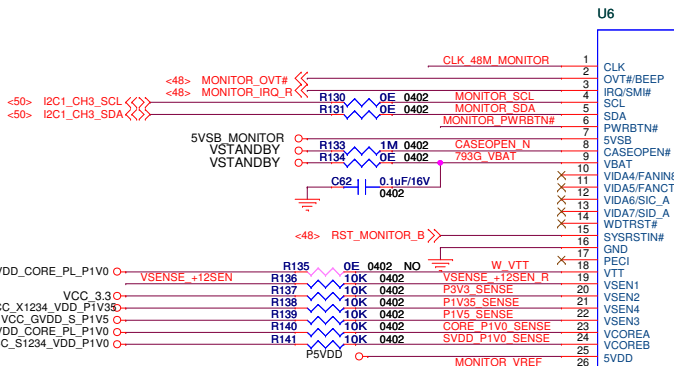
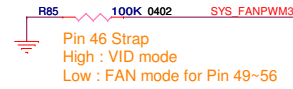
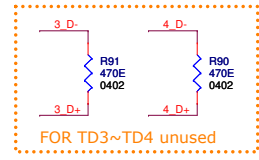
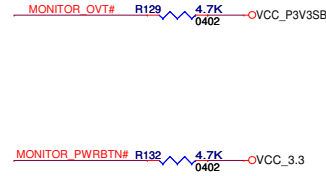
## RTC

<30,31,39,40,41,43,48,50,52,66,72> I2C1\_CH0\_SDA <<>  
 <30,31,39,40,41,43,48,50,52,66,72> I2C1\_CH0\_SCL <<>

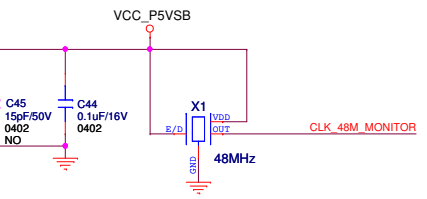
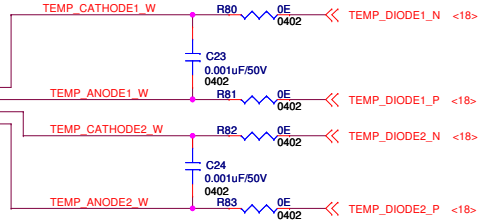
System Real-Time Clock  
 Address = 0X68

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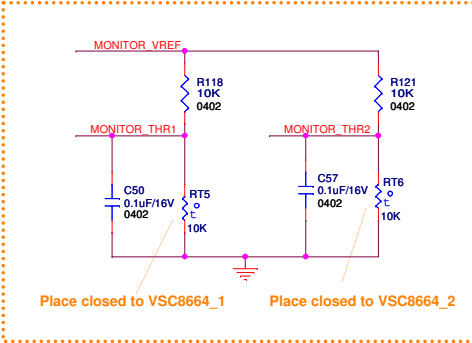
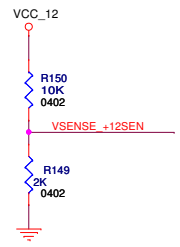
Title		
<b>I2C Devices RTC &amp; EEPROM</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	308X
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For I2C address 0X2F

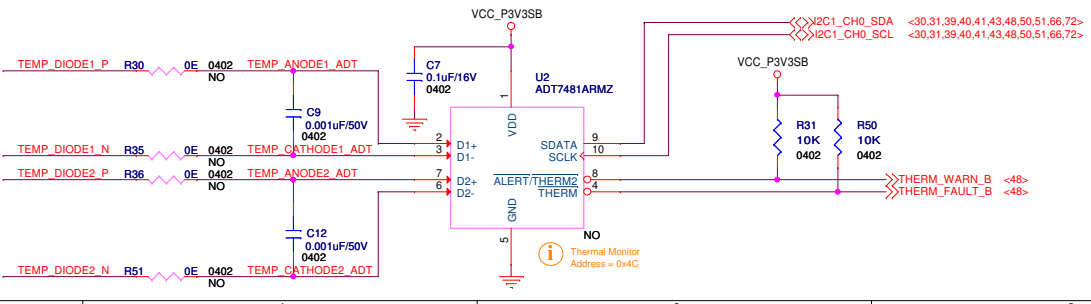


Layout Note:  
The trace between W83793(Pin1) & oscillator(output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.



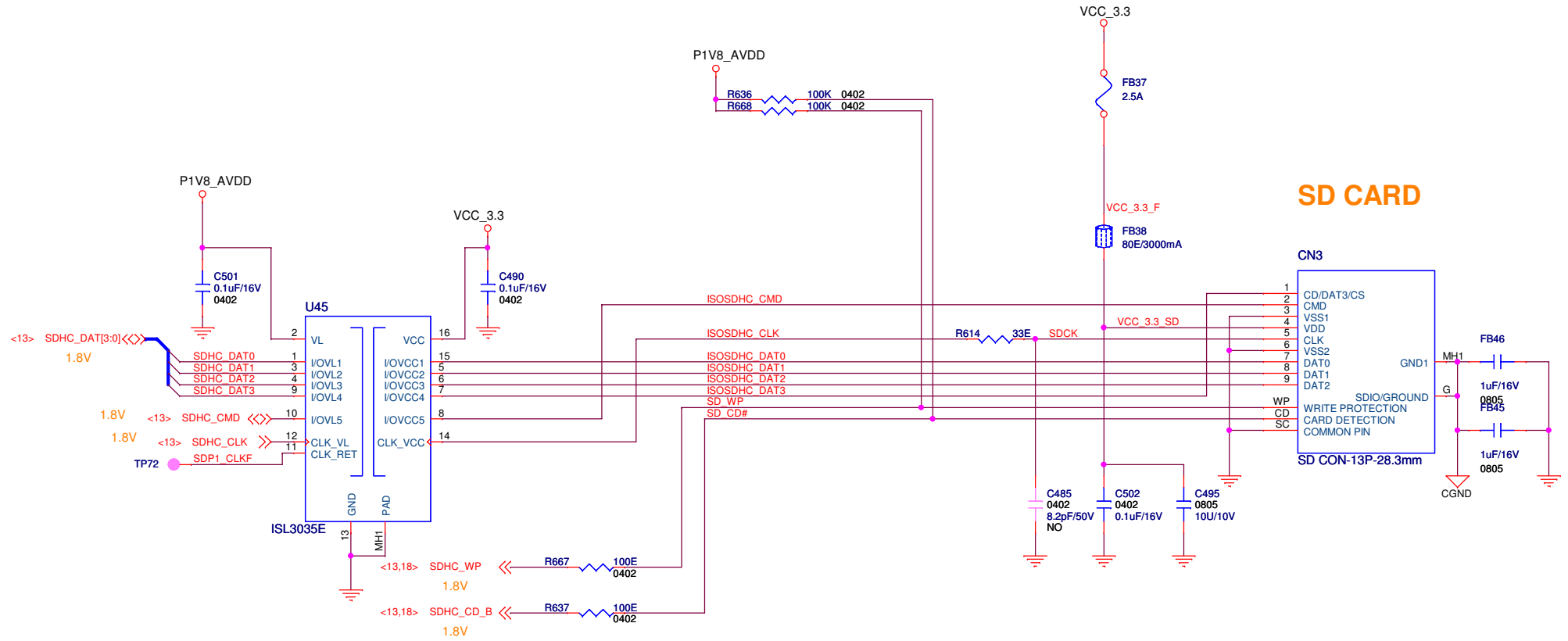
Strap I2C ADD

	FANCTL2 / A1=0	FANCTL2 / A1=1
FANCTL1 / A0=0	793G(0X58) 1_D+(0x90) 2_D+(0x98)	793G(0X5C) 1_D+(0x94) 2_D+(0x9C)
FANCTL1 / A0=1	793G(0X5A) 1_D+(0x92) 2_D+(0x9A)	793G(0X5E) 1_D+(0x96) 2_D+(0x9E)



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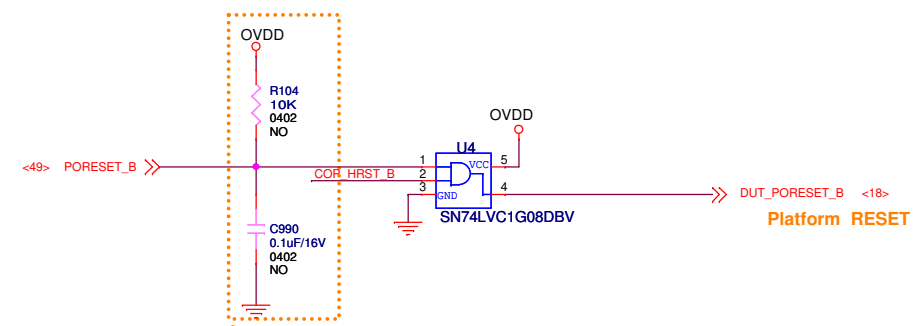
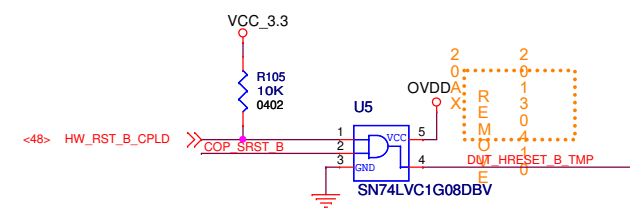
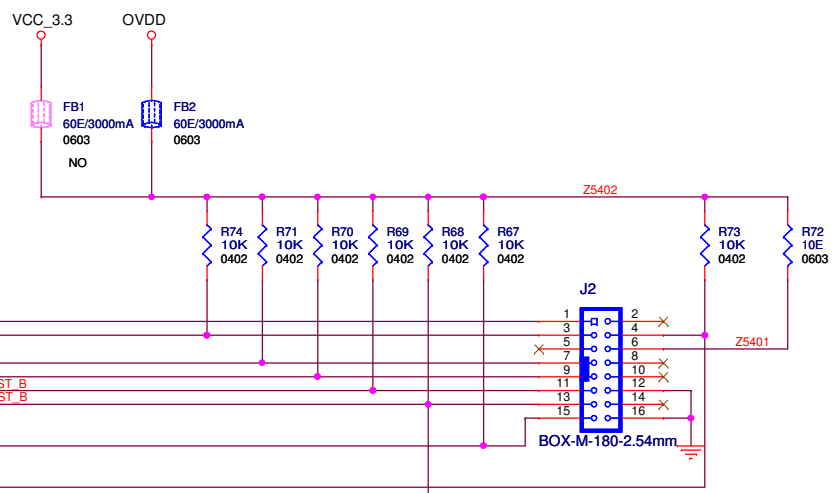
Title		I2C Devices 2
Size	Document Number	Rev
Customer	4BS05640C1X10	808X
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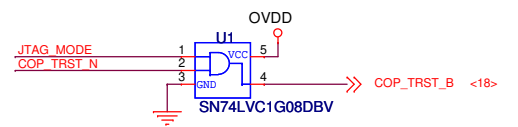
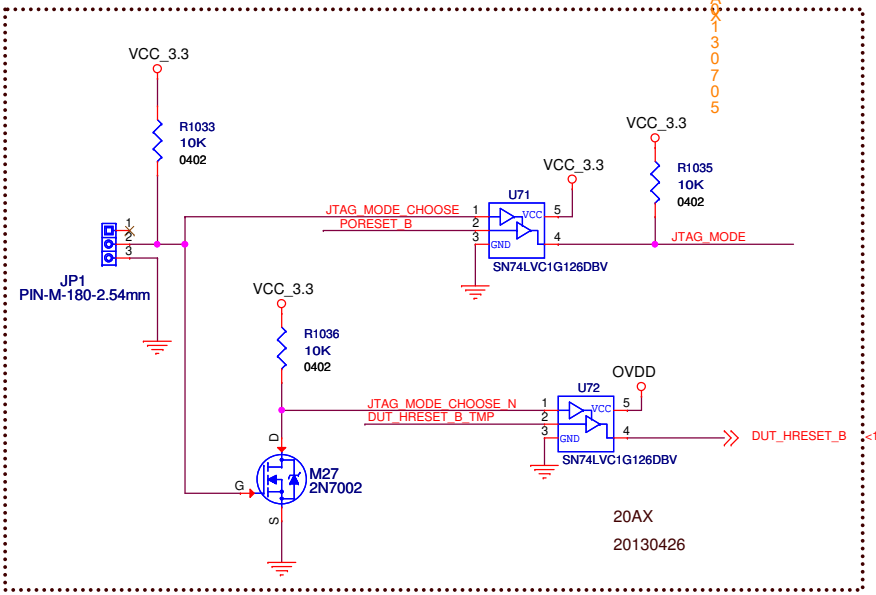
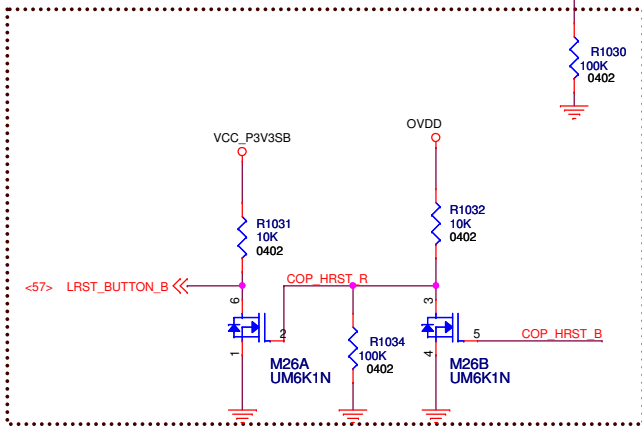
**NOTE:** Even though SDHC cards can be commanded to change operating voltage to 1.8V, it must power up at 3.3V which is not compatible with the T4240 IO levels, so translation is required.

CD and WP are also added to the RSVD pins on T4 that are powered from OVDD (1.8V).

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Title <b>SDHC SLOT</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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If the JTAG interface and COP header will not be used  
No pull-up/pull-down is required for TDI, TMS or TDO  
& JTAG JUMPER to 1-2



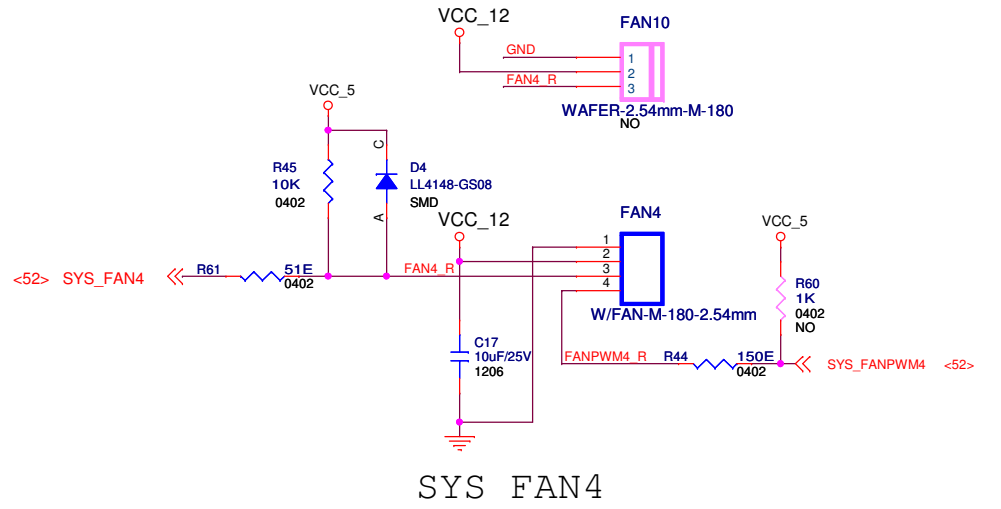
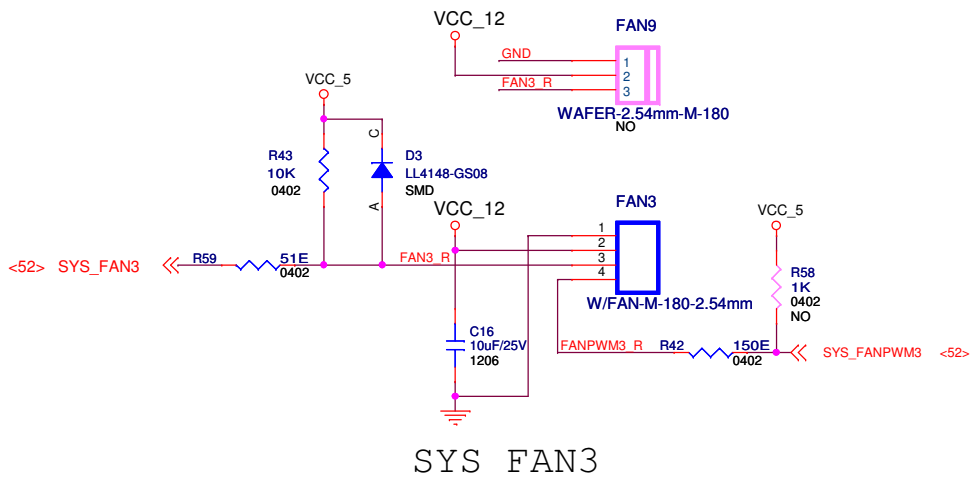
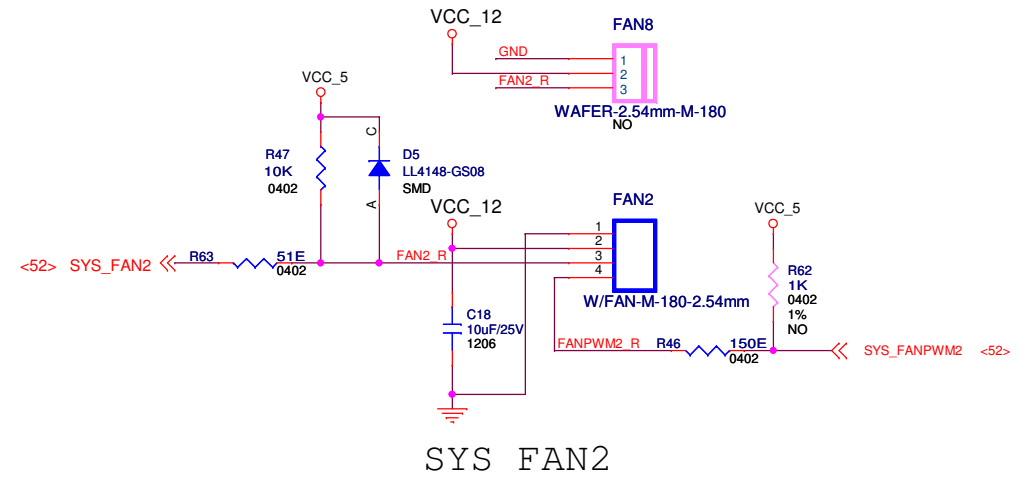
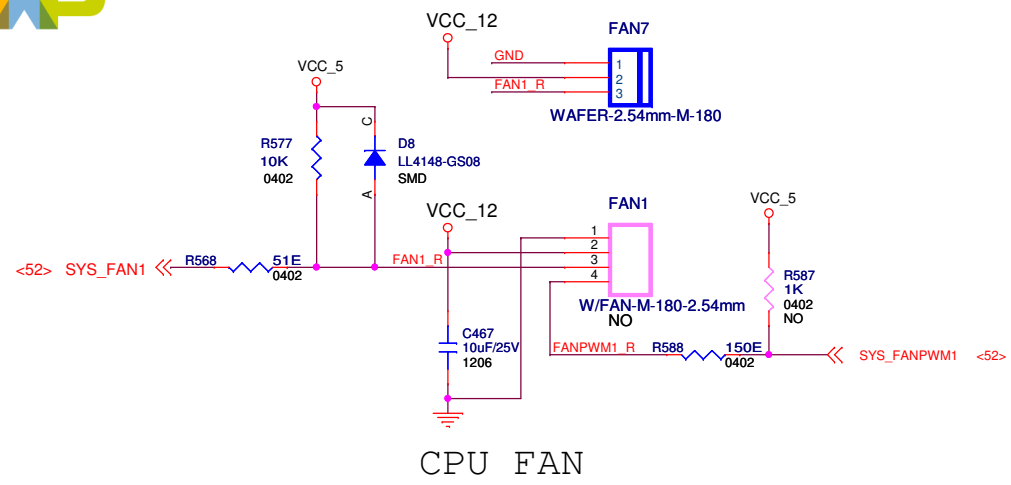
20AX  
20130426

20AX  
20130426

JP1(1-2)  
MINI JUMPER

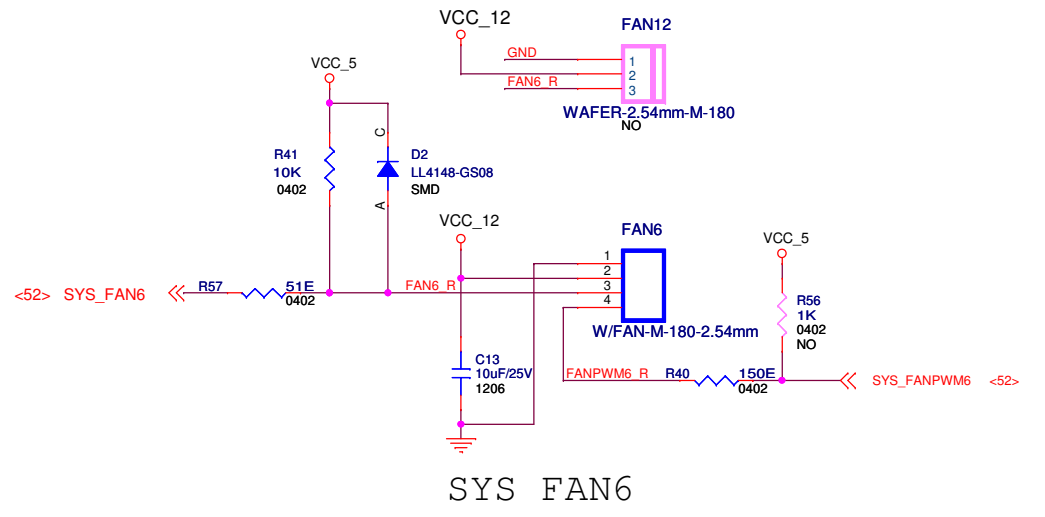
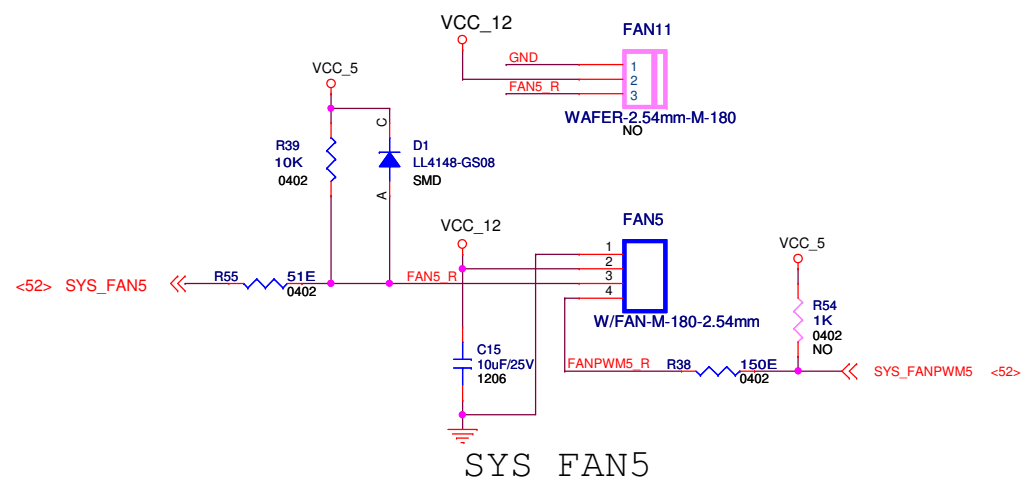
JP1	
JTAG MODE CHOOSE	
1-2	NORMAL MODE (DEFAULT)
2-3	JTAG MODE

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Title <b>COP(JTAG)</b>		
Size	Document Number	Rev
Custom	<b>4BS05640C1X10</b>	<b>30BX</b>
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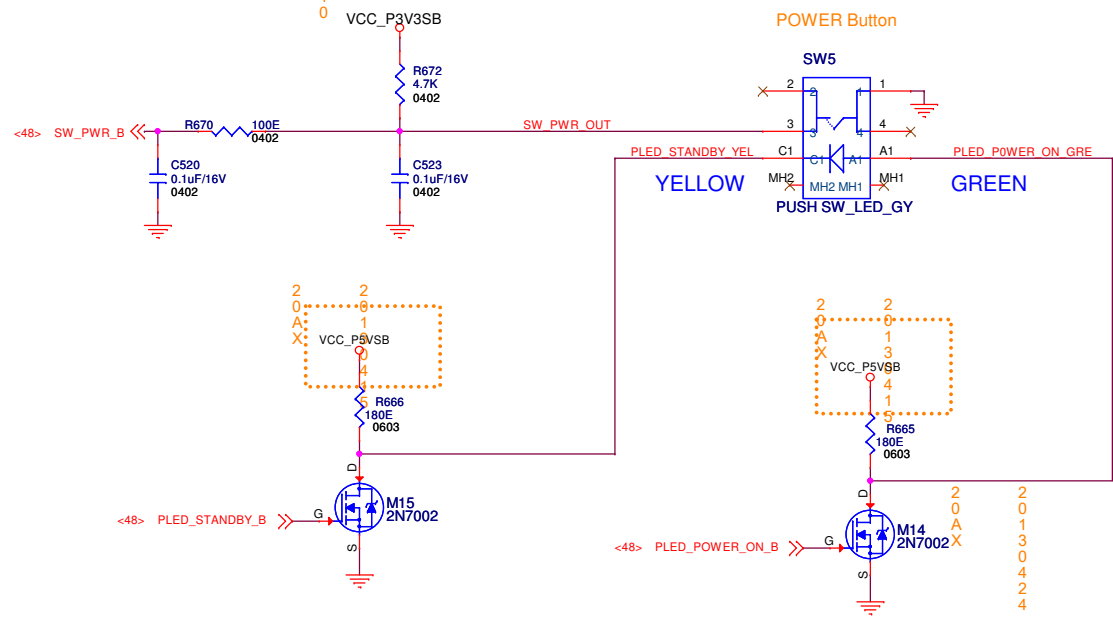
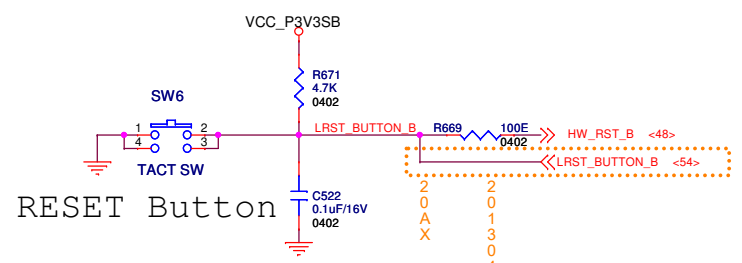
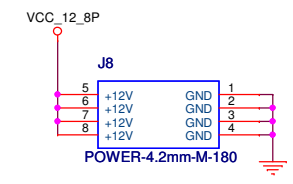
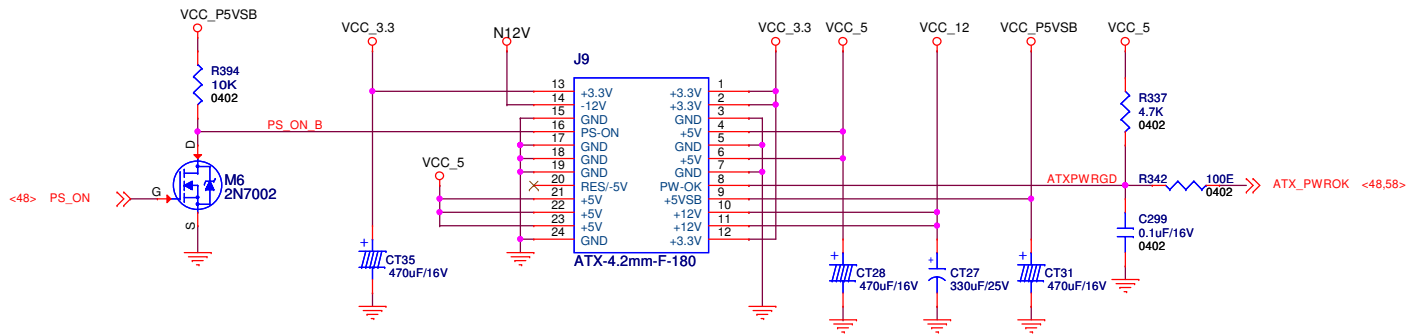
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Title		
<b>SYS FAN 1-4</b>		
Size	Document Number	Rev
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		<b>Title</b> <b>SYS FAN 5-6</b>	
<b>Size</b> B	<b>Document Number</b> <b>4BS05640C1X10</b>	<b>Rev</b> 30BX	
<b>Date:</b> Friday, August 16, 2013		<b>Sheet</b> 56 <b>of</b> 86	

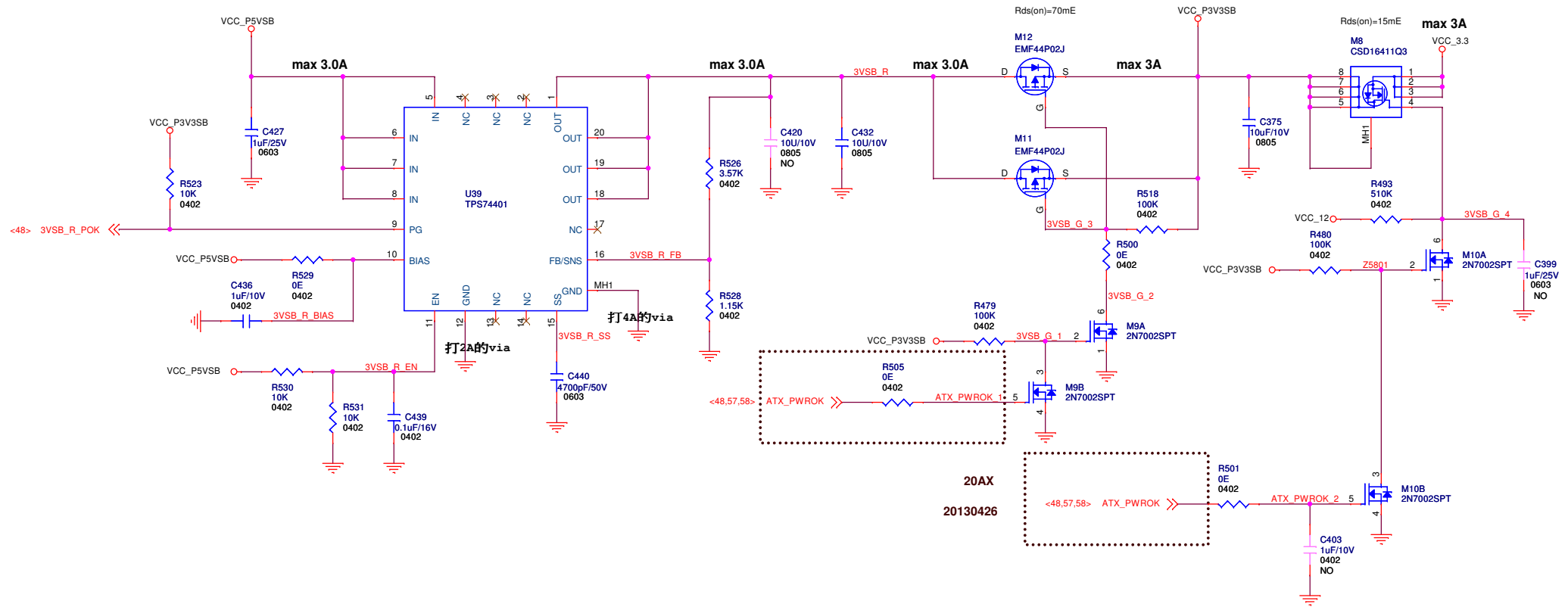




	PLED_STANDBY_B	PLED_POWER_ON_B
YELLOW	0	1
GREEN	1	0
X	1	1
X	0	0

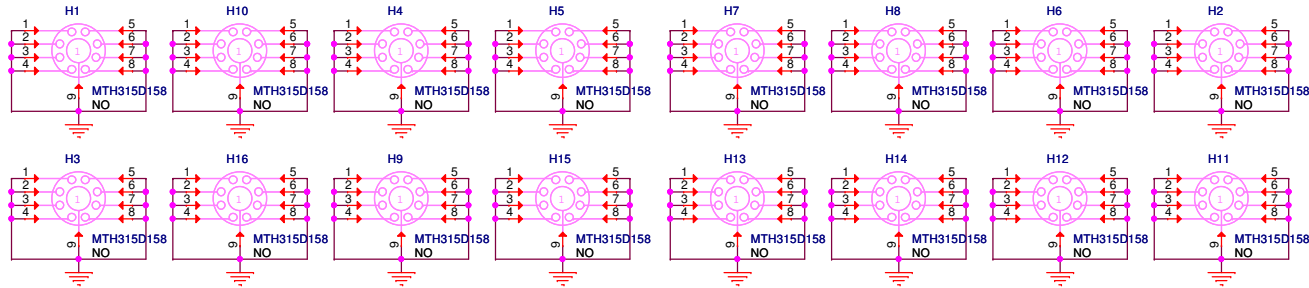
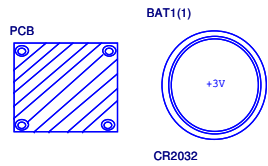
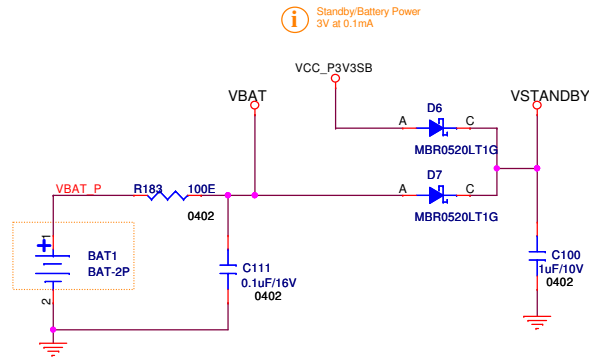
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Title <b>Power CON, Chassis I/O</b>		
Size	Document Number	Rev
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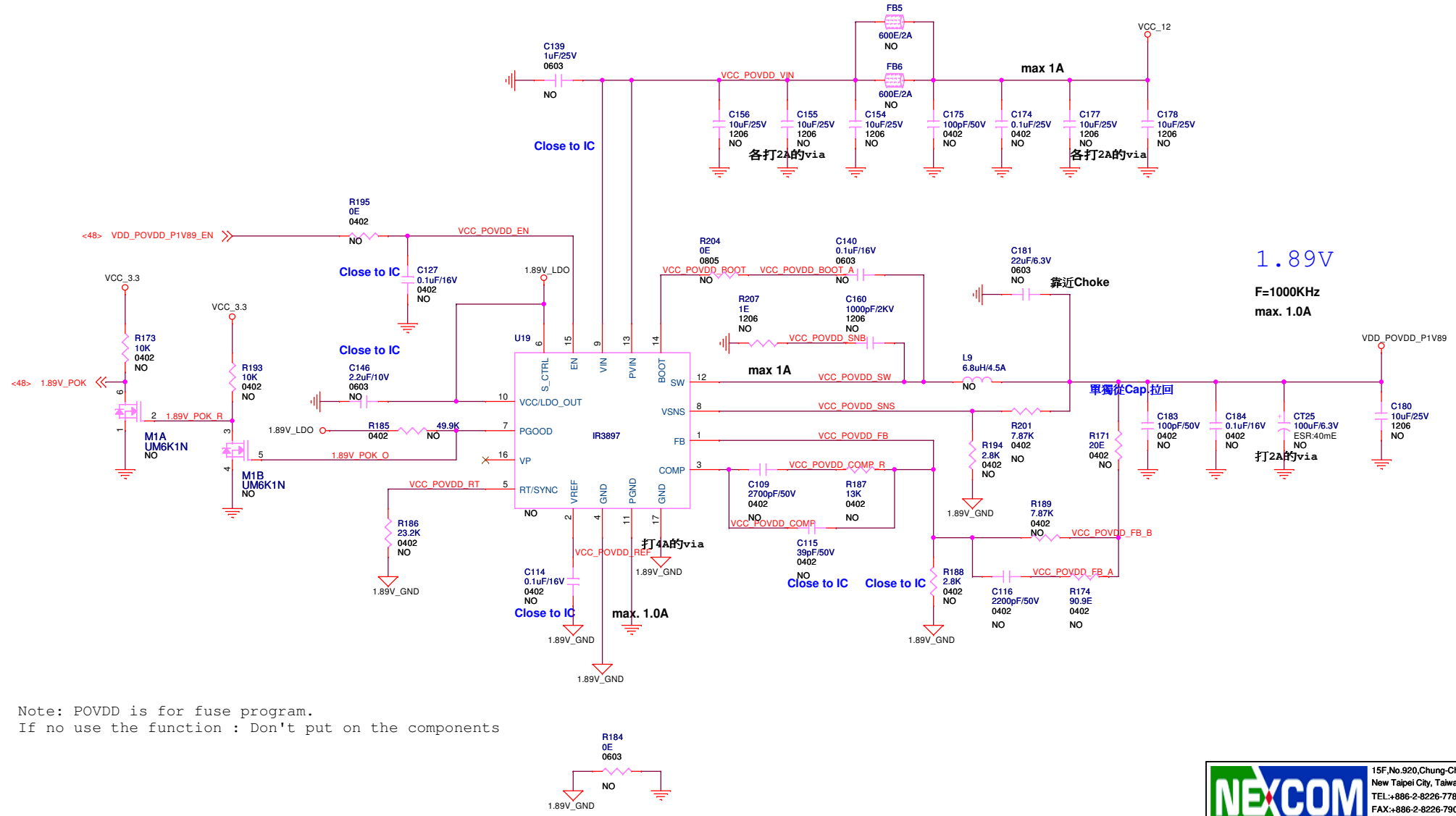
		15F, No. 920, Chung-Cheng Road, Zhonghe Dist. New Taipei City, Taiwan 23586, R.O.C. TEL: +886-2-8226-7786 FAX: +886-2-8226-7906 http://www.nexcom.com.tw	
Title <b>3.3VSB</b>			
Size A3	Document Number <b>4BS05640C1X10</b>		Rev 30BX
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### Standby/Hot\_Power/Battery



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		Title <b>1.2V StandbyPower, Battery</b>	
Size	Document Number	Rev	
Customer	<b>4BS05640C1X10</b>	30BX	
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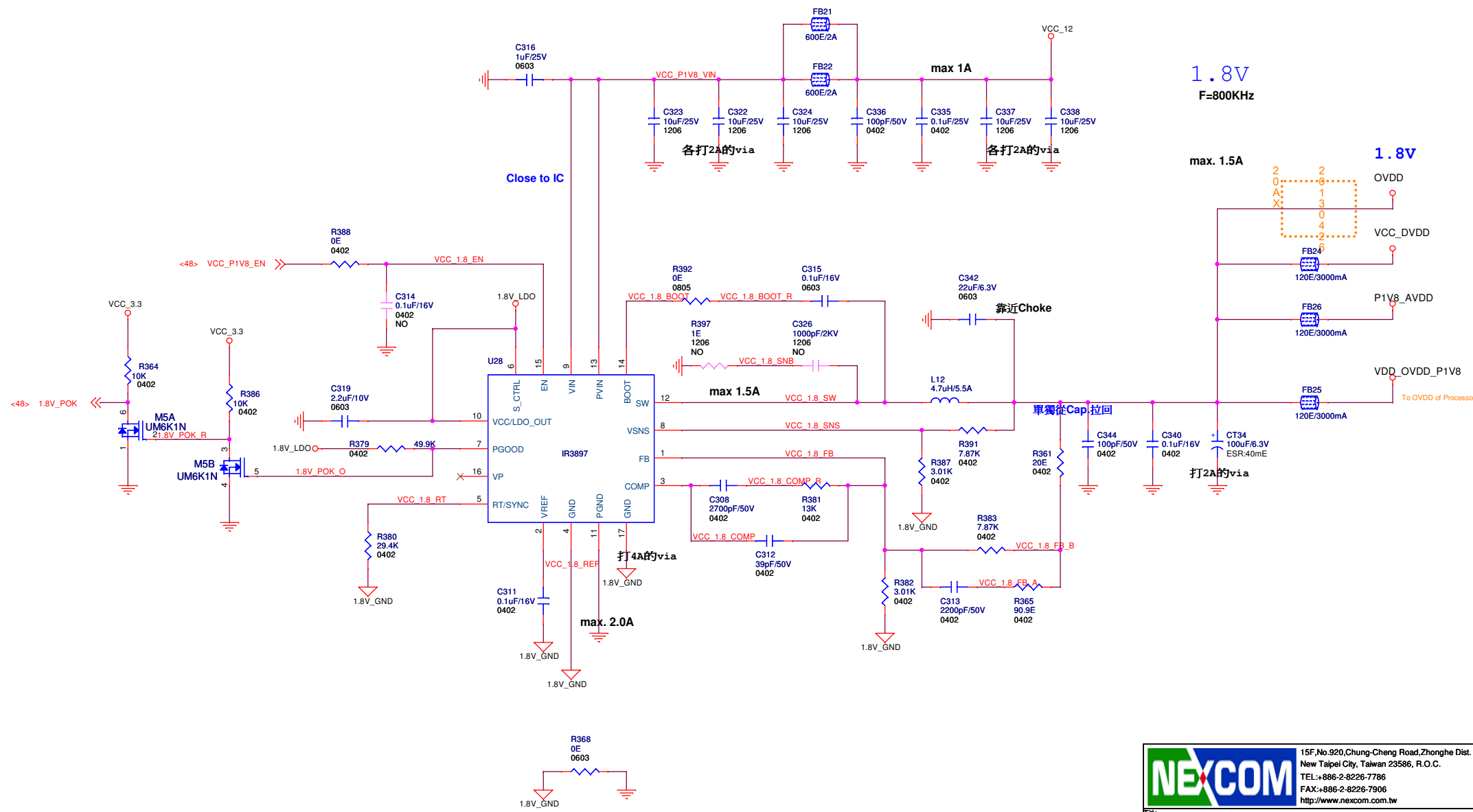




Note: POVDD is for fuse program.  
 If no use the function : Don't put on the components

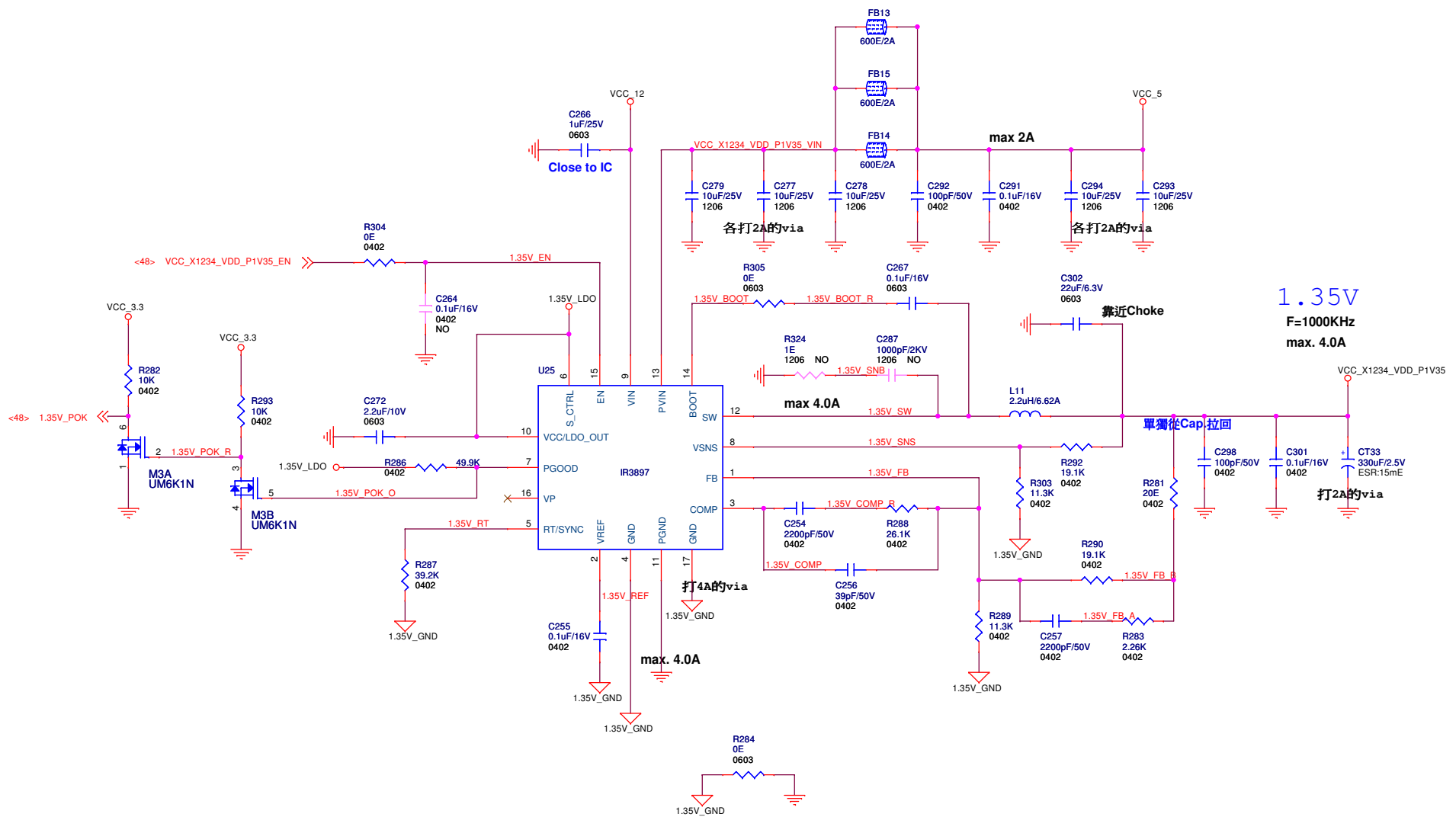
		15F, No. 920, Chung-Cheng Road, Zhonghe Dist. New Taipei City, Taiwan 23586, R.O.C. TEL: +886-2-8226-7786 FAX: +886-2-8226-7906 http://www.nexcom.com.tw
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Title <b>1.89V</b>		
Size	Document Number	Rev
Customer	<b>4BS05640C1X10</b>	30BX
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Title		
1.8V		
Size	Document Number	Rev
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Title		
1.35V		
Size	Document Number	Rev
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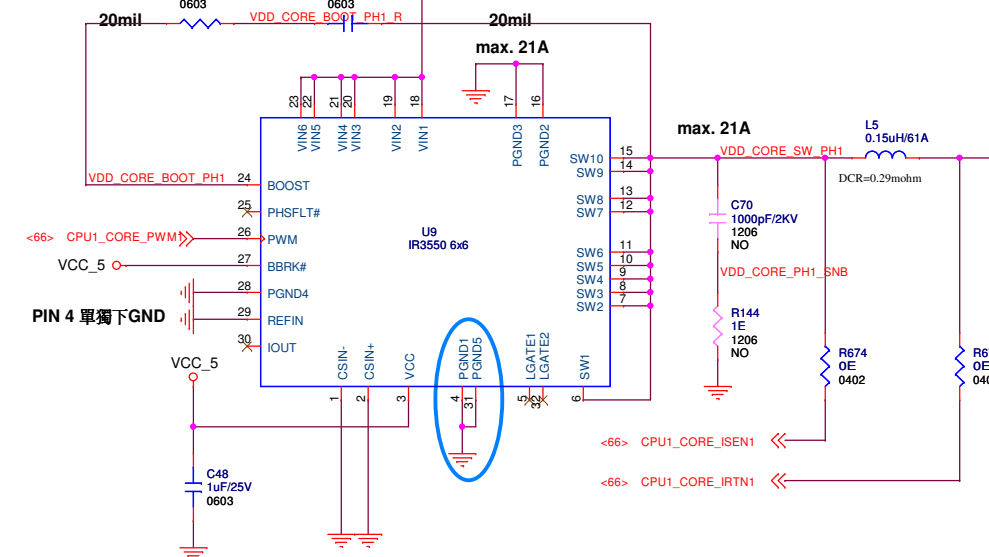






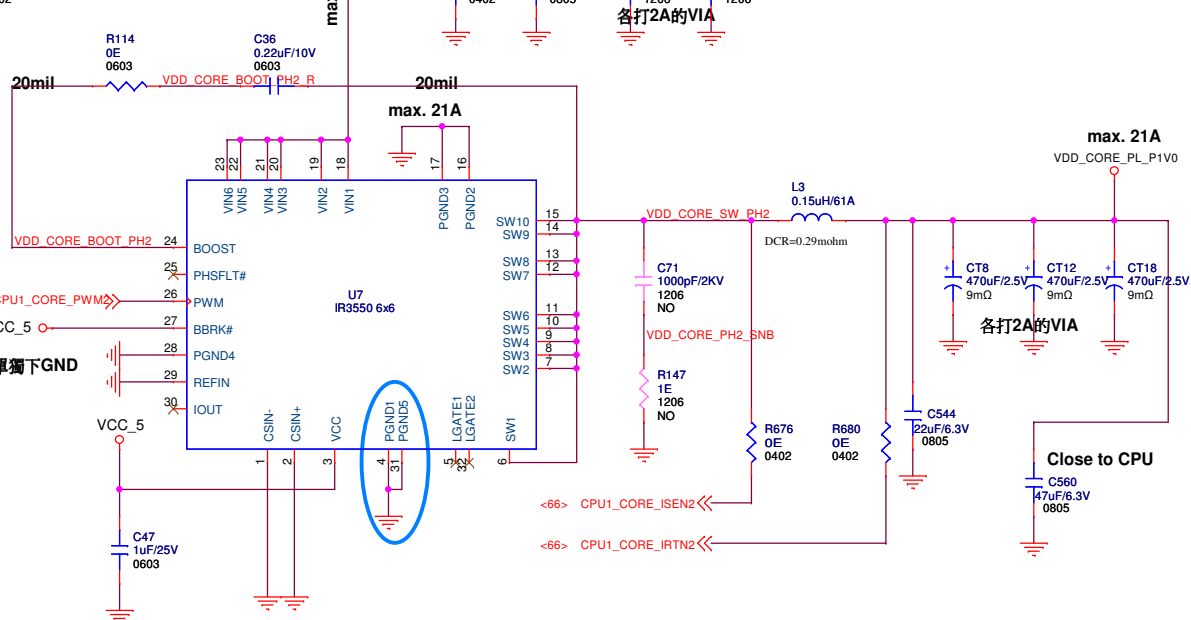


# Phase1



If no using CSIN+/CSIN- function, pin31 can connect to ground directly.  
 If using CSIN+/CSIN- function, pin31 should be floating.

# Phase2

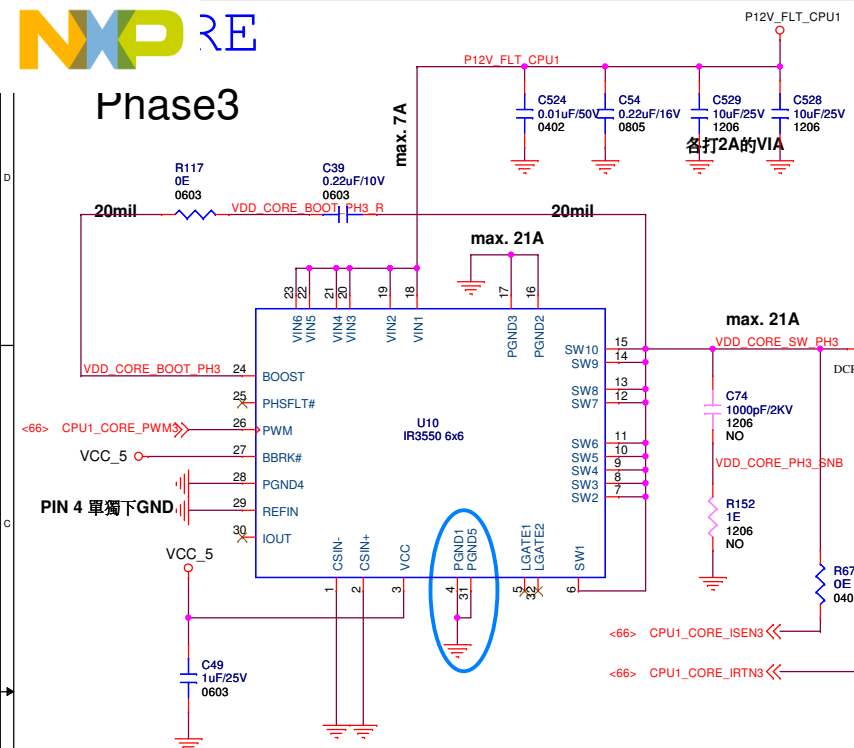


If no using CSIN+/CSIN- function, pin31 can connect to ground directly.  
 If using CSIN+/CSIN- function, pin31 should be floating.

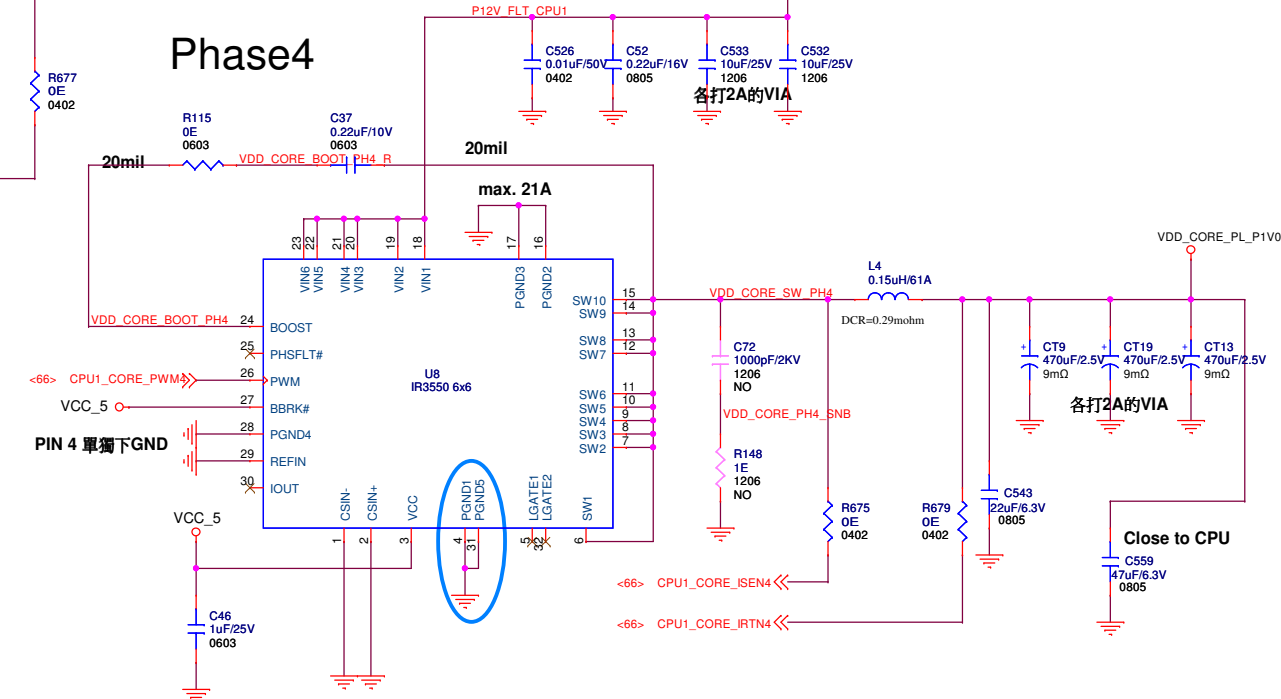
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Title		
1V VCORE PHASE 12		
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# Phase3



# Phase4



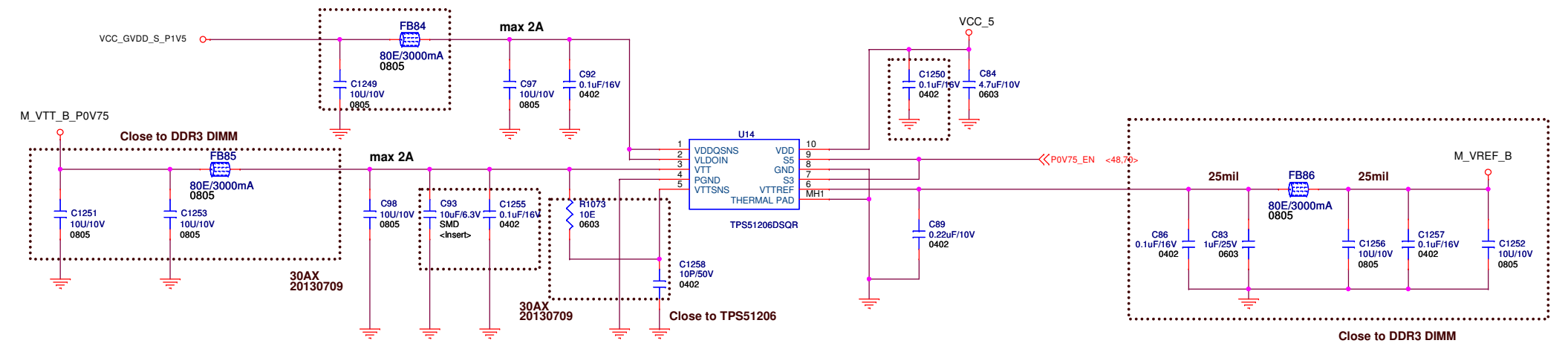
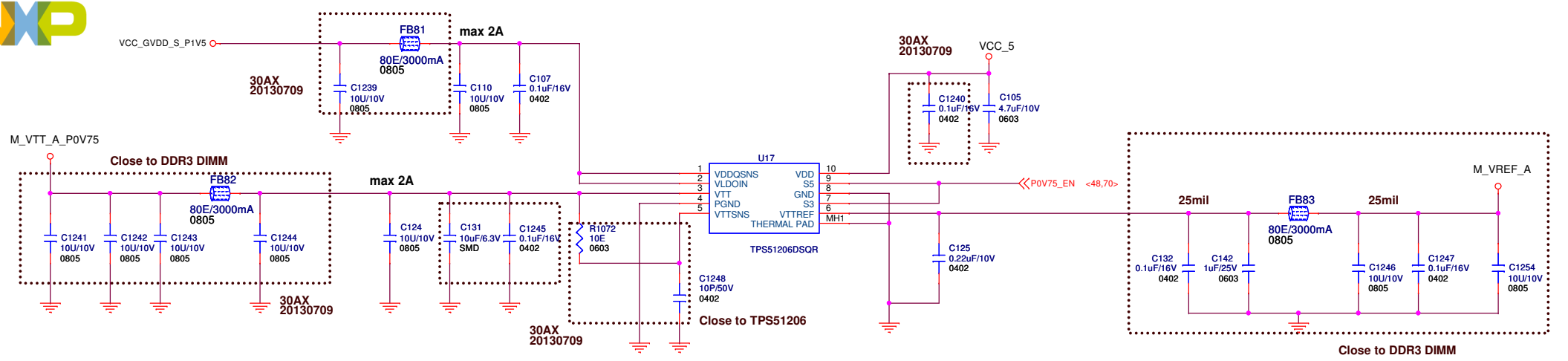
If no using CSIN+/CSIN- function, pin31 can connect to ground directly.  
 If using CSIN+/CSIN- function, pin31 should be floating.

If no using CSIN+/CSIN- function, pin31 can connect to ground directly.  
 If using CSIN+/CSIN- function, pin31 should be floating.

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Title		
1V VCORE PHASE 34		
Size	Document Number	Rev
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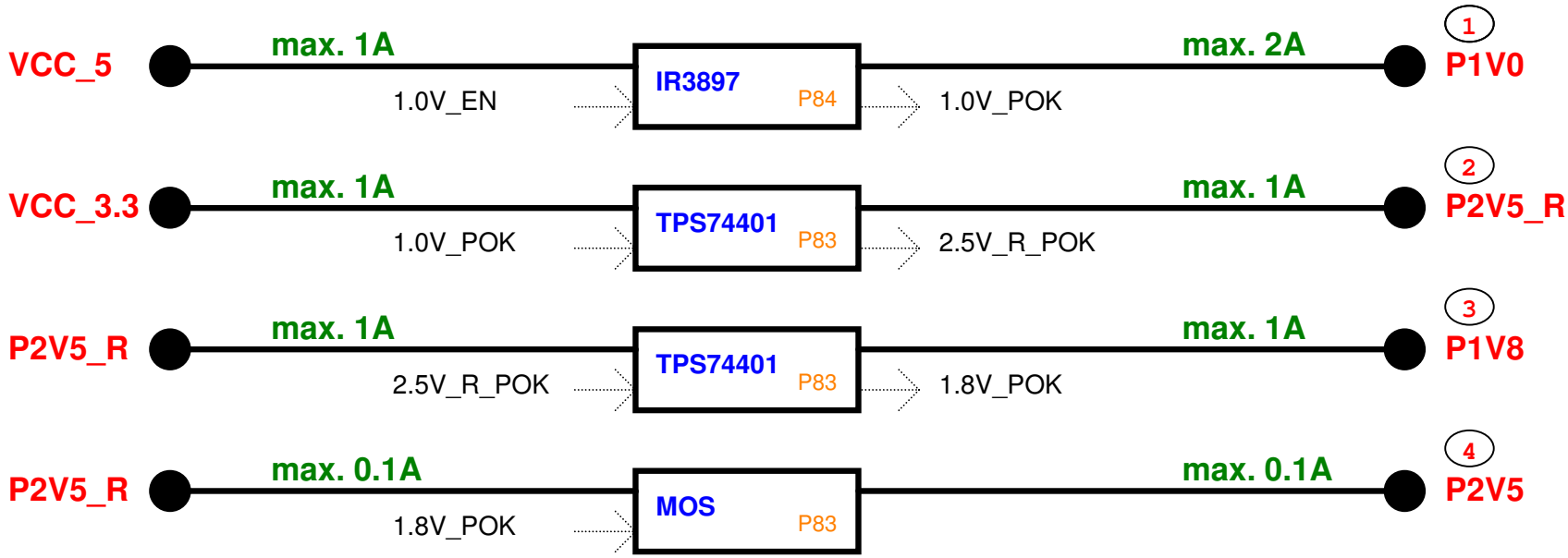




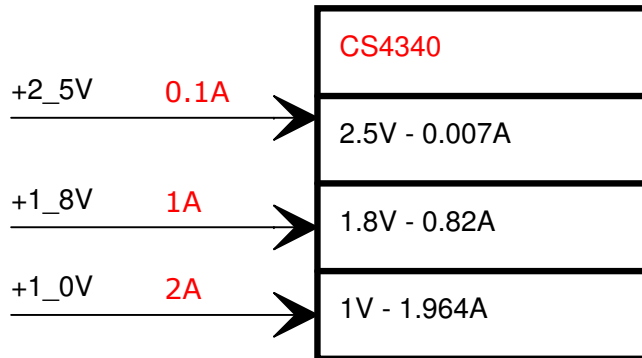
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0_75V		
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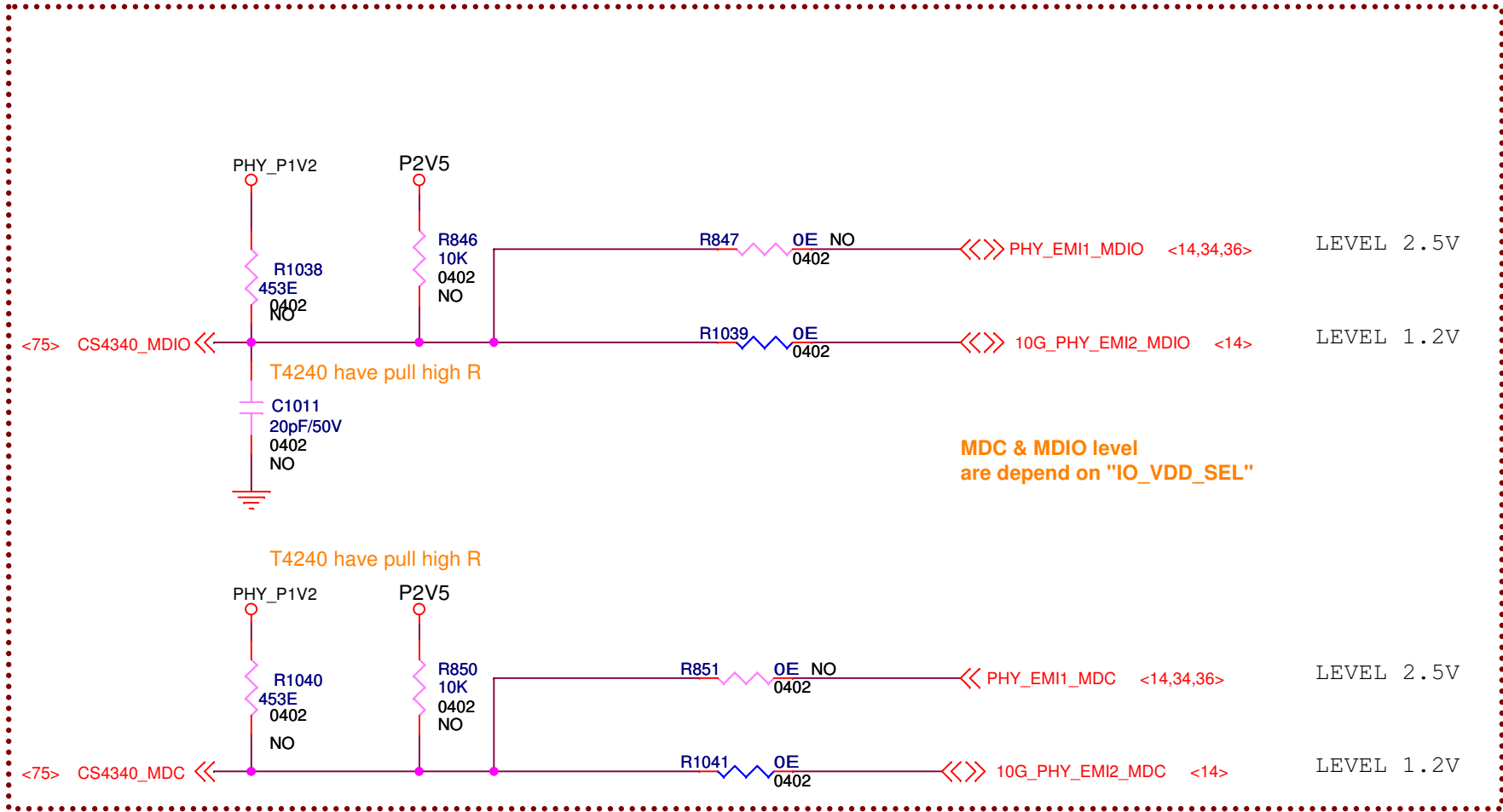
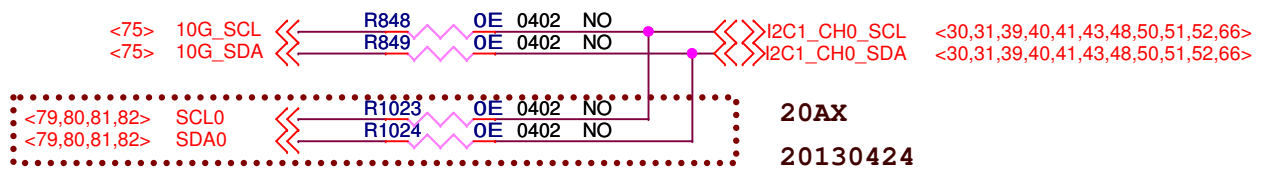
# Power Delivery & Sequence



## Max 3.5W



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Title: <b>POWER delivery</b>			
Size A	Document Number: <b>4BS05640C1X10</b>		Rev: 30BX
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20130426



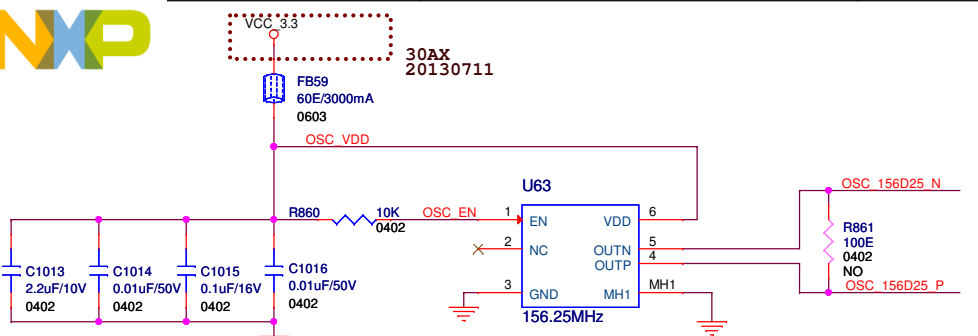
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Title		
10G_MDC/MDIO		
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A	4BS05640C1X10	30BX
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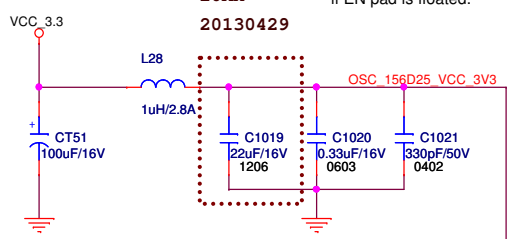




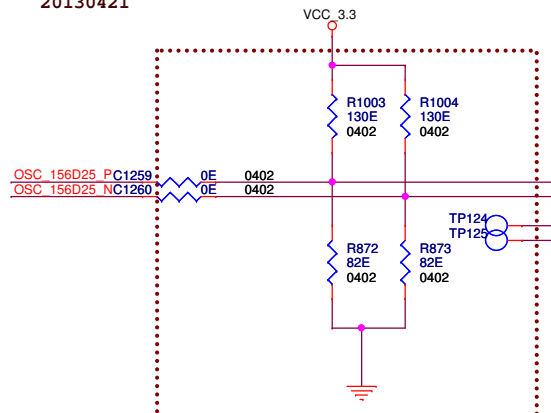
30AX  
20130711



20AX  
20130429



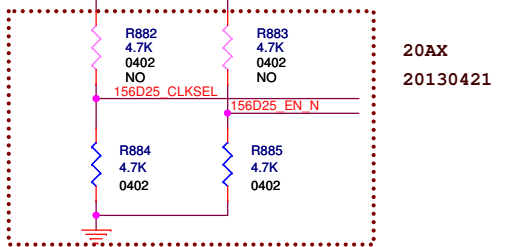
20AX  
20130421



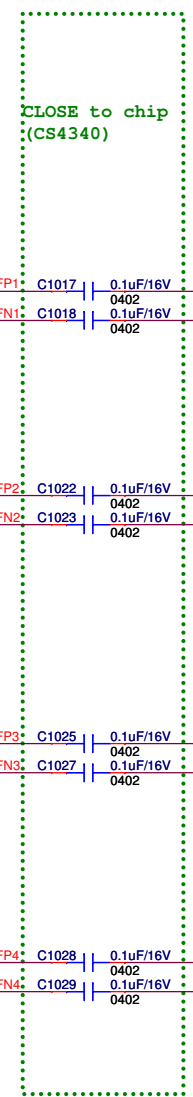
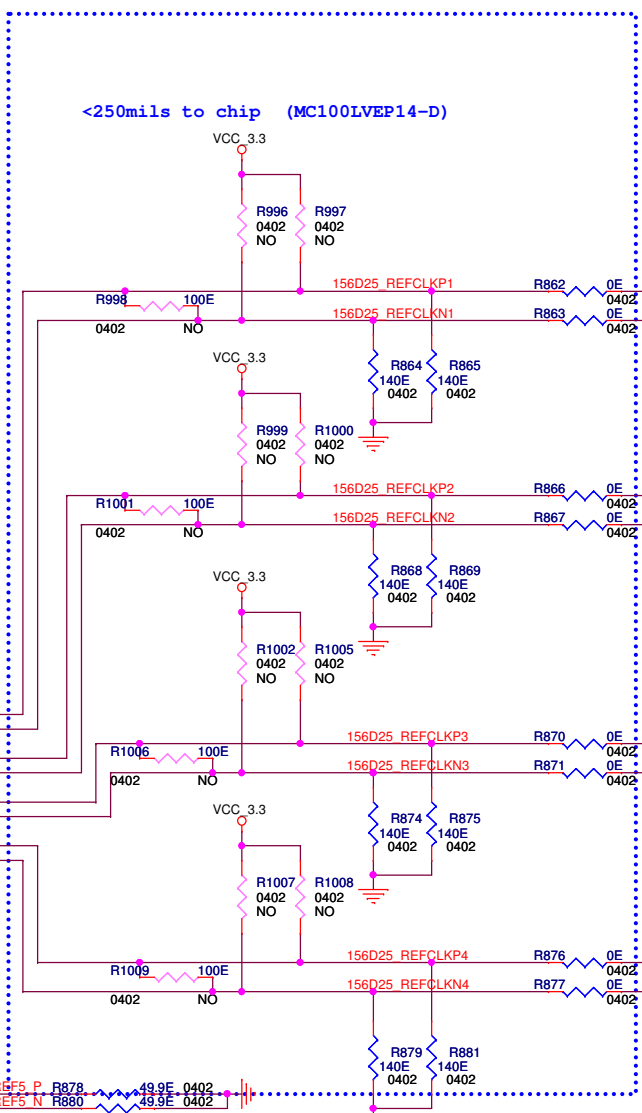
30BX  
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CLK0	CLK1	CLK_SEL	EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\*On next negative transition of CLK0 or CLK1



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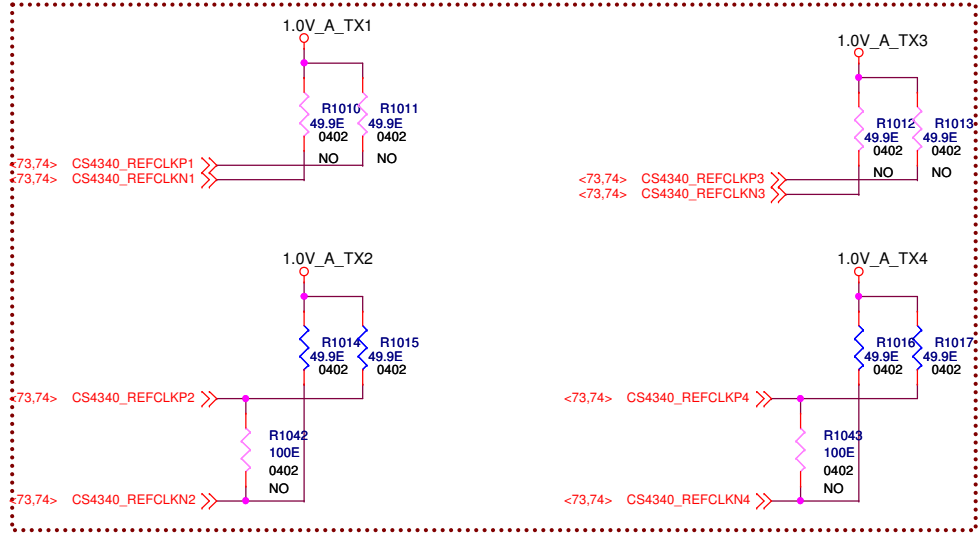
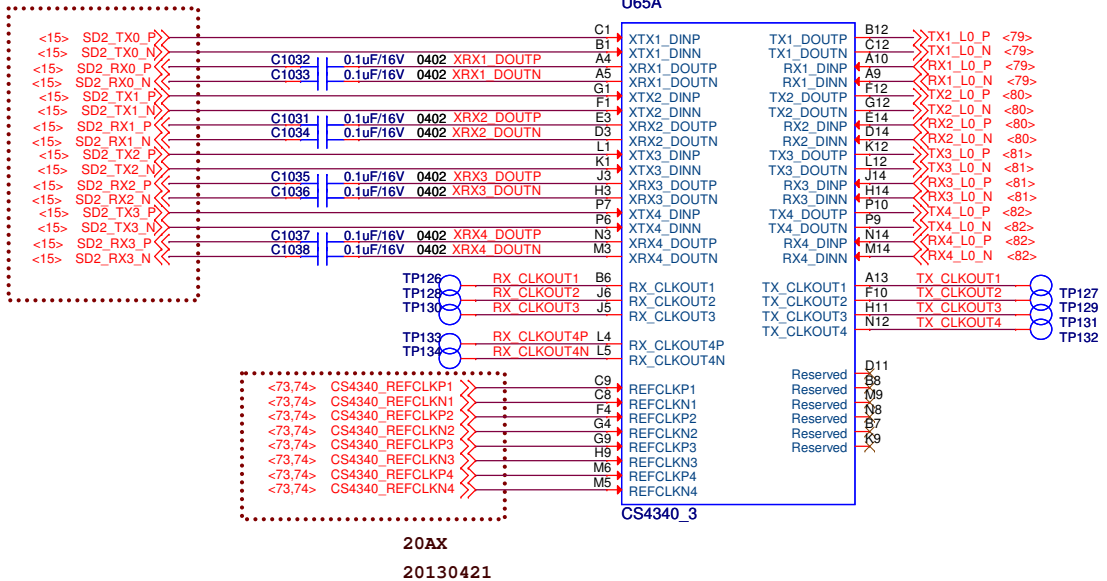


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Title		156.25MHz
Size	Document Number	Rev
B	4BS05640C1X10	30BX
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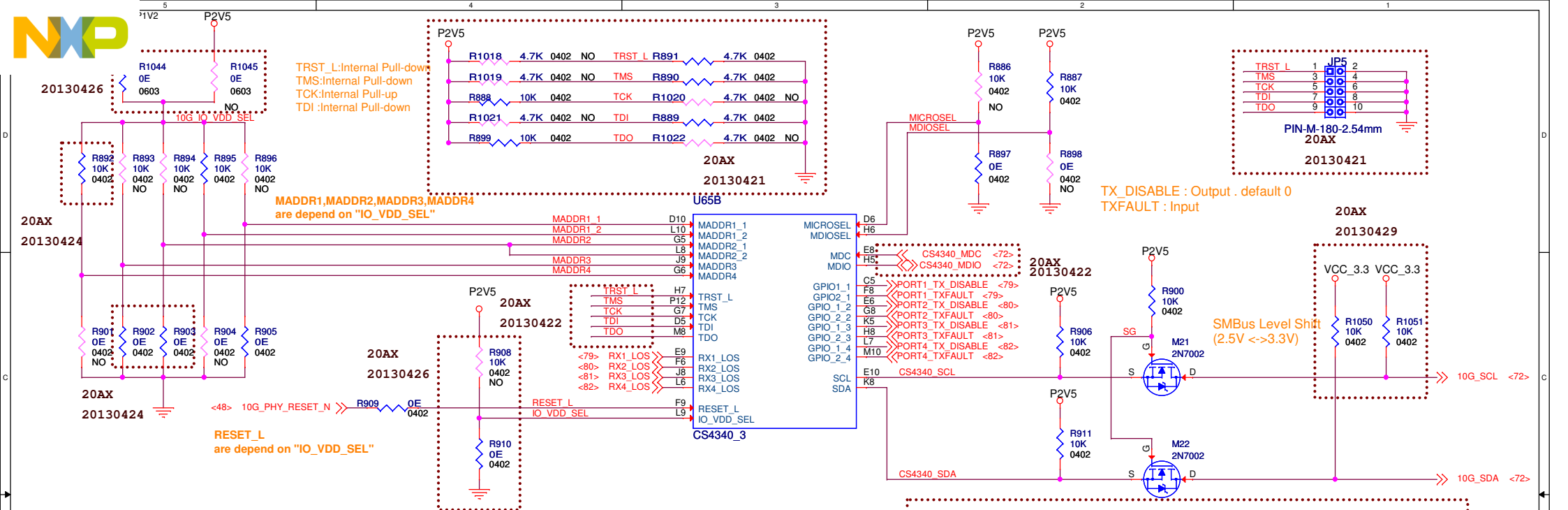


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Title <b>CS4340_XFI</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
Date: Friday, August 16, 2013	Sheet 74	of 86

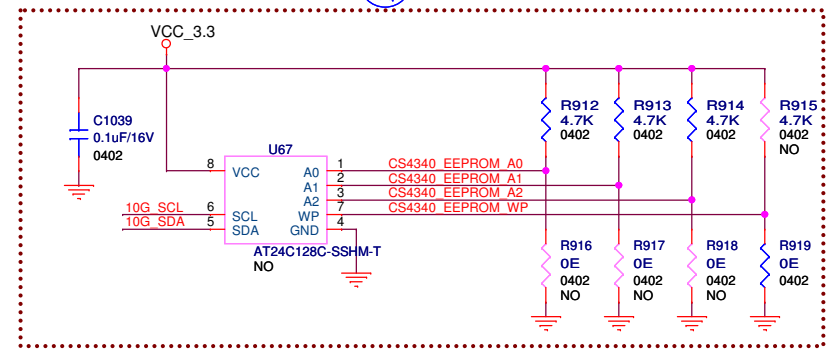


IO_VDD_SEL	L9	DC	LVC MOS Input Internal Pullup
0			MDC and MDIO operate at 1.0 V (IEEE 802.3a Clause 45 compliant)
1			MDC and MDIO operate at 1.8/2.5 V. This is the default.

Note: The I/O voltages of RESET\_L, MADDR1, MADDR2, MADDR3 and MADDR4 are also controlled by IO\_VDD\_SEL.

**Table 11 Microprocessor Interface Modes**

Mode	MICROSEL	MDIOSEL	MADDR Pin						
			MADDR0 <sup>(1)</sup>	MADDR1_1 <sup>(2)</sup>	MADDR1_2	MADDR2_1 <sup>(3)</sup>	MADDR2_2	MADDR3	MADDR4
MDIO <sup>(4)</sup>	0	1	PRTAD[0] hardwired inside the package	PRTAD[1] Tie to VSS	PRTAD[1] Tie to VDD	PRTAD[2] Tie together with MADDR2_2	PRTAD[2] Tie together with MADDR2_1	PRTAD[3]	PRTAD[4]
I <sup>2</sup> C <sup>(5)</sup>	1	0	slave_addr[0] hardwired inside the package	slave_addr[1] Tie to VSS	slave_addr[1] Tie to VDD	slave_addr[2] Tie together with MADDR2_2	slave_addr[2] Tie together with MADDR2_1	slave_addr[3]	slave_addr[4]
SPI	1	1	hardwired inside the package	chip select, device #1 (active low)	chip select, device #3 (active low)	chip select, device #2 (active low)	chip select, device #4 (active low)	MOSI	X



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Title <b>CS4340_STRAP PIN</b>		
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DIGVDD:44mA

V2P5:3mA

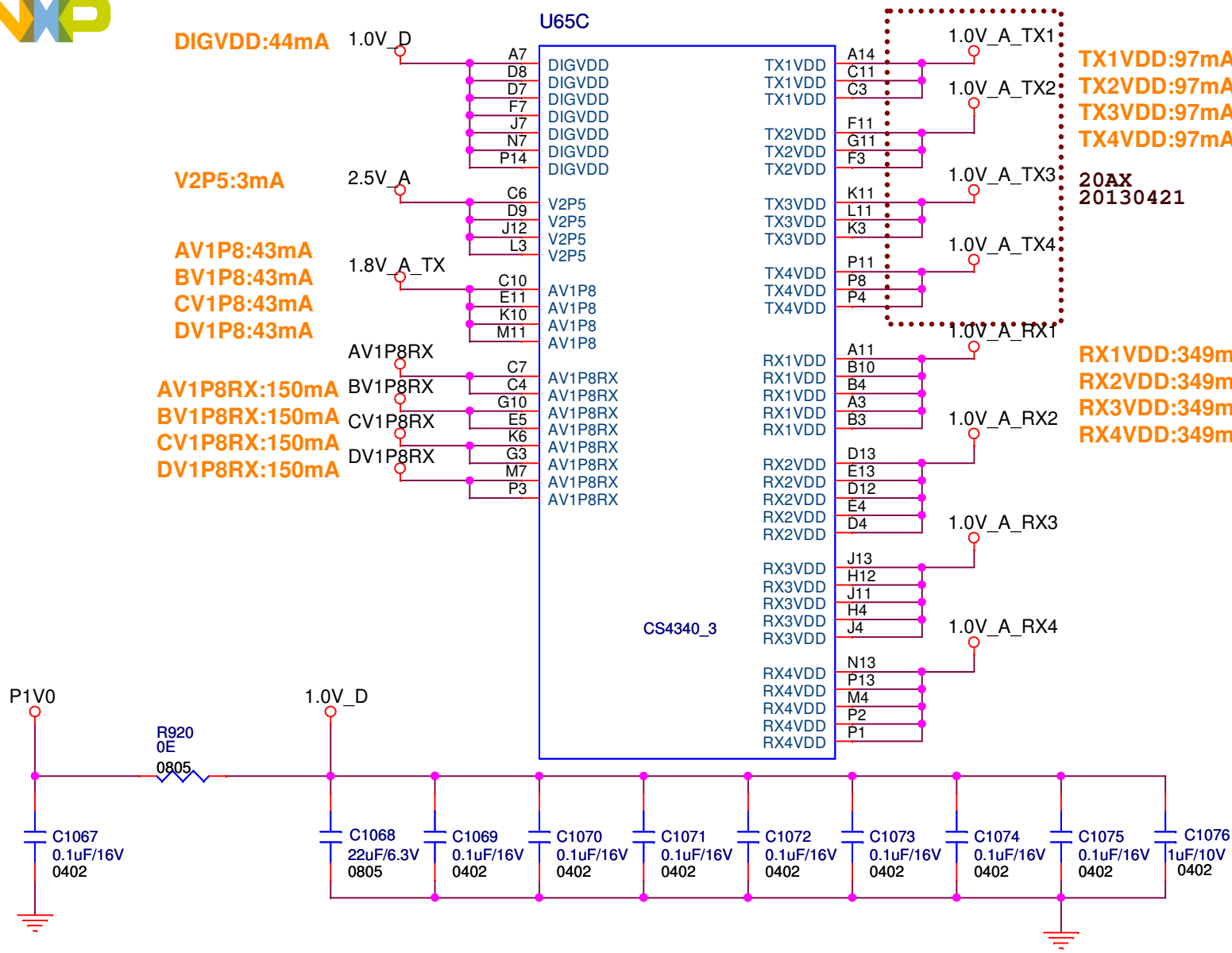
AV1P8:43mA  
BV1P8:43mA  
CV1P8:43mA  
DV1P8:43mA

AV1P8RX:150mA  
BV1P8RX:150mA  
CV1P8RX:150mA  
DV1P8RX:150mA

TX1VDD:97mA  
TX2VDD:97mA  
TX3VDD:97mA  
TX4VDD:97mA

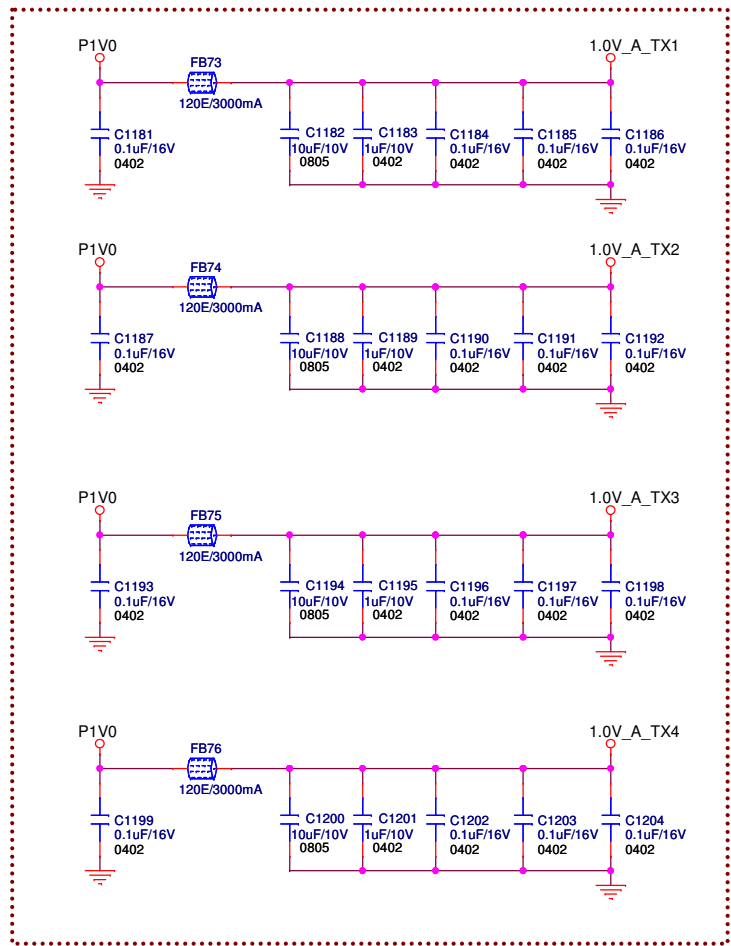
20AX  
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RX1VDD:349mA  
RX2VDD:349mA  
RX3VDD:349mA  
RX4VDD:349mA

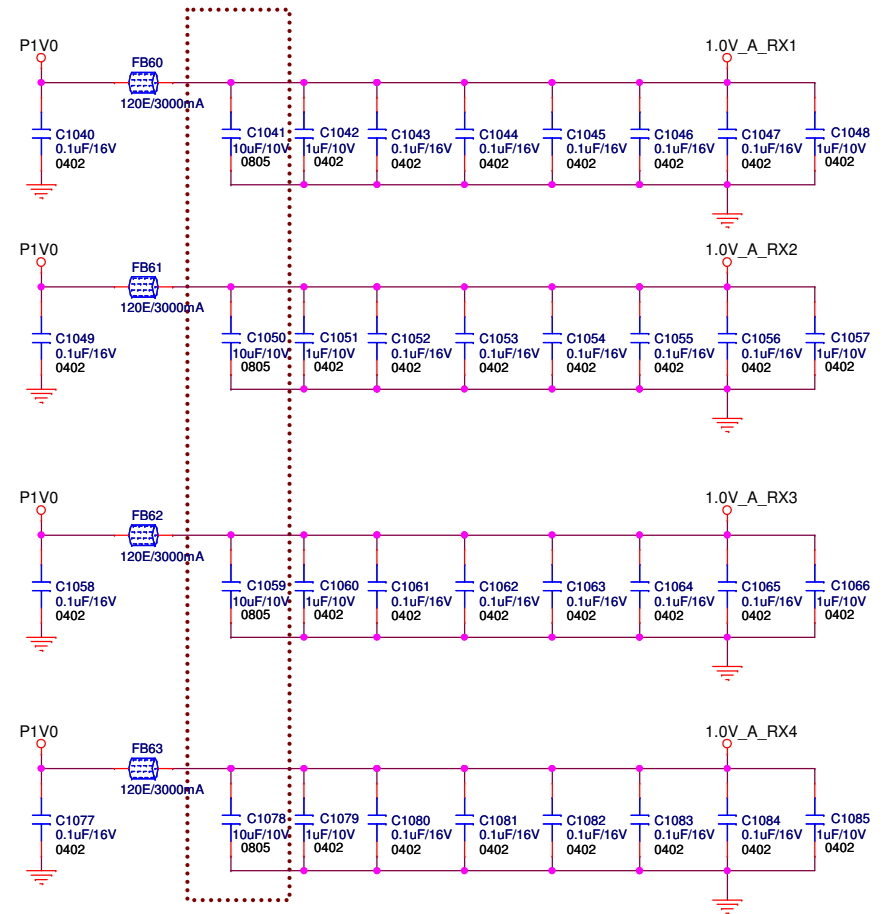



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Title		
CS4340_PWR_P1V0		
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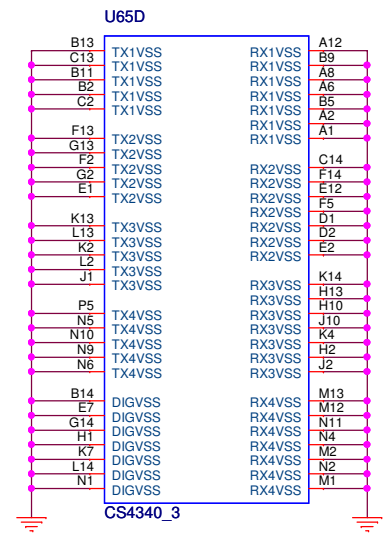
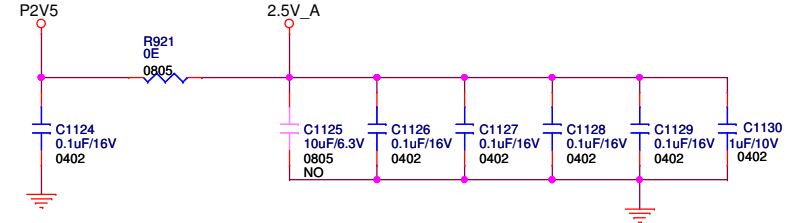
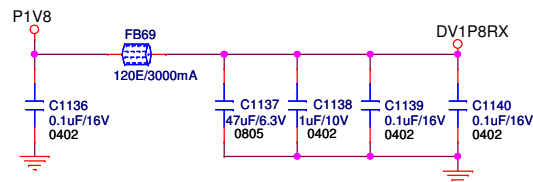
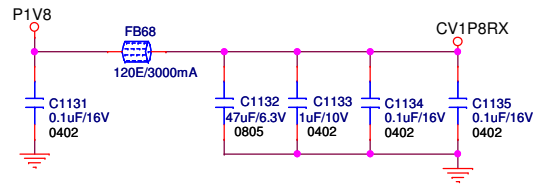
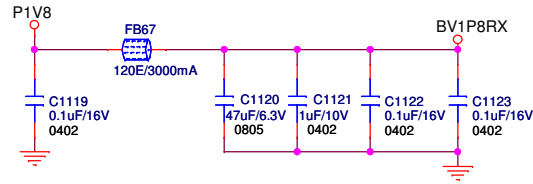
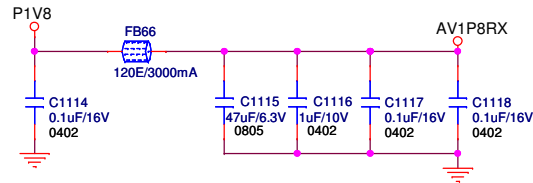
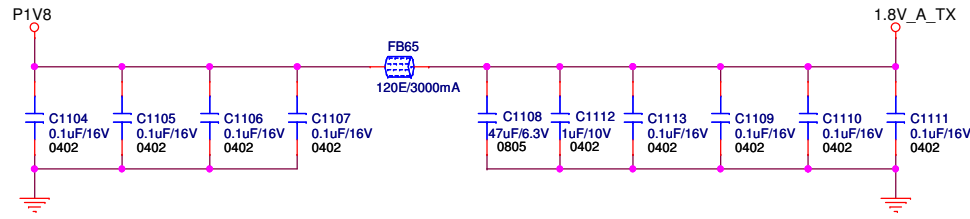


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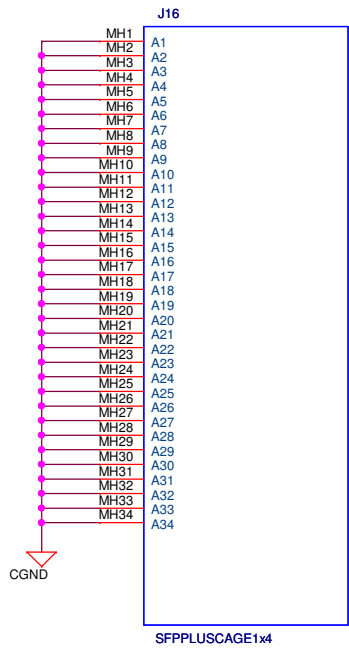
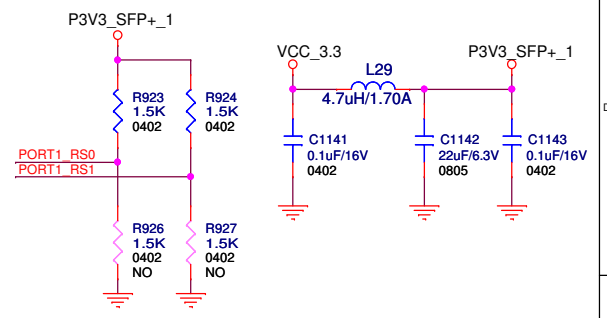
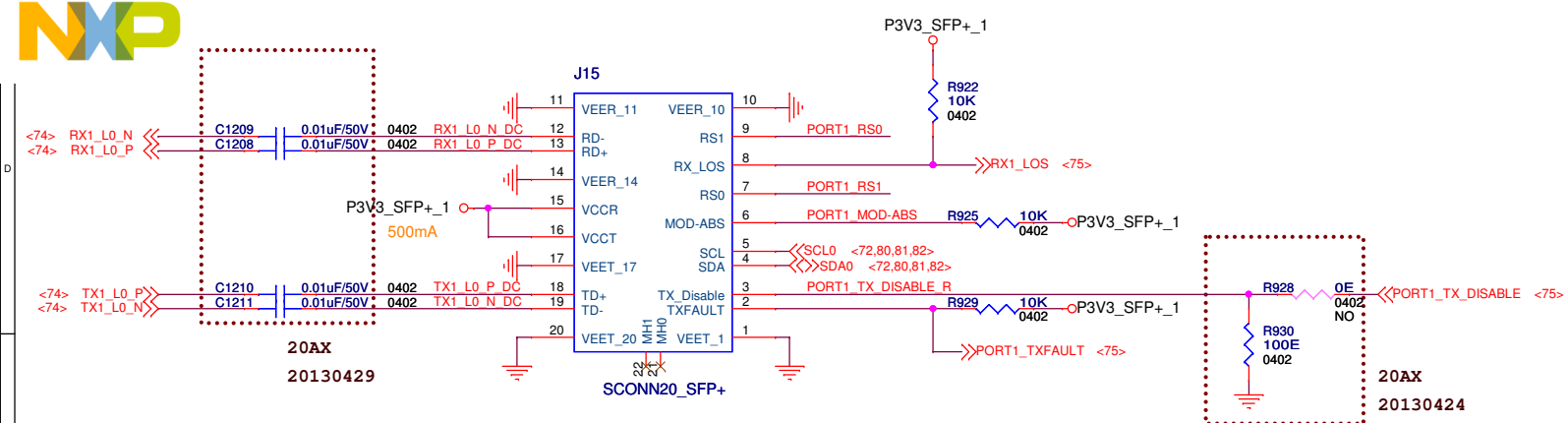


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Title <b>CS4340_PWR_P1V0_FILTER</b>		
Size B	Document Number <b>4BS05640C1X10</b>	Rev 30BX
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<b>Title</b> CS4340_PWR_P1V8_P2V5		
<b>Size</b> B	<b>Document Number</b> 4BS05640C1X10	<b>Rev</b> 30BX
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### 2.4.4 Mod\_ABS

Mod\_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this contact up to Vcc\_Host with a resistor in the range 4.7 kΩ to 10 kΩ. Mod\_ABS is asserted "High" when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF-8074) this contact has the same function but is called MOD\_DEF0.

### 2.4.1 Tx\_FAULT

Tx\_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. If Tx\_Fault is not implemented, the Tx\_Fault contact signal shall be held low by the module and may be connected to Vee within the module.

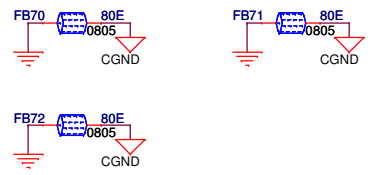
The Tx\_Fault output is an open drain/collector and shall be pulled up to the Vcc\_Host in the host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 6.

Parameter	State	Conditions
RS0	Low	RX signalling rate less than or equal to 4.25 GBd
	High	RX signalling rate greater than 4.25 GBd
RS1	Low	TX signalling rate less than or equal to 4.25 GBd
	High	TX signalling rate greater than 4.25 GBd

### 2.4.2 Tx\_DISABLE

When Tx\_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off unless the module is a passive cable assembly (see Appendix E) in which case this signal may be ignored. This contact shall be pulled up to VccT with a 4.7 kΩ to 10 kΩ resistor in modules and cable assemblies. Tx\_Disable is a module input contact.

When Tx\_Disable is asserted low or grounded the module transmitter is operating normally.

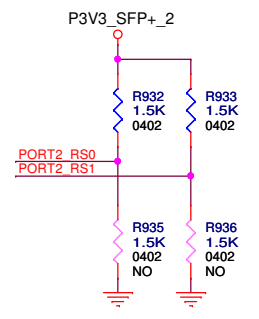
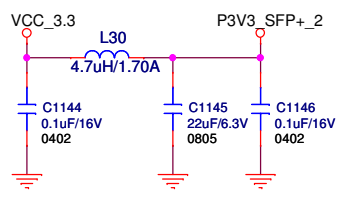
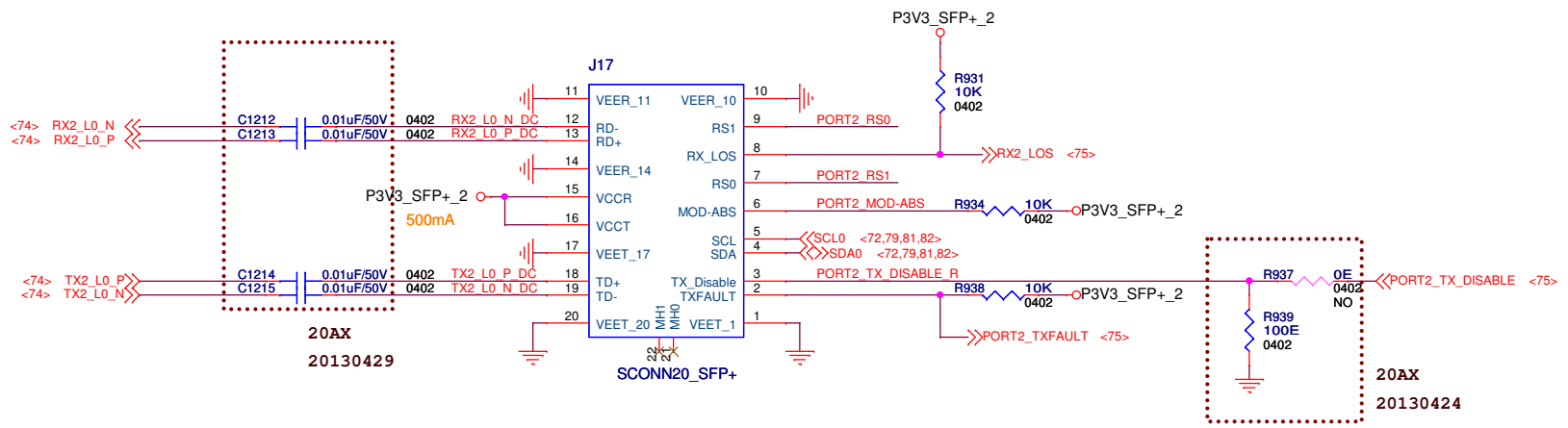


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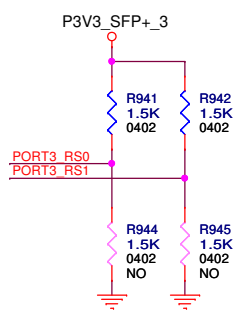
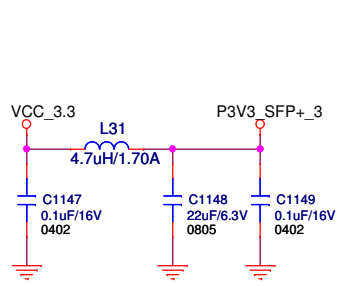
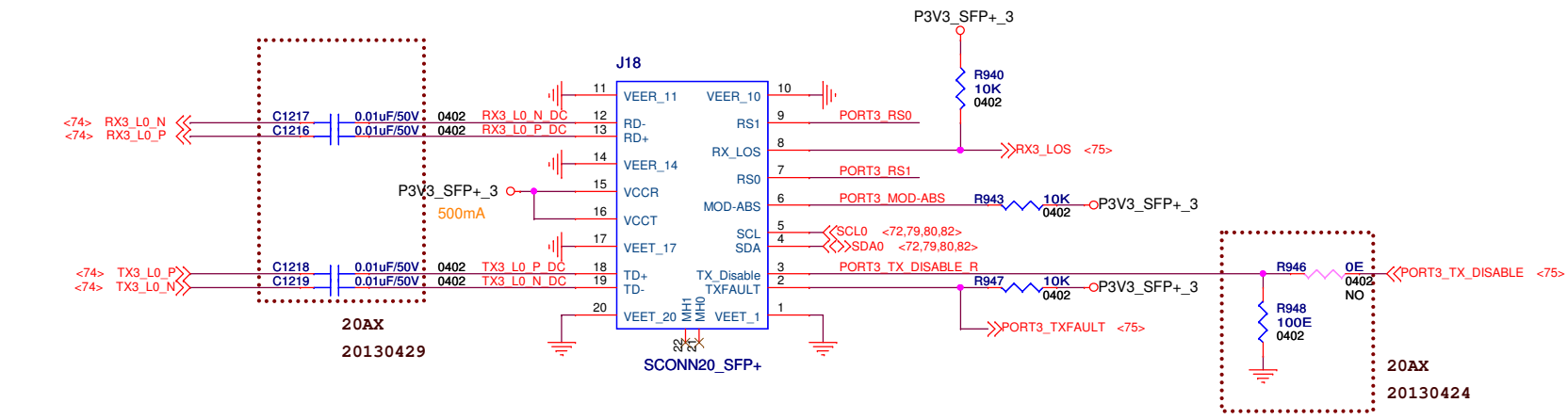
Title: **PORT0 SFP+**

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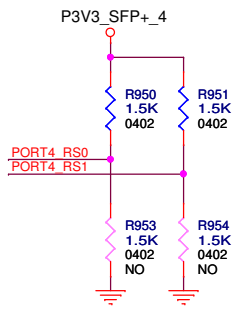
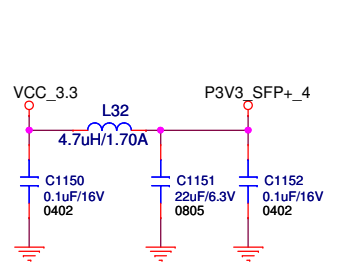
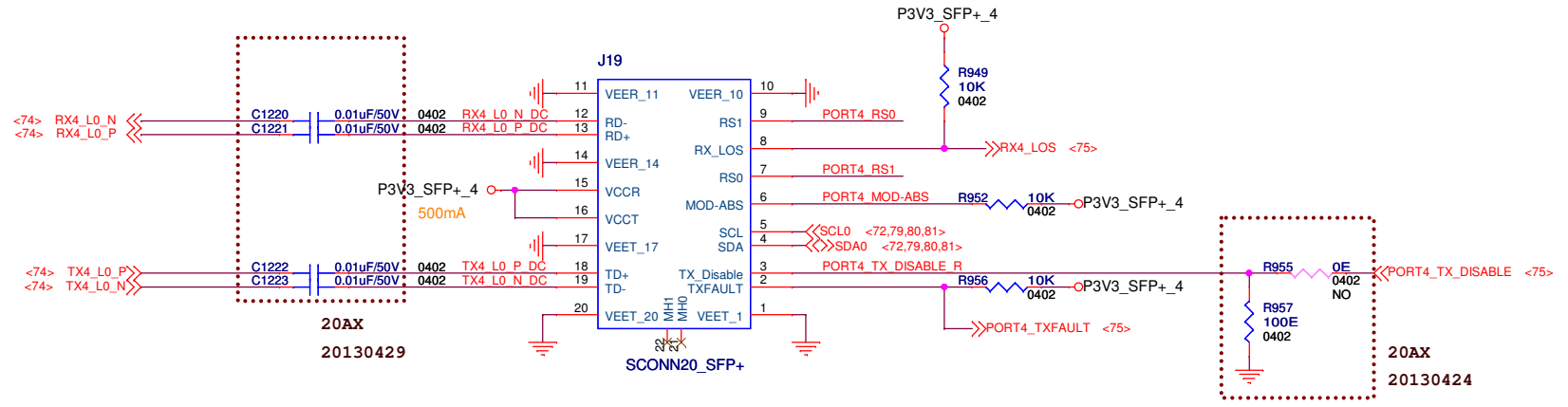


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		<b>Title</b> <b>PORT1 SFP+</b>	
<b>Size</b> B	<b>Document Number</b> <b>4BS05640C1X10</b>		<b>Rev</b> 30BX
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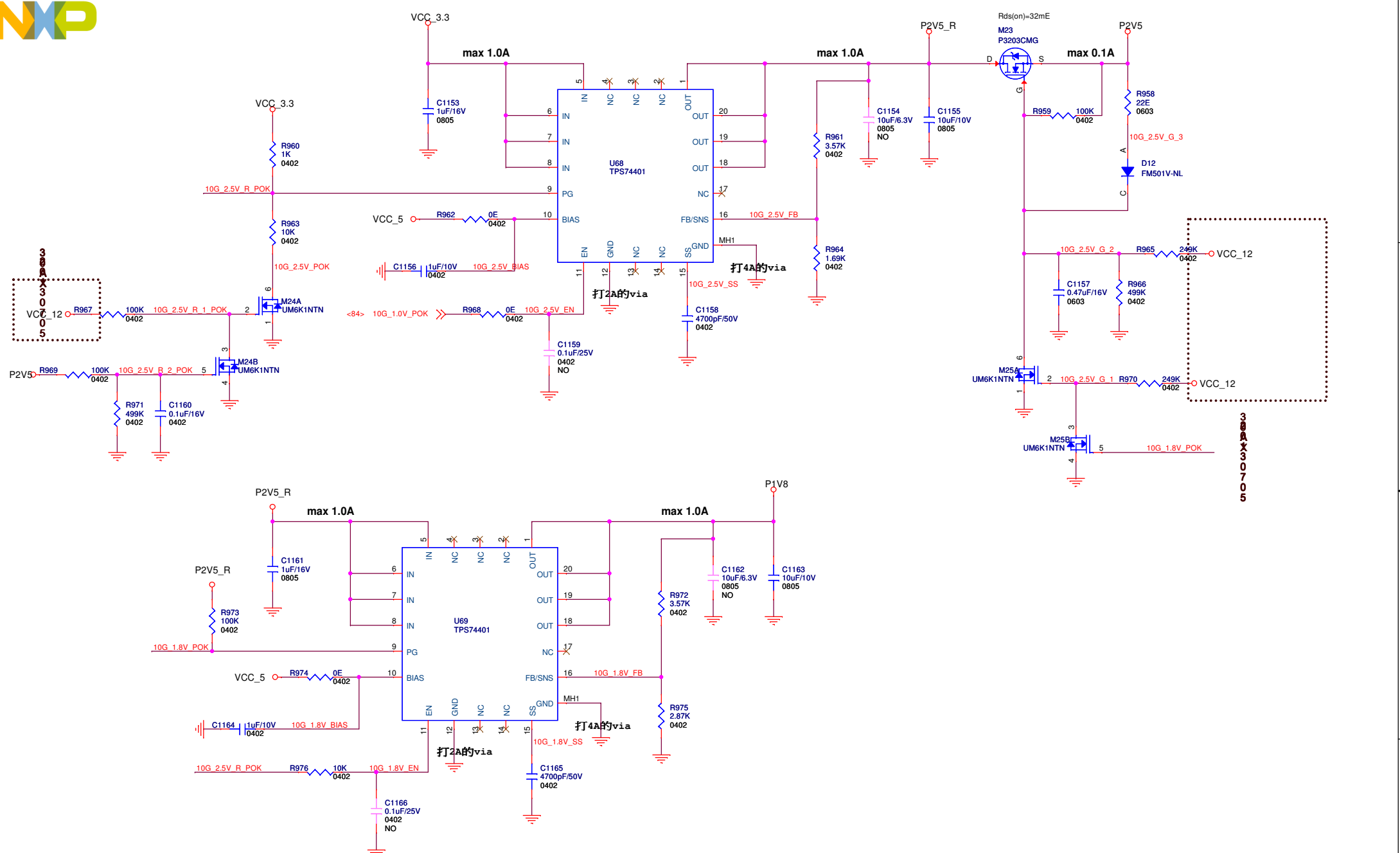




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		Title <b>PORT2 SFP+</b>	
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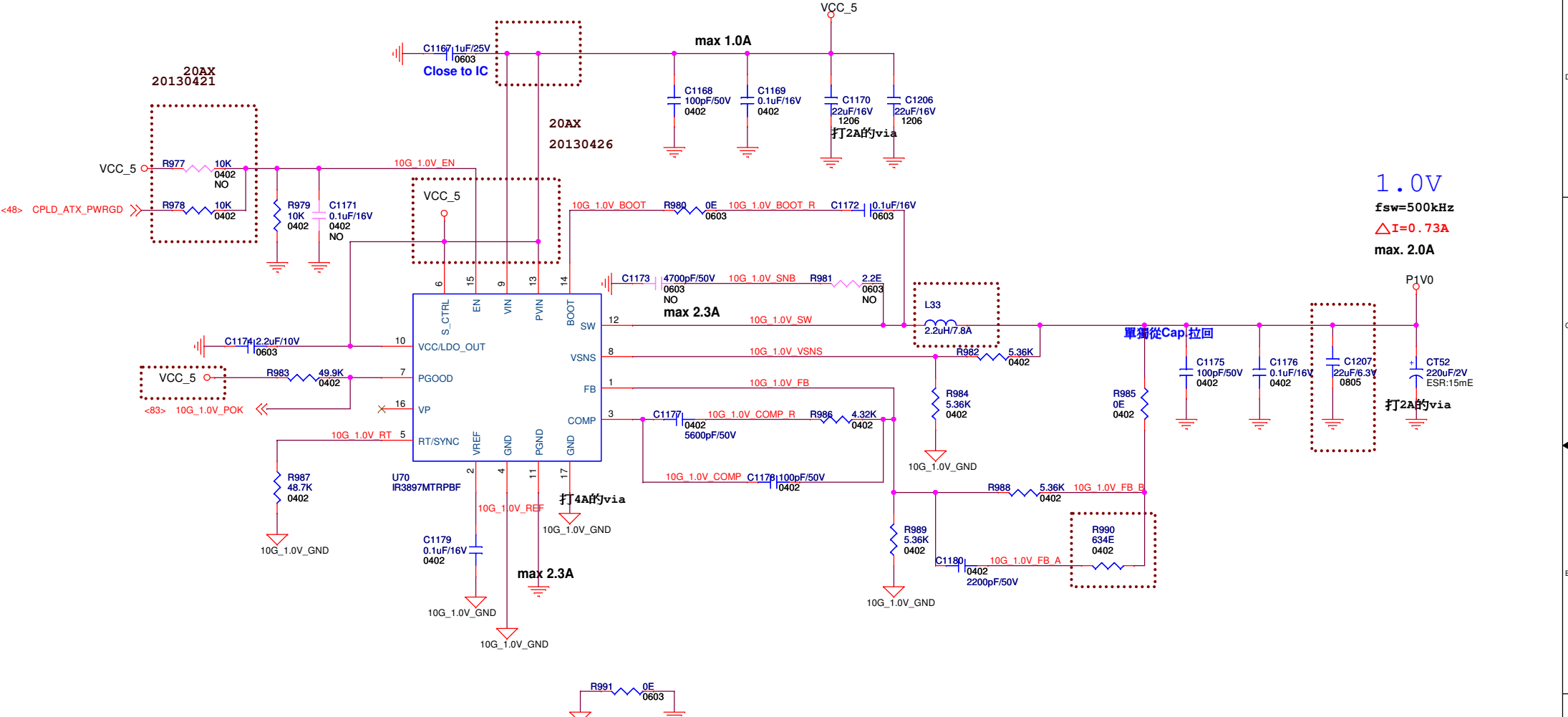
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Title: <b>PORT3 SFP+</b>		
Size: B	Document Number: <b>4BS05640C1X10</b>	Rev: 30BX
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Title			2.5V_1.8V		
Size	Document Number		Rev		
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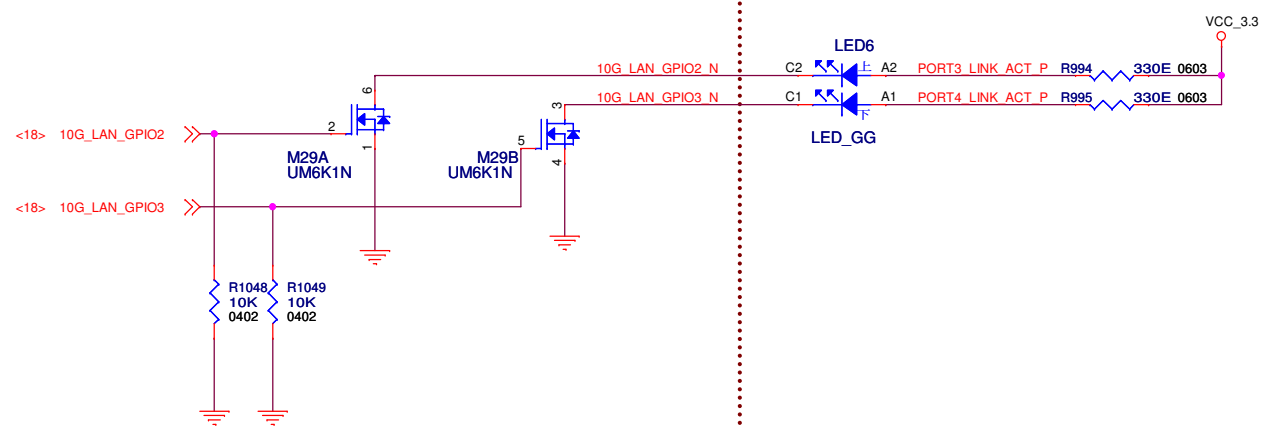
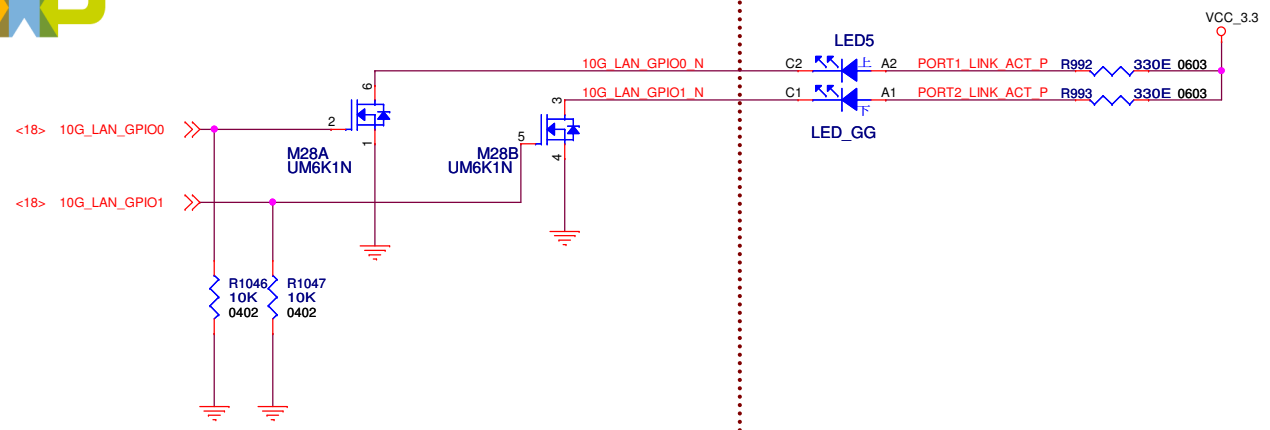


1.0V  
 fsw=500kHz  
 ΔI=0.73A  
 max. 2.0A

**Design Summary:**  
 Input Voltage & Biasing Voltage : 5V (i.e. PVin=Vin=Vcc=5V)  
 Switching Frequency: 500kHz  
 Iout: 2.3A  
 OCP Trip point: 7A  
 BW: 15kHz  
 PM: 63 degree

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Title		
1.0V		
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Title <b>LED</b>		
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	Revision	Note
2012/08/17	00AA	First draft
2012/12/19	10AA	Release
2013/04/23	20AA	<p>P12,P48:BCTL connect to CPLD</p> <p>P15,P42,P71~P85 :Del 10G slot , CS4340 on board</p> <p>P27 :Strap pin setting</p> <p>P30,P31,P50:Del I2C multiplexor ,Add I2C buffer</p> <p>P34,P36 :Strap pin setting</p> <p>P43 :Del miniPCIe slot , add PCIe X4 SLOT</p> <p>P45:Add bead between UART'GND and GND</p> <p>P46,P47:Add jump to switch the booting device(NOR or NAND)</p> <p>P48:R326 connect to P3V3SB</p> <p>P54:R104:NC,add C990:0.1uF</p> <p>P57:Connect SW6.2 to J2.13</p> <p>P57:SW5'LED power connect to 5VSB</p> <p>P58:Add net :ATX_PWROK_GAL to CPLD</p> <p>P62:Connect OVDD to 1.8V</p> <p>P64~P66:change value</p>
2013/07/08	30AA	<p>P18:Add R1074,R1075</p> <p>P34,P36:Add FB77,FB78,FB79,FB80</p> <p>P45:Add damping resistor and capacitor for UART1 ,UART2</p> <p>P47:Add level ic for IFC_CS0_B , IFC_CS1_B IFC_CS0_B_CPLD , IFC_CS1_B_CPLD</p> <p>P51:Add 0 ohm for RTC power</p> <p>P54:Remove C990</p> <p>P70:Add 0.75 V filter</p> <p>P73:Modify 156.25MHz CLK input</p> <p>P83:Connect 12V to R965,R970,R967</p>



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