KINETIS K-SERIES 120 MHZ K21F/K22F (2N03G and 3N03G mask sets) DATASHEET, REFERENCE MANUAL and ERRATA UPDATE

LIST of CHANGES

Datasheet:

• Updated table 4 "Voltage and current operating behaviors"

The following specification were updated in Table 4:

I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	
I_{IND}	Input leakage current, digital pins • $V_{SS} \le V_{IN} \le V_{IL}$					, 3
	• All digital pins	—	0.002	0.5	µA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	µA	
	• PTD7	—	0.004	1	µA	
I_{IND}	Input leakage current, digital pins • $V_{IL} < V_{IN} < V_{DD}$					2
	• $V_{DD} = 3.6$ V	—	18	26	µA	
	• $V_{DD} = 3.0$ V	—	12	19	µA	
	• $V_{DD} = 2.5$ V	—	8	13	µA	
	• $V_{DD} = 1.7$ V	—	3	6	µA	
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	—	1	50	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	0.25	µA	
I_{OZ_Tamper}	Hi-Z (off-state) leakage current (per Tamper pin)	—	—	0.25	µA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	35	50	kΩ	4
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	35	50	kΩ	5

Reference Manual:

- **Removed CEA709.1 registers from UART**

All CEA709.1 registers were removed from the new reference manual.

- UARTx_C6, UARTx_PCTH, UARTx_PCTL, UARTx_B1T, UARTx_SDTH, UARTx_SDTL, UARTx_PRE, UARTx_TPL, UARTx_IE, UARTx_WB, UARTx_S3, UARTx_S4, UARTx_RPL, UARTx_RPREL, UARTx_CPW, UARTx_RIDT, UARTx_TIDT

- **Removed EARS registers from DMA**

The following registers were removed from the new reference manual.

22.3.16 Enable Asynchronous Request in Stop Register (DMA_EARS)

Address: 4000_8000h base + 44h offset = 4000_8044h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												EDREQ_3	EDREQ_2	EDREQ_1	EDREQ_0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA_EARS field descriptions

Field	Description
31–4 Reserved	Reserved. This field is reserved. This read-only field is reserved and always has the value 0.
3 EDREQ_3	Enable asynchronous DMA request in stop for channel 3. 0 Disable asynchronous DMA request for channel 3. 1 Enable asynchronous DMA request for channel 3.
2 EDREQ_2	Enable asynchronous DMA request in stop for channel 2. 0 Disable asynchronous DMA request for channel 2. 1 Enable asynchronous DMA request for channel 2.
1 EDREQ_1	Enable asynchronous DMA request in stop for channel 1. 0 Disable asynchronous DMA request for channel 1 1 Enable asynchronous DMA request for channel 1.
0 EDREQ_0	Enable asynchronous DMA request in stop for channel 0. 0 Disable asynchronous DMA request for channel 0. 1 Enable asynchronous DMA request for channel 0.

- **Removed LPOPO bit from SMC_VLLCTRL registers**

SMC VLLCTRL register in the current reference manual:

Bit	7	6	5	4	3	2	1	0
Read	0		PORPO	RAM2PO	LPOPO	VLLSM		
Write								
Reset	0	0	0	0	0	0	1	1

SMC VLLCTRL register in the new reference manual:

Bit	7	6	5	4	3	2	1	0
Read	0		PORPO	RAM2PO	0	VLLSM		
Write								
Reset	0	0	0	0	0	0	1	1

- **Removed C9 and C10 registers from MCG**

The following registers were removed from the new reference manual.

25.3.13 MCG Control 9 Register (MCG_C9)

Address: 4006_4000h base + Eh offset = 4006_400Eh

Bit	7	6	5	4	3	2	1	0
Read	0				0			
Write								
Reset	0	0	0	0	0	0	0	0

MCG_C9 field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

25.3.14 MCG Control 10 Register (MCG_C10)

Address: 4006_4000h base + Fh offset = 4006_400Fh

Bit	7	6	5	4	3	2	1	0
Read	0				0			
Write								
Reset	0	0	0	0	0	0	0	0

MCG_C10 field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
3–0 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

- **Added SPI chapter "3.9.3.11 Writing SPI Transmit FIFO"**

3.9.3.11 Writing SPI Transmit FIFO

In Master mode, only 32-bit write accesses are supported for the PUSHR register, the top TX FIFO entry. In Slave mode, 8-bit, 16-bit and 32-bit write accesses are supported for the PUSHR register, although wach write increments the write pointer.

Errata:

Removed: e4935: UART: CEA709.1 features not supported

Errata type: Errata

Description: Due to some issues that affect compliance with the specification, the CEA709.1 features of the UART module are not supported. Normal UART mode, IrDA, and ISO-7816 are unaffected.

Workaround: Do not use the UART in CEA709.1 mode.

Added: e6070: I2C: Repeat start cannot be generated if the I2Cx_F[MULT] field is set to a nonzerovalue

Errata type: Errata

Description: If the I2Cx_F[MULT] field is written with a non-zero value, then a repeat start cannot be generated.

Workaround: There are two possible workarounds:

1) Configure I2Cx_F[MULT] to zero if a repeat start has to be generated.

2) Temporarily set I2Cx_F [MULT] to zero immediately before setting the Repeat START bit in the I2C C1 register (I2Cx_C1[RSTA]=1) and restore the I2Cx_F [MULT] field to the original value after the repeated start has occurred.

Added: e5641: FlexCAN: Module does not transmit a message that is enabled to be transmitted at a specific moment during the arbitration process.

Errata type: Errata

Description: FlexCAN does not transmit a message that is enabled to be transmitted in a specific moment during the arbitration process. The following conditions are necessary to have the issue.

- Only one MB is configured to be transmitted

- The write which enables the MB to be transmitted (write on Control status word) happens during a specific clock during the arbitration process

After this arbitration process occurs, the bus goes to Idle state and no new message is received on bus.

For example:

1) MB13 is deactivated on RxIntermission (write 0x0 on CODE field from Control Status word) - First write on CODE

2) Reconfigure the ID and data fields

3) Enable the MB13 to be transmitted on BusIdle (write 0xC on Code field) - Second write on code

4) CAN bus keeps in Idle state

5) No write on Control status from any MB happens

During the second write on code (step 3), the write must happen one clock before the current MB13 is to be scanned by arbitration process. In this case, it does not detect the new code (0xC) and no new arbitration is scheduled.

The problem can be detectable only if the message traffic ceases and the CAN bus enters into Idle state after the described sequence of events.

There is NO ISSUE if any of the conditions below holds:

a) Any MB (either Tx or Rx) is reconfigured (by writing its CS field) just after the Intermission field.

b) There is other configured MB to be transmitted

c) A new incoming message sent by any external node starts just after the Intermission field

Workaround: To transmit a CAN frame, the CPU must prepare a Message Buffer for transmission by executing the following standard 5 step procedure:

1. Check if the respective interrupt bit is set and clear it

2. If the MB is active (transmission pending), write the ABORT code (0b1001) to the CODE field of the Control and Status word to request an abortion of the transmission. Wait for the corresponding IFLAG to be asserted by polling the IFLAG register or by the interrupt request if enabled by the respective IMASK. Then read back the CODE field to check if the transmission was aborted or transmitted. If backwards compatibility is desired (MCR[AEN] bit negated), just

write the INACTIVE code (0b1000) to the CODE field to inactivate the MB but then the pending frame may be transmitted without notification.

3. Write the ID word

4. Write the data bytes

5. Write the DLC, Control and CODE fields of the Control and Status word to activate the MB

The workaround consists of executing two extra steps:

6. Reserve the first valid mailbox as an inactive mailbox (CODE=0b1000). If RX FIFO is disabled, this mailbox must be MB0. Otherwise, the first valid mailbox can be found by using table "RX FIFO filters" on FlexCAN3 chapter.

7. Write twice INACTIVE code (0b1000) into the first valid mailbox.

Note: The first mailbox cannot be used for reception or transmission process.

Added: e8807: USB: In Host mode, transmission errors may occur when communicating with a Low Speed (LS) device through a USB hub

Errata type: Errata

Description: In Host mode, if the required 48 MHz USB clock is not derived from the same clock source used by the core, transmission errors may occur when communicating with a Low Speed (LS) device through a USB hub. A typical example that causes this issue is when an external 48 MHz clock is used for the USB module via the USB_CLKIN pin, and a separate external clock on XTAL/EXTAL is used to generate the system/core clock. This issue does not occur when in USB Device mode or if the LS device is not connected through a USB hub.

Workaround: In Host mode, ensure the 48 MHz USB clock is derived from the same clock source that the system clock uses. The two clocks, while they do not need to be the same frequency, both need to come from the same source so that they are in sync. For example, generate the 48 MHz USB clock by dividing down the PLL clock used by the core/system via the SIM_CLKDIV2[USBFRAC] and SIM_CLKDIV2[USBDIV] bit fields.

Added: e7135: FTFE: Swap indicator address in upper half of 512KB block can cause ACCERR or MGSTAT0 error indications during swap commands

Errata type: Errata

Description: The flash is organized as 1024 KB of total memory configured in two 512 KB logical blocks (Pflash block 0 and P-flash block 1) where the two logical blocks can be swapped so that either of the logical blocks is at address 0x0. During initialization of the swap system a swap

indicator address must be provided. The swap indicator address will be used to reserve the provided address in P-flash block 0 and the address at the same offset in P-flash block 1 to store information about the current swap status. Both of the swap indicator addresses, the address in P-flash block 0 and the corresponding address in P-flash block 1 must be erased in the erased state when initializing the swap system. Due to an error with the swap erase check logic, if the swap indicator address is in the upper half of P-flash block 0, then in addition to erasing the swap indicator address locations in both P-flash block 0 and block 1, the corresponding addresses where bit 18 of the address is cleared must also be erased. The swap logic drops the most significant bit of the address (bit18) so that when swap operations are performed four addresses can be used instead of just the two expected ones. This can lead to an access error flag (FTFE_FSTAT[ACCERR] = 1) during swap initialization or memory controller command completion errors (FTFE_FSTAT[MGSTAT0] = 1) during other swap commands.

For example, if desired swap indicator address is 0x0004_8000, and 0x0004_8000 is erased as required, but 0x0000_8000 is NOT erased, then the swap initialization will return an ACCERR. In this example, 0x0004_8000, 0x0000_8000, 0x000C_8000, and 0x0008_8000 should all be erased and reserved by the application so that they are not modified outside of the swap system.

Workaround: - Choose a swap indicator address in the lower half of P-flash block 0.

- If the swap indicator address needs to be in the upper half of P-flash block 0, then make sure the corresponding address in the lower half of P-flash block 0 (bit 18 = 0) is erased before initializing the swap system. In addition, the corresponding offsets in P-flash block 1 for both addresses should be erased before initializing the swap and not modified directly by the application. Note that the security byte in the flash configuration field is typically programmed so that address should be avoided.

- If the flash swap feature is not being used or if the flash is fully erased (except for the security byte) before initializing the swap system, then no workaround is required.