

White Paper

Mobile Extreme Convergence:

A Streamlined Architecture to Deliver Mass-Market Converged Mobile Devices

Contents

1. Executive Summary.....	3
1.1 Limitations of Today's Architectures	3
1.2 Mobile Extreme Convergence System Architecture	3
1.3 Mobile Extreme Convergence Benefits.....	4
2. Market Opportunity	5
2.1 Market Growth in Feature Phones	5
2.1.1 The Case of Camera Phones	5
2.2. Consumers Adopting New Behaviors	6
2.2.1 Consumer Market Segments	7
2.3 OEMs Seeking Faster, Easier Product Development.....	7
2.4 Carriers Seeking Return on Network Investment	8
2.5 Content-Driven Security Needs	8
3. Technical Obstacles to Overcome	9
3.1 Limitations of Current Architectures	9
3.2 System Cost.....	13
3.3 Security Challenges.....	13
4. The Mobile Extreme Convergence Architecture	14
4.1 System Architecture	14
4.1.1 Single-Core Modem	15
4.1.2 Dedicated Application Processor Core.....	17
4.1.3 Software Architecture.....	19
4.1.4 Smart System Power Management	20
4.1.5 Best-in-Class System Memory Support	21
4.1.6 Multimode Connectivity: PAN, LAN, WAN	21
4.1.7 Location Services.....	22
4.1.8 Feature Summary	22
4.2 System Security	23
4.3 Small Footprint.....	23
5. Mobile Extreme Convergence Benefits.....	25
6. Conclusion.....	25

1 Executive Summary

The dramatic growth hoped for in the mobile device industry can only happen if the creativity of both device designers and applications developers can be unleashed—freed from oppressive demands of outdated architectures that are based on attempts to further miniaturize already overly complex systems or to retrofit power-hungry PC architectures to a pocket-sized, untethered, 24/7 world. Freescale Semiconductor*, with its more than 50 years of wireless know-how, is uniquely qualified to deliver this first major rethinking of wireless and mobile smart handheld architecture, reducing complexity, size and power consumption while building in the future. With its revolutionary hardware and software design and the incorporation of patented security technologies developed by Freescale to drive mobile commerce, the Mobile Extreme Convergence (MXC) architecture will enrich the mobile experience of the mass-market consumer through easy-to-use, compact and affordable universal mobile products.

The answer is to be able to offer smartphones, feature phones and a wide variety of converged and mobile devices at mass-market prices. To do this, Freescale has taken a major step in the design of the core architectures used to power such devices.

1.1 LIMITATIONS OF TODAY'S ARCHITECTURES

The early-generation analog cell phones consisted of a discrete single CISC-based microcontroller (MCU) core controlling a number of analog circuits. The move from analog to digital technology drove the need for a digital signal processor (DSP) core to be added to the architecture. Dual-core architectures, consisting of an MCU and a DSP, evolved from several discrete parts to a single ASIC in the mid-nineties.

Current dual-core baseband architectures were not designed to support the feature requirements of converged devices, and as a result, today's smartphone architecture requires additional processing resources by adding a discrete application processor to the discrete dual-core cellular baseband IC. Each processor requires its own memory system comprising RAM and Flash. Support for additional wireless networking, such as Wi-Fi® and Bluetooth(tm) wireless technology, requires additional modules for each function, including radio transceivers, digital basebands, RAM and Flash components within the module. This approach yields a system architecture having a minimum of three, or as many as six, CPUs, each with its own dedicated memory system, peripherals, clock generator, reset circuit, interrupt controller, debug support and interprocessor communications software.

1.2 MOBILE EXTREME CONVERGENCE (MXC) SYSTEM ARCHITECTURE

Adoption of features, such as color display, cameras and converged capabilities, would not be possible without advances in semiconductor technology, microarchitectures and embedded systems. It is for this reason, and to implement more advanced features, such as 2-D and 3-D graphics, mobile multimedia, Mobile IP and personal entertainment, that Freescale has created the MXC architecture.

The MXC architecture completely rethinks how a phone platform is designed, providing a 50 percent reduction in design complexity. It is the first single architecture for manufacturers and applications developers to cost-effectively bring highly valued applications into the mass-market at favorable price and cost points, unlocking trapped value for suppliers, carriers, developers and consumers alike.

Freescale's MXC architecture offers seamless access to multimode features, such as world connectivity, Internet readiness, wireless local-area networking (WLAN), global positioning service (GPS) and Bluetooth connectivity, coupled with the ability to deliver portable applications, such as multimedia messaging, voice activation features, gaming, wireless photos, mobile video and MP3 playback and many other consumer applications that the mass consumer market has yet to enjoy because of the unnecessary complexity, high costs and unwieldy size created by current architectures

The MXC platform is the result of 24 months of intense research and development by a team of Freescale engineers with combined experience of more than 100 years in wireless system design.

- **Single-core modem (SCM)**—Using the newest generation DSP based on StarCore(tm) technology, the single-core modem complex performs all the signaling protocol layers (L1, L2 and L3) for 2.5G, 2.75G and 3G (WCDMA, UMTS) standards. The performance needed to support high-speed wireless data is achieved by using a combination of embedded nonvolatile memory (NVM) and RAM. The architecture incorporates an L1 cache to improve performance when using slower memory systems. It also provides additional power savings by reducing the frequency of accesses to the memory system.
- **Dedicated application processor**—An ARM1136(tm) core, operating at 400 MHz with 128 KB of on-chip L2 cache and a full complement of peripherals, provides a dedicated application processor environment that surpasses the performance of discrete application processors on the market today.
- **System security**—MXC architecture includes Freescale's security framework, comprising both hardware and software elements required for a wide range of security services and applications.
- **Small footprint**—The MXC vision encompasses technologies required to realize this new architecture in a single package—a package whose area is less than a 1/2 -square inch. The complete package is an assembly of subsystems: MXC IC consisting of single-core modem and application processing cores, memory, RF/PA and power management.

1.3 MOBILE EXTREME CONVERGENCE BENEFITS

The MXC architecture unites digital signal processing, applications processing and multiple connectivity systems-functions previously performed by many dozens of memory- and power-hungry components-into one highly integrated nucleus. This simpler approach removes layers of architectural redundancy, creating lower overhead, lower memory requirements, fewer handoffs and opportunities to drop instructions, as well as lower development and manufacturing costs. Key architecture changes include:

- The convergence of all protocol processing into a single core, which drives the entire range of global cellular and local connectivity protocols, eliminating as many as six processor cores and substantially dropping part count and complexity.
- An integrated applications processing function, which allows developers to write once and port their applications to any other device, using a consistent processing core.
- Shared memory systems and reduced interprocessor communication systems to free up processing capability, reduce part count and streamline communication.
- Hardware acceleration and memory caching techniques to dramatically cut power consumption.

When productized, the architecture will deliver a complete smartphone platform in a 16 mm x 20 mm package and a slim 1.4 mm, enabling virtually any device—an MP3 player, a handheld DVD player, a digital camera-to become a smartphone.

2. Market Opportunity

Over the next several years, industry analysts predict enormous growth in the market for converged mobile devices that merge voice-phone capability with multimedia, PDA and game applications. These types of devices will expand the market to include new categories of consumers, who will use them for activities far beyond traditional mobile phone calls. Original equipment manufacturers (OEMs) and carriers must strive to meet this growth by providing smart products and content-rich services that consumers and content providers alike can trust with their data, while still maintaining profit margins.

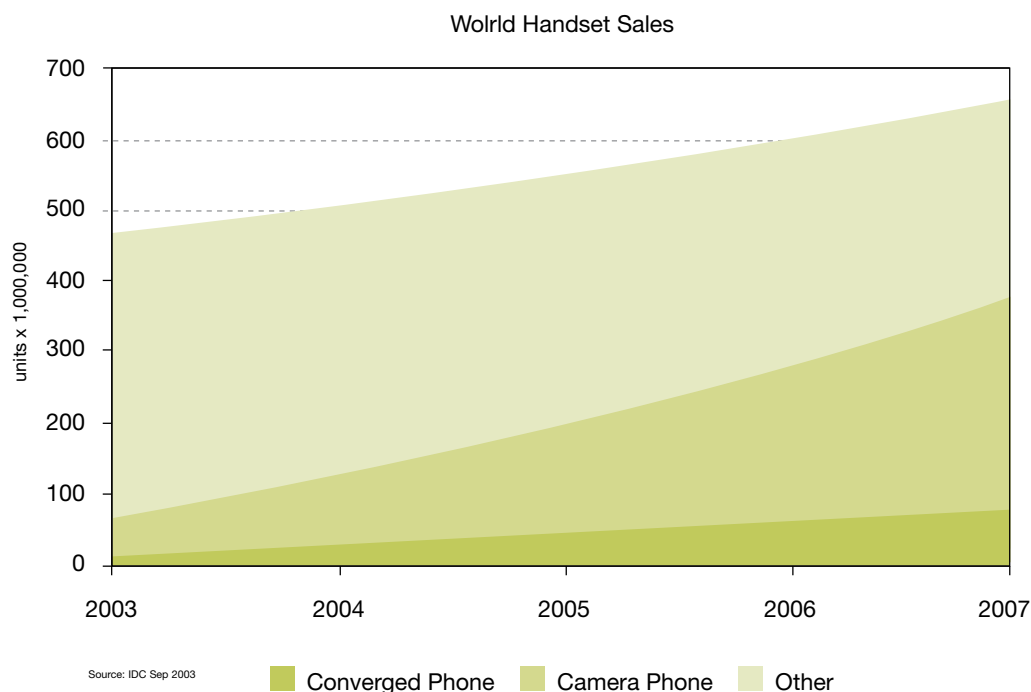
2.1 MARKET GROWTH IN FEATURE PHONES

In 2003, converged mobile devices-smartphones-were forecast to make up three percent of worldwide mobile phone sales volume. The converged mobile device market will continue to expand at triple digit year-over-year growth rates, driven by the evolution of voice-centric converged mobile devices, mobile phones with applications processors and advanced operating systems supporting a range of data functions, including application download and execution. Such sustained growth is the result of these voice-centric devices, which are specifically designed and positioned to serve as a subscriber's only mobile device, replacing pagers and PDAs. But these market forecasts do not take into account the market potential that can be unlocked by a disruptive technology that could double the number of devices used on global cellular systems.

2.1.1 THE CASE OF CAMERA PHONES

In 2003, as shown in Figure 1, camera phone shipments made up 10 percent of worldwide mobile phone sales volume. As this technology claims a significant penetration level in Japan, all major mobile phone vendors are extending it to other markets. With its added bill-of-materials cost continuing to decline, digital capture capability is becoming simply an expected feature of mid-range and high-end mobile phones. One-megapixel capture resolution expanded throughout mobile phone lines in Japan in 2003, while VGA and sub-VGA resolutions will remain dominant in the U.S. and Europe into 2004, when one-megapixel capability reaches those shores. Mobile phones with two-megapixel capture resolution are not expected to reach volume production until 2005 at the earliest. Meanwhile, mobile phones with one-megapixel capture resolution will become dominant worldwide.

Figure 1. Cell Phone Features Market Outlook



While selling camera phones is important, what is more important to the carrier is getting subscribers to use picture-messaging services. This is because getting a customer to use such services increases the average revenue per unit (ARPU) generated, which in turn helps the carrier increase the lifetime value of a customer. Simply put, if enough subscribers use picture-messaging services, a carrier will realize a gain to its bottom line.

What if, instead of putting a camera in a phone, manufacturers could easily add cellular or wireless capability to digital cameras? In a world in which virtually any handheld consumer electronics device could add cellular capability while maintaining battery life, size and cost would significantly shift the way the cellular market is forecasted.

2.2 CONSUMERS ADOPTING NEW BEHAVIORS

Over the last 20 years, the world's cellular market has grown impressively, to the point that there are now more cellular handsets in use than wired telephones. While the growth has been substantial, it has been accomplished mainly by selling to business users and consumers who have significant disposable income. But to reach the full potential of the market, the industry must start to address the needs of the mass of consumers with less disposable income but the same craving for fully featured products.

Simply offering more services under the current sales models is not the answer-the answer is penetrating new segments with services that those users will find attractive and compelling. New market segments mean new devices and capabilities, and potentially new brands or images.

To maximize the investment in acquiring a subscriber, the operator must be able to support additional non-voice services—for example, downloadable music, movies or games in a specialized device—to these new segments in a way that provides sustainable service revenue. But the cost of smart and feature phones is higher than for a standard handset, meaning that the operator has to increase the subsidy to penetrate the segment successfully. This destroys the typical business model.

The answer is to be able to offer smartphones, feature phones and converged mobile devices at mass-market prices and through mass-market channels. How to do this presents a major challenge to OEMs and carriers.

2.2.1 CONSUMER MARKET SEGMENTS

Growing the world's wireless market beyond current levels will require penetration of new market segments, such as:

- Casual-use (low-tier) small-business users, such as those who travel occasionally for business. While they may not need all the features of a *smartphone*, they require access to e-mail and corporate applications.
- Low-tier consumer users, such as limited-use subscribers. While voice communications will be a priority with these users, the operator can increase revenues by providing handsets that support polyphonic ring tones, basic games and other advanced features.
- Emergency users, including children and consumers who will only use a wireless device for emergency situations, but will require features, such as GPS, color screens and long battery life. And since they are fashion-conscious consumers, the device should ideally be “cool”.
- *Unwired early adopters, who own a plethora of digital devices, including digital cameras, MP3 players and gaming consoles, such as Tapwave's Zodiac. Most such devices do not currently support wireless connections, but could be enhanced by adding such capabilities.

Future growth in the wireless market as a whole will be mainly due to the expansion of the consumer segments. Specifically, consumer growth in the next five years will be in the pre-teen, teenage, college and lower income segments. The industry cannot ignore any potential market segment, but must determine how best to address each one to make it profitable and leverage it as a possible conduit into other profitable market segments.

The trick is that new segments must be penetrated with new services, devices and business models. Just as Neiman Marcus and Wal-Mart® offer different products, buying experiences and pricing, so the wireless industry must move away from the traditional handset-subsidy-activation-monthly-rate-plan-plus-airtime model for these untapped segments and develop new models appropriate to each market segment.

2.3 OEMS SEEKING FASTER, EASIER PRODUCT DEVELOPMENT

Original equipment manufacturers and others involved in the design and production of wireless devices are continually seeking ways to shorten time to market, reduce development costs and simplify product complexity. Designing devices for multiple market segments can mean starting over for each type of device (feature phone, smartphone, wireless PDA, wireless game gear, etc.), due to divergent underlying technologies. They must balance the need to reduce the cost to consumers against the need for more and more features to drive revenue per unit.

Today's development cycles can range from 12 to 24 months and consume thousands of engineering hours in software, hardware and RF, and manufacturing testing. A fully developed and pre-certified cellular platform can shave six to nine months off development cycles, freeing resources to focus on innovation to drive new business opportunities and differentiated applications, interfaces and designs.

2.4 CARRIERS SEEKING RETURN ON NETWORK INVESTMENT

The mobile operators worldwide face many challenges as the market develops beyond current levels. In the past, simply investing in a new network or network technology would lead to new revenues, usually related to voice traffic. But with increased competition, the commoditization of voice services and the need to continually improve the quality of service, returns on new network investments are not guaranteed. Some of the issues that operators face include:

- Declining average revenue per user (ARPU)-ARPU in the U.S. market is forecast to fall from \$51.87 in 2003 to \$49.84 in 2007, while the voice segment of that revenue will drop 24 percent through 2006, from \$48.14 to \$36.48 in 2007 (iGillottResearch, 2003). Many users are spending far less, certainly less than \$25 per month. Thus, the importance of data, content and advanced services is amplified.
- Decreasing revenues without decreasing costs-Mobile operator margins will be increasingly squeezed, as operators target lower revenue segments but are unable to remove an equivalent amount of cost from the service operations or channels.
- Reduced device subsidies-To control costs and maintain margins, operators will be forced to reduce or limit device subsidies. This will place additional pressure on the device manufacturers to reduce device costs, while still differentiating product and providing innovation. Lowered device costs will encourage more device churn, increasing activation/provisioning costs for operators.

2.5 CONTENT-DRIVEN SECURITY NEEDS

As data-capable mobile devices become increasingly prevalent, end users, naturally, are using their new-found freedom to conduct business, personal or corporate, while on the go-sitting in an airport or a prospective customer's office, or waiting in line at the grocery store. Because these devices are portable and disconnected, there is an increased risk of the wrong people getting access to personal data, corporate data or fee-based content or services.

It is imperative, then, to safeguard the data that is created on, stored on or transmitted through wireless devices, and then to ensure that the correct owner accesses it. Although wireless equipment and software vendors have released many products to protect transmitted data, more progress must be made in two areas:

- Authentication of the end user, not just the device
- Protection of data stored or created on the mobile device, including the use of encryption

The perception that wireless networks are far less secure than their wired counterparts creates an obstacle to adoption. In February 2003, iGillottResearch surveyed 1,052 enterprise IT managers and found that only 17 percent of respondent companies had deployed a wireless data solution. Approximately 35 percent of the respondents said that they had no plans to deploy wireless technology. The perceived lack of security was a top reason for a negative response.

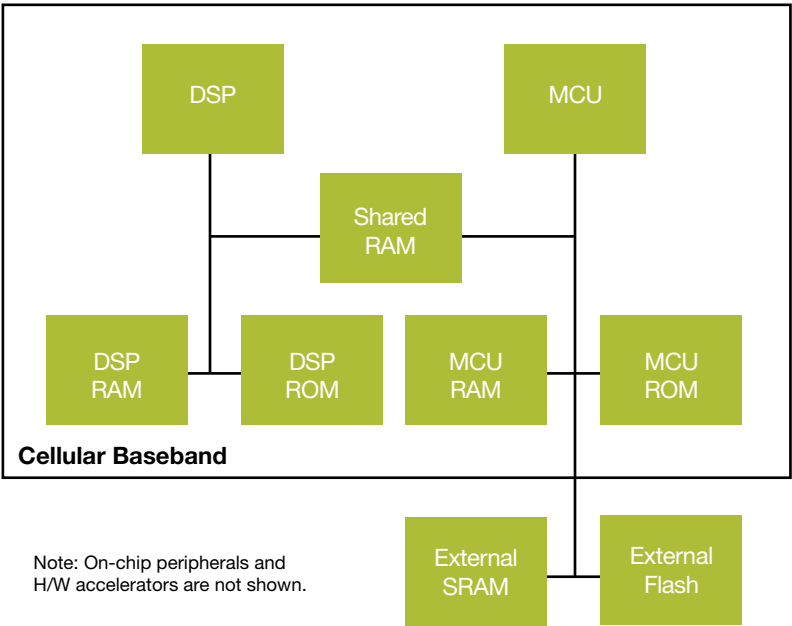
3. Technical Obstacles to Overcome

To capitalize on the growing market for smart mobile devices, OEMs and carriers must overcome a number of obstacles, including the technical complexity of current converged architectures, the inherent cost of systems based on such architectures and the security challenges posed by smart devices.

3.1 LIMITATIONS OF CURRENT ARCHITECTURES

The early-generation analog cell phones consisted of a discrete single CISC-based MCU core controlling a number of analog circuits. The move from analog to digital technology drove the need for a DSP core to be added to the architecture. A block diagram of the current-generation digital cellular baseband architecture is shown in Figure 2. This dual-core architecture, consisting of an MCU and DSP, evolved from several discrete parts to a single ASIC in the mid-nineties.

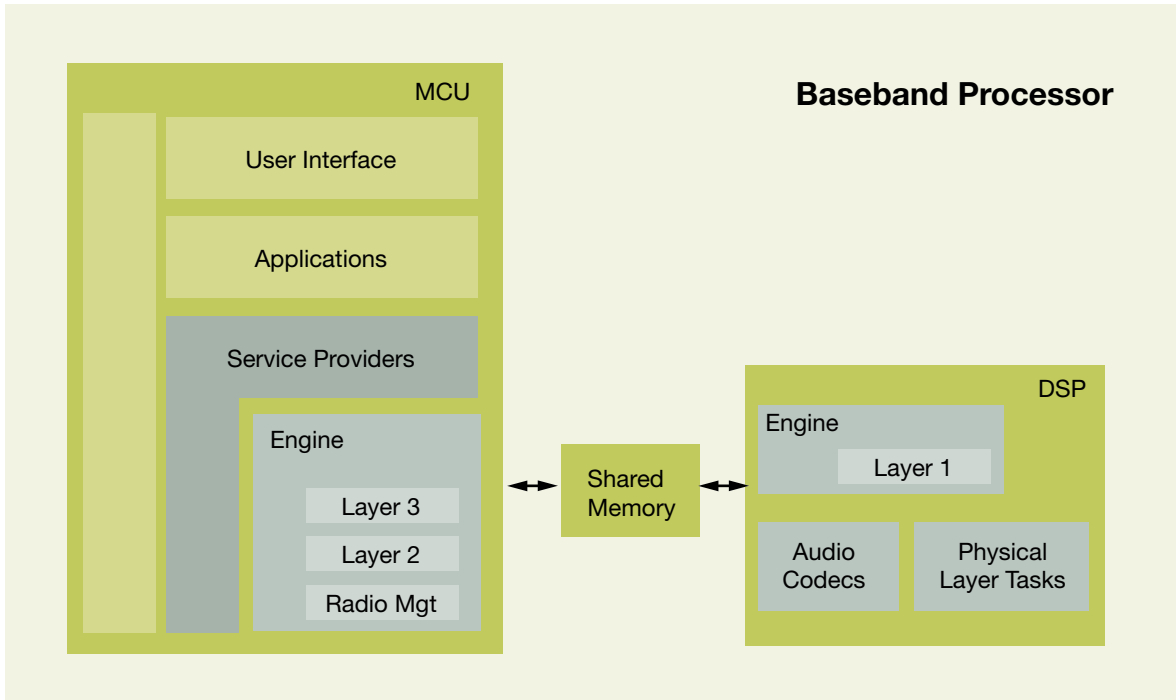
Figure 2. Block Diagram of Current Generation Digital Cellular Baseband IC



The additional performance required to support packet data (i.e., GPRS) was addressed by increasing the clock speed for both cores, adding hardware accelerators for encryption/decryption and adopting support for burst mode Flash memory.

Past- and current-generation dual-core cellular baseband ICs, across the industry, use approximately the same process partition, as shown in Figure 3, with the DSP performing signaling tasks and serving as a slave processor to the host MCU (a RISC core), which runs the upper layers (L2/L3) of the communications software protocol stack. The Layer 1 signal processing tasks handled by the DSP include equalization, demodulation, channel coding/decoding, voice codec, echo and noise cancellation, and audio equalization.

Figure 3. Current Generation Feature-Phone Software Architecture

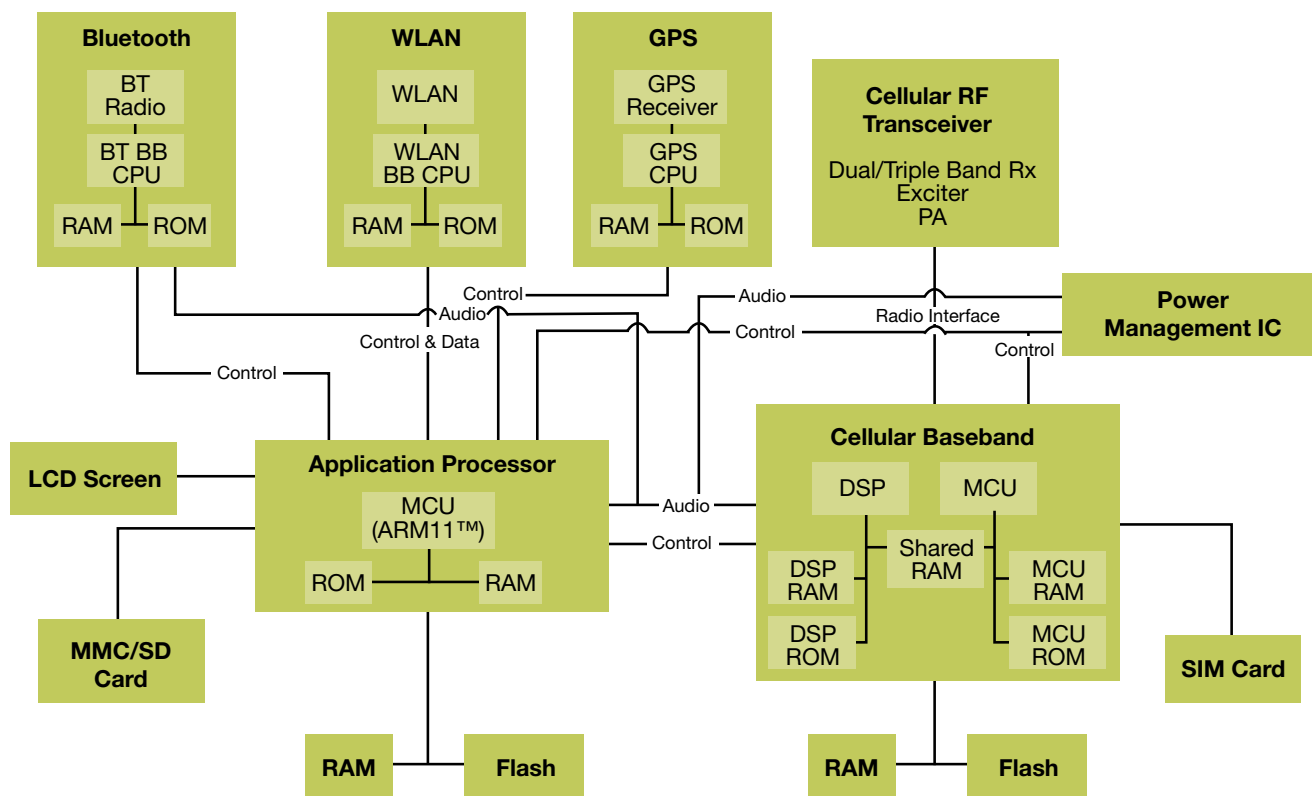


The host MCU manages the radio hardware while performing the upper layers of the network protocol stack, subscriber identity, user interface, battery management and the nonvolatile memory for storage for the phone book.

The utility of the Internet and the introduction of wireless packet data service created the need for converged mobile devices in their simplest form, through the merger of PDAs and cellular telephones. This convergence requires all the wireless processing capability of today's cellular baseband architecture, together with the additional processing resources needed to support applications containing multimedia and graphics.

The current dual-core baseband architecture was not designed to support the feature requirements of converged devices, and as a result, today's smartphone architecture provides additional processing resources by adding a discrete application processor to the discrete dual-core cellular baseband IC, as shown in Figure 4. Each processor requires its own memory system comprising RAM and Flash. Support for additional wireless networking, such as Bluetooth and WLAN connectivity, requires additional modules for each function, including radio transceivers, digital basebands, RAM and Flash components within the module. This approach yields a system architecture having a minimum of three, or as many as six, CPUs, each with its own dedicated memory system, peripherals, clock generator, reset circuit, interrupt controller, debug support and interprocessor communications software.

Figure 4. Block Diagram of Current-Generation Smartphone Using Discrete Baseband IC with Discrete Application Processor



Having separate and independent processing resources requires a sophisticated interprocessor communication network to perform data exchange and control. The complexity of this approach increases with each module added to the system. Interprocessor communication becomes a formidable design challenge to software and hardware designers, as the need to exchange real-time audio, high-speed packet data and closed-loop system control becomes critical to achieving the desired product features and use cases. The interprocessor communication traffic is not limited to communication between the cellular baseband and application processor. Supporting a full duplex digital audio stream between the cellular baseband and the Bluetooth module, while simultaneously supporting packet data communications between the application processor and cellular baseband, requires a sophisticated internetworking approach. The complexity of this interprocessor communication networking overhead reduces the processing performance available for end-user applications and increases power consumption, which results in reduced battery life and usage time for the end user.

A lower-cost alternative to the smartphone architecture depicted in Figure 5, is to merge the application processor and the cellular baseband into a single ASIC consisting of two or three cores. In the dual-core solution, the performance capability of the MCU is enhanced to serve user applications and cellular call processing roles. In this case, the performance of the MCU is shared between PDA applications and the rigid timing requirements associated with running the communication protocol stack. The dual-core approach makes it difficult to deliver the responsive end-user application environment needed to support rich multimedia applications. This approach also exposes the wireless system to potential security vulnerabilities via computer viruses, spread by applications that are downloaded into the device.

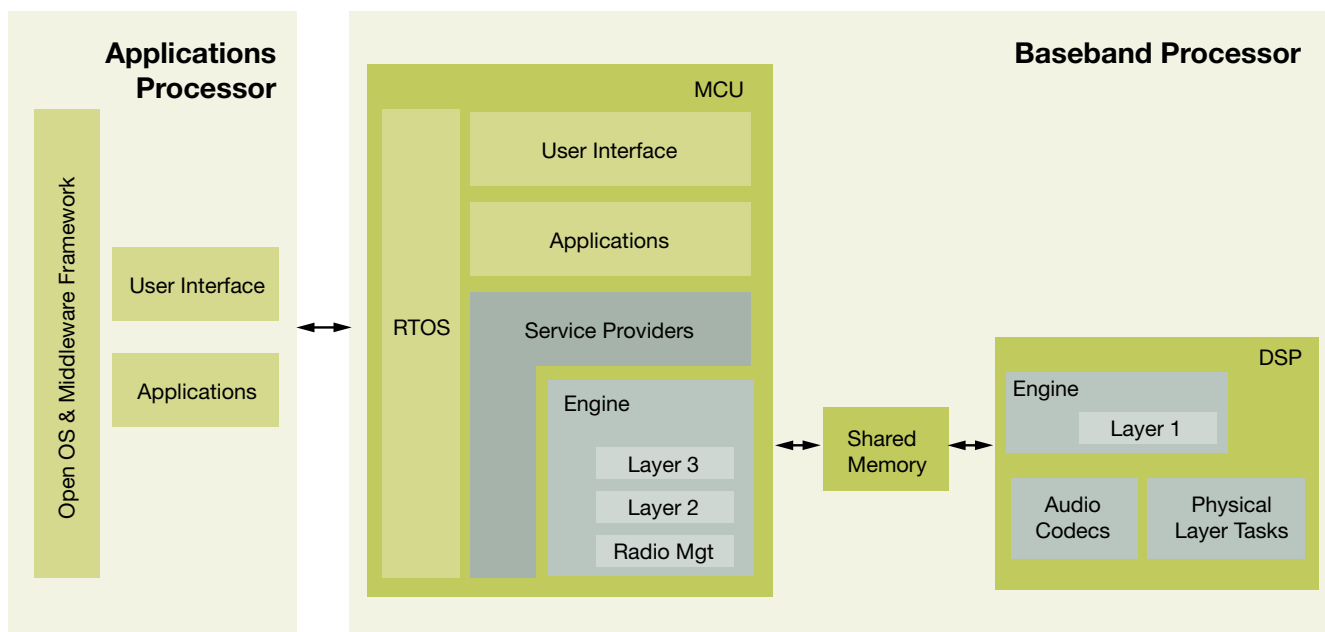
The three-core approach merges a traditional dual-core cellular baseband architecture with a third (MCU) core dedicated to user applications. This approach eliminates the performance conflict between the communication protocol tasks and multimedia workloads and addresses the security issues that are prevalent in the dual-core partition. The complexity of interprocessor communication among the three cores is not reduced, however, because the application processor must interact with both the DSP and the call processor MCU. In addition, the allocation of on-chip memory resources among the three cores introduces additional layout (array efficiency) complexity and limits the flexibility to accommodate new applications and networking protocols.

The current generation smartphone architecture (Figure 4) uses a separate baseband modem complex for each wireless network type. The disadvantage of managing separate modems to support multiple wireless networks is threefold:

- **Interprocessor communication complexity**—The interface between the application processor and each wireless modem requires a multilayer software-based protocol stack in order to support user traffic, network ID settings, bearer channel configuration and control of the modem module itself. Support for digital speech adds another layer of complexity. Two hardware implementations have emerged to address the interface requirements. One option is to separate the speech from the control and data traffic by providing two distinct serial interfaces. The other approach is to create a sophisticated serial interface with provisions to support multiple traffic payloads over a single hardware serial interface. Regardless of the approach taken, the necessity for complex serial communication protocol schemes is unavoidable. The net performance required at both ends of the serial interfaces consumes battery power and, in the case of the application processor side of the interface, reduces the performance available for the end user applications.
- **System power and standby time**—Monitoring for the presence of wireless networks requires interaction between the application processors for each connectivity node that needs to be monitored. This periodic activity and the complexity associated with interprocessor communication introduce additional processing overhead that consumes battery power.
- **Cost**—Separate baseband-processing functions for each wireless connectivity mode require a processor, memory, clock and support logic for each connectivity node. This increases the total cost of the silicon and the cost associated with the increase in PCB area.

The current generation smartphone software architectures, as shown in Figure 5, have evolved from feature-phone implementations that provide enhanced services in the modem software (on the MCU side). The interprocessor communication provides the bridge between the application environment on the application processor and the modem software on the baseband processor. This architecture, due to its evolution, includes complex interactions, redundancies and duplication between the application environment and the modem software.

Figure 5. Current Generation Smartphone Software Architecture



3.2 SYSTEM COST

A significant drawback of the current-generation smartphone architecture is the high component count that results from having discrete application processor and cellular baseband devices with separate dedicated memory. Some suppliers have addressed this issue by using IC packaging techniques (SiP) in an attempt to lower the part count and reduce the PCB area. While this approach can reduce component count by as much as 28 percent (from seven LSIs to five), it adds more cost and does not reduce complexity.

The additional modules that are needed to support Bluetooth and WLAN networking call for additional integration in order to achieve a low component count with small PCB area and a compact product profile. Here again, multiple modules having stacked dies or reliance on costly mixed-signal (analog and digital) technology leads to increased system cost.

3.3 SECURITY CHALLENGES

In addition to the ubiquity and expansion of the wireless data pipe, a number of other factors are driving the need for security as the number of converged mobile devices grows.

- Given the trend towards open architectures and operating systems, such as Linux® OS, Windows® CE, Palm OS® and Symbian OS™, users can install software and functionality on the handset. The easier it is to install applications on a device, the easier it is to attack the security of the device.
- With the potential of high value content stored on or accessed by the device, content providers have significant concerns about the risk of content being stolen, pirated or compromised.
- As converged devices become widespread and ubiquitous, the very factors that integrate them into users' lives also make them an attractive target of a criminal element.

The potentially large m-commerce market will not develop unless security issues are addressed. Given that interception of radio signals is significantly easier than intercepting information on wireline networks and that digital items can be perfectly copied and shared at virtually no cost, any architecture focused on the wireless industry must provide security solutions.

4. The Mobile Extreme Convergence (MXC) Architecture

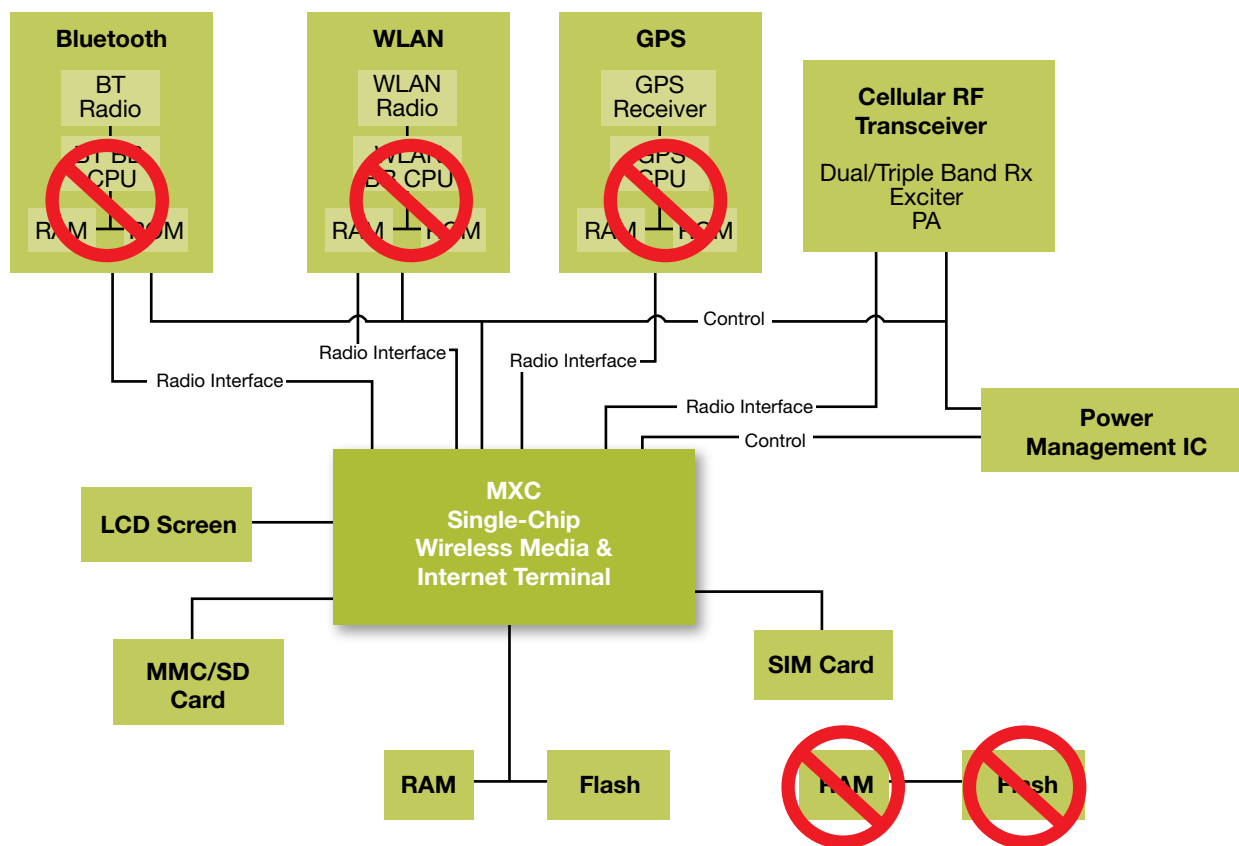
To address the need for low-cost, converged devices that can support new markets, services and business models while preserving profits for OEMs and operators, Freescale has created the MXC architecture. This architecture represents a radical simplification of the architecture for smart wireless devices, while providing a secure environment for content-rich applications..

4.1 SYSTEM ARCHITECTURE

The MXC architecture is the result of 24 months of intense research and development by a team of Freescale engineers with combined experience of over 100 years in wireless system design.

Figure 6, is a block diagram of the MXC architecture as applied to a full-featured smartphone. By comparison to Figure 4, two memories and one IC have been eliminated without compromise in functionality or performance. In addition, the complexity of the Bluetooth, WLAN and GPS modules has been reduced by eliminating the need for an embedded processor, memory and support logic in each module.

Figure 6. Simplified Block Diagram of a Mobile Extreme Convergence Architecture Smartphone



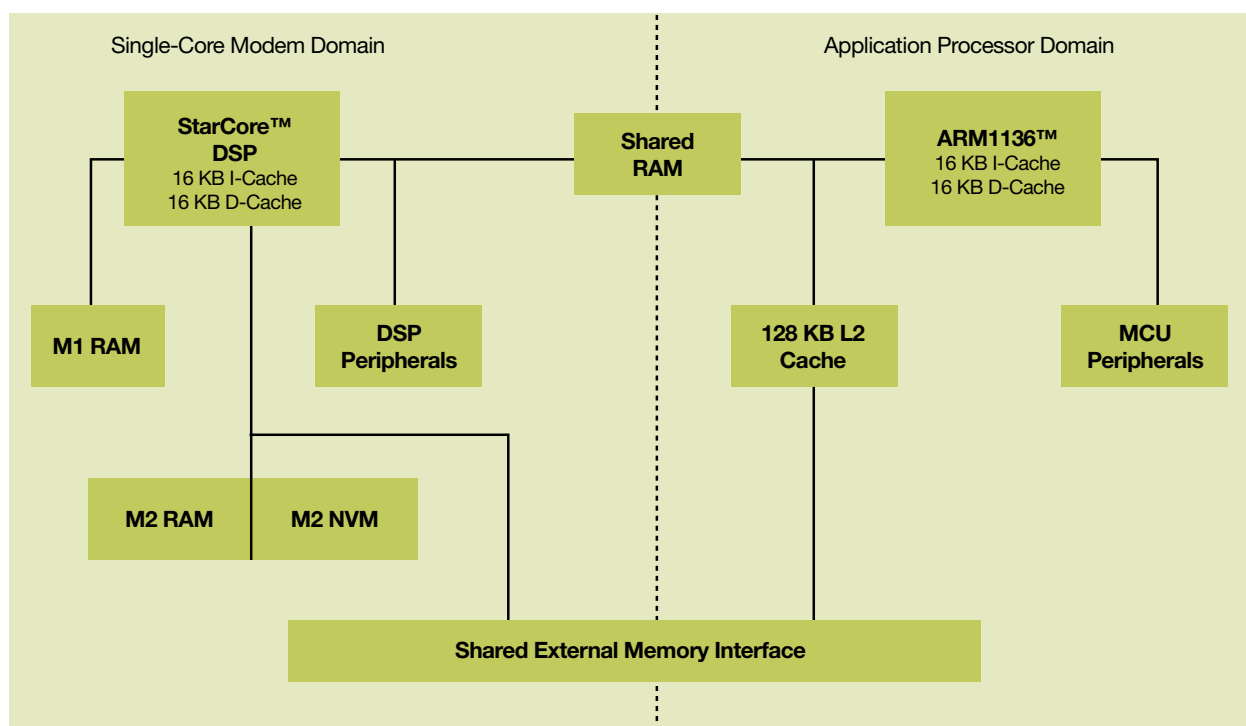
A total of four processors, three RAMs, three ROMs and three blocks of processor support logic have been eliminated and replaced by a single IC serving as the host processing complex.

The MXC IC, shown in Figure 7, serves as the host processing complex of the MXC architecture. While it is similar to current cellular baseband architectures in having two embedded cores, the underlying architecture and partitioning of the MXC architecture represent a revolution in process partitioning, system resource management, security and complexity reduction. The result is a lower smartphone system cost with no compromise in performance or functionality.

The reduction in complexity and cost is achieved through advances in DSP architecture and communications protocol stack design that enable a single DSP core to support the entire communications protocol stack. This breakthrough enables the RISC MCU, based on the ARM11(tm) core, to exclusively serve the user application environment. Improvement in the performance of the application processor over current discrete application processors is realized by an ARM1136 equipped with L1 and L2 caches.

The following sections describe this innovative architecture and provide performance comparisons.

Figure 7. Simplified Block Diagram of the MXC Host Processor



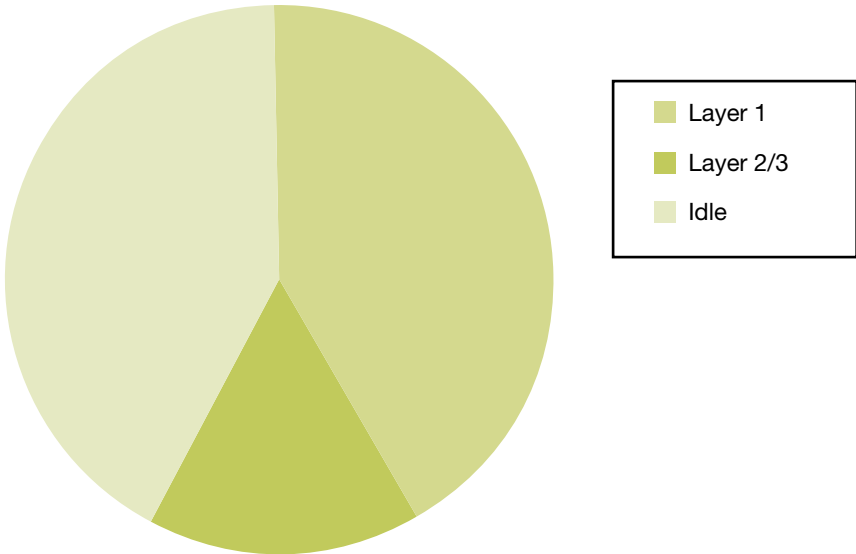
4.1.1 SINGLE-CORE MODEM

Using the newest generation DSP based on StarCore technology, the single-core modem (SCM) complex performs all the signaling protocol layers (L1, L2 and L3) for 2.5G, 2.75G and 3G (WCDMA, UMTS) standards. The performance needed to support high-speed wireless data is achieved by using a combination of embedded NVM and RAM. The architecture incorporates an L1 cache to improve performance when using slower memory systems. The cache also saves power by reducing the frequency of accesses to the memory system.

Access to the external shared memory assures system designers that they can expand the modem software to include support for multiple wireless access protocols in a single design. Alternatively, the memory expansion capability can be used to leverage the DSP to perform advanced features, such as audio codec functions or voice recognition processing. The result is a flexible multimode modem with low current drain characteristics to achieve best-in-class standby time.

The DSP based on StarCore technology runs at clock frequencies up to 208 MHz and features four MACs and two address generation units capable of executing six instructions per clock cycle. This capability provides an extra margin of performance to go beyond meeting minimal radio channel processing requirements. For example, this additional performance can be used to enhance channel equalization and error correction, which can be a differentiator in the marketplace. Another application could be an enhanced parametric audio equalizer tailored to match the unique acoustic characteristics of speakers, transducers and headsets. Figure 8, shows a profile of the task loading for the DSP based on StarCore technology operating at 156 MHz and supporting an EDGE Class 12 connection (4 dn, 1 up). In this example, all L2 and L3 protocol tasks are executed from an external memory through the L1 cache. The amount of DSP idle time in this example profile was 41 percent, and this reserve performance is available to support other applications.

Figure 8. Estimated DSP Based on StarCore Technology Task Loading for EDGE Class 12 (4 dn, 1 up)



The margin of reserve performance and shared memory system also enable the DSP to support alternative wireless connectivity options, such as Bluetooth and WLAN networking without adding further processing capability to the architecture.

The StarCore programming environment features a memory management unit (MMU) for memory protection with optional support for virtual memory. This enables the DSP to have access to the external shared memory space for the efficient (low overhead), high-bandwidth interprocessor communication that is needed to support next-generation wireless networks.

The software architecture for the DSP incorporates an RTOS that is optimized for StarCore and for the needs of real-time signal processing environments. A proven C compiler with provisions for in-line assembly assures the developer of an efficient solution while meeting short time to market windows. Our experience in wireless communications systems enables us to offer a proven communication stack solution for GSM, GPRS, EDGE and 3G (WCDMA).

4.1.2 DEDICATED APPLICATION PROCESSOR CORE

An ARM1136 core operating at 400 MHz with 128 KB of on-chip L2 cache and a full complement of peripherals provide a dedicated application processor environment that surpasses the performance of discrete application processors on the market today. Figure 9 and Figure10, show the performance advantage of the L2 cache when executing from an external SDRAM or from a combination of Flash and SDRAM, respectively.

Figure 9. Comparison of Application Processor Performance with 133 MHz SDRAM

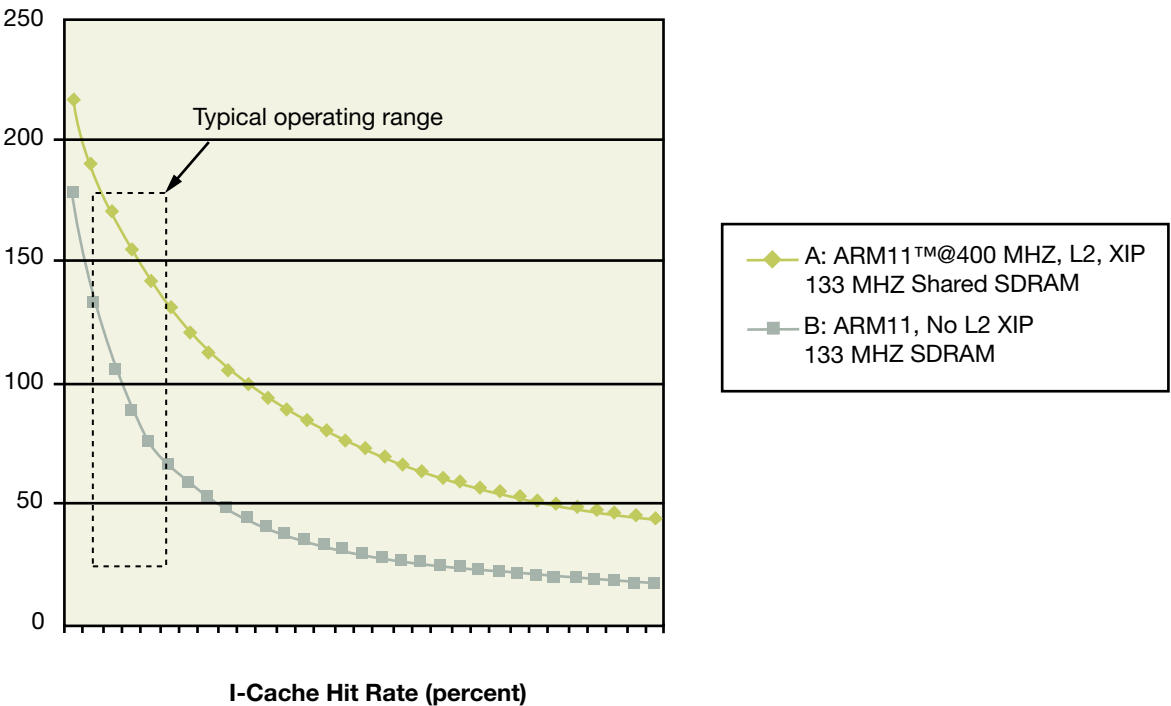
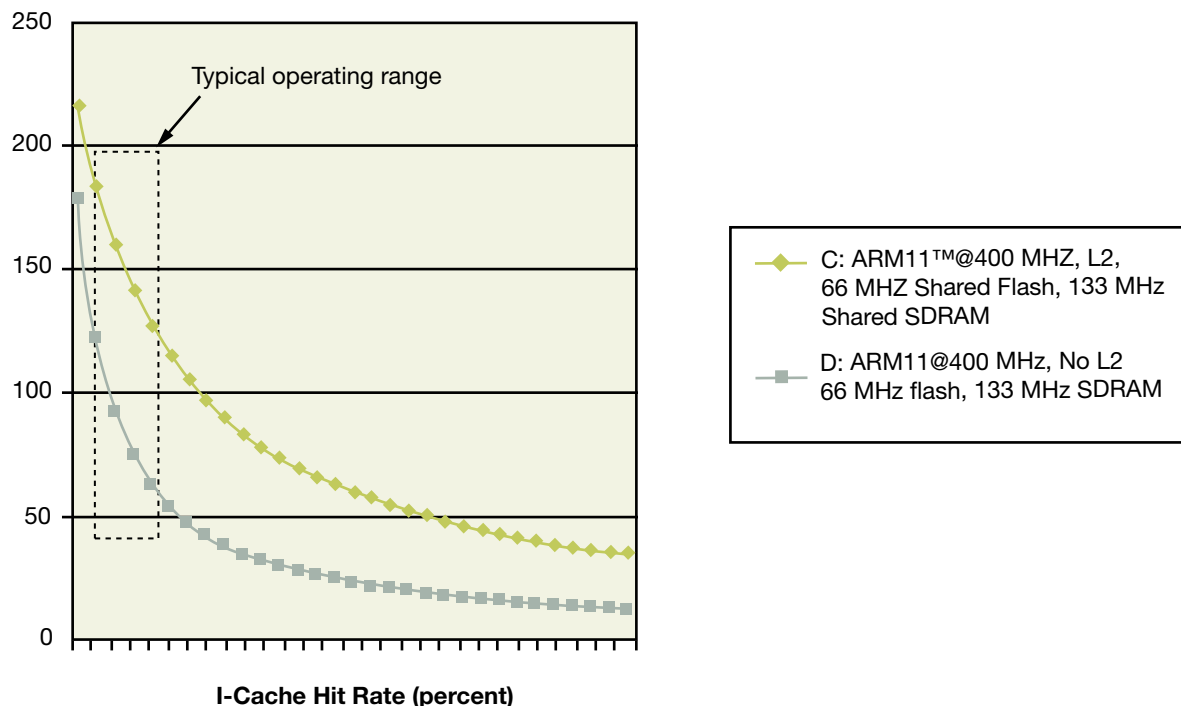


Figure 10. Comparison of Application Processor Performance with 66 MHz Flash and 133 MHz SDRAM



Curve A in Figure 9, and curve C in Figure 10, illustrate the performance characteristics of the ARM1136 core with L2 cache operating in a shared memory environment. In this case, the memory bandwidth demand of the ARM1136 core is shared with the memory bandwidth demand of the DSP executing L2/L3 software in an EDGE Class 12 scenario. By comparison, Curve B in Figure 9, and curve D in Figure 10, illustrate the ARM1136 core without L2 cache and operating as a discrete application processor without the side effect of the shared memory. Note that Figure 9, represents execution from a single 133 MHz SDRAM while Figure 10, represents program execution from a 66 MHz NOR Flash with data transactions to a 133 MHz SDRAM. The system parameters used in the profile are listed in Appendix A.

Figure 9 and Figure 10, demonstrate a performance improvement of better than 145 percent and 152 percent, respectively, for an ARM® core equipped with an L2 cache, compared to the same core without the L2 cache. This performance advantage includes the side effect of sharing the external memory system with the DSP. The DSP operating mode profiled in this case is an EDGE Class 12 packet data scenario.

The peripheral set for the ARM1136 core supports a variety of smart and dumb LCD panels, as well as image sensors. A variety of external connectivity options is supported, including USB 2.0, MMC/SD, and SDIO. The peripherals are supported by a flexible DMA engine containing 32 independent channels, which ensures that the developer can meet the complex usage scenarios needed in the next generation of converged products and applications.

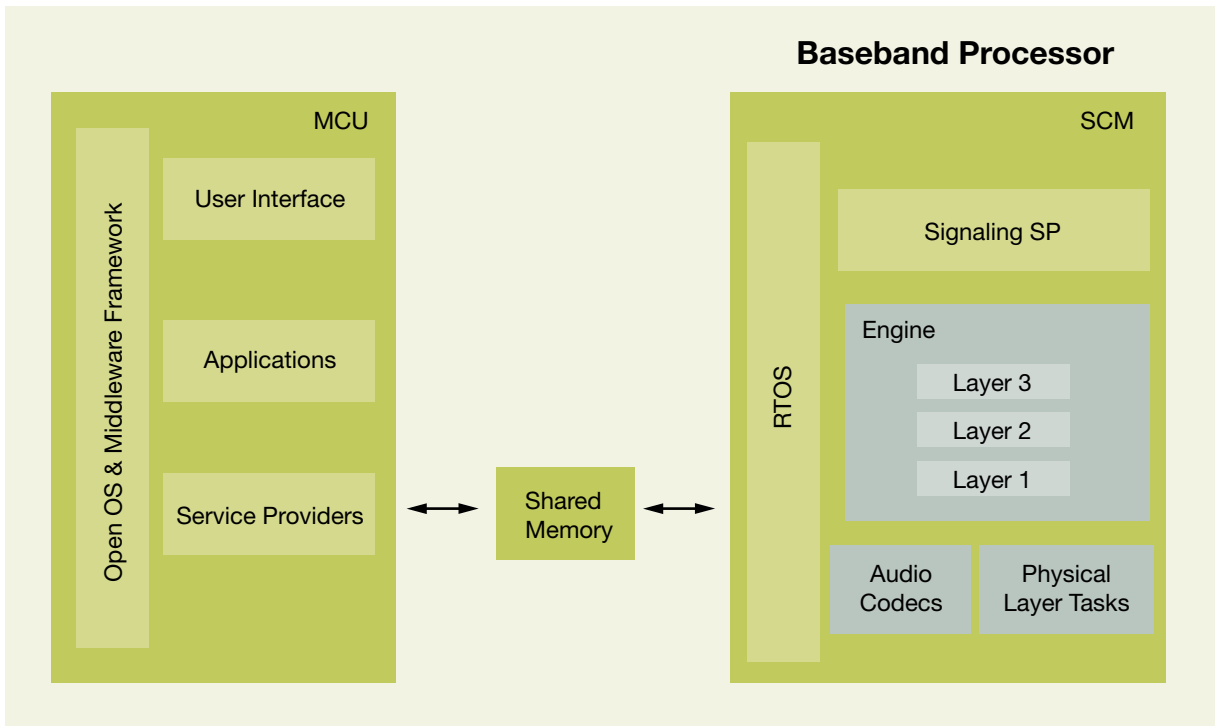
Adopting the single-core modem concept and incorporating the ARM1136 core with L2 cache eliminates the need to compromise the application environment with low-level wireless communication protocol tasks. This assures the developer a responsive multimedia environment, reducing the effort to bring intensive multimedia and gaming applications to the market. The ARM1136 core complex and peripheral set is designed to support Linux OS, Microsoft® Pocket PC, Microsoft SmartPhone, Palm OS, and Symbian OS. A complete support package of optimized codecs, graphic libraries and multimedia libraries is available.

The system designers placed special emphasis on multimedia applications when defining the MXC architecture. The high performance of the ARM1136 core with L2 cache is augmented by a scriptable Bit-Blit engine for 2-D graphics, a floating point coprocessor for 3-D graphics and a flexible hardware image processor that eliminates the intense software workload on the application processor when rendering viewfinder images. This results in longer battery life while preserving MCU performance for user applications.

4.1.3 SOFTWARE ARCHITECTURE

MXC smartphone software architecture envisions the complete protocol stack (L1 through L3) executing on the SCM. The MCU is completely available for applications. In the streamlined architecture, as shown in Figure 11, the single-core modem handles all modem processing, with call signaling and audio codecs.

Figure 11. Mobile Extreme Convergence Smartphone Software Architecture



Because the L2 and L3 protocol layers in the traditional dual architecture require a small amount of processing power (~15 MIPS), the average MIPS requirement for the DSP to handle modem tasks does not change significantly. However, the real-time system performance (peak MIPS requirement) in this architecture must handle additional tasks without sacrificing the time criticality of the protocol stack. This is addressed with a real-time operating system, running on the SCM, with preemptive multitasking capabilities. This architecture can be extended to handle the MAC software of various wireless connectivity protocols in the DSP. The services—telephony, file management, power management, multimedia, security, etc.—are provided by the application environment under an open OS running on the MCU. The clean separation of the applications, with the service providers, from the protocol stack makes the open OS adaptation library and the interprocessor communication much simpler, more optimized and easier to implement.

The software design of the MXC architecture provides the following benefits to software developers:

- **Separation**—The software separation allows the application environment and the modem environment to be developed independently and each on a single core. This simplifies the development, with one tool suite, one OS interaction and one debug view. Applications developed for open OS environments can be easily ported across a variety of mobile products, reducing development cycle time for shorter time to market.
- **Simplicity**—The reduced complexity is realized by having fewer cores in the system regardless of wireless connectivity. A single interface between two cores through a simple shared memory system for all wireless protocols greatly reduces the software complexity. The architecture provides a simplified software development environment with high-level language programming based on a standardized set of well-documented application programming interfaces (APIs). These high-level APIs allow application and content to be developed without making direct calls to the underlying platform hardware.
- **Secure connectivity**—A plug-and-play environment is crucial to ease of development. The MXC software architecture enables the application environment to plug into any connectivity solution suitable for the target-converged product. This again simplifies development, and the built-in security enhances the usability of this flexible wireless connectivity.
- **Uniformity**—Taken together, the separation, simplicity and secure connectivity provide a uniform application software development opportunity over all wireless global and local protocols, reinforcing from the software perspective the infinite possibilities to develop once and deploy anywhere.

4.1.4 SMART SYSTEM POWER MANAGEMENT

The MXC architecture places a major emphasis on minimizing power consumption for both active and standby modes. Among its goals is achieving the same standby time as today's voice-only cellular telephones, with the memory capacity and performance capability of tomorrow's smart mobile devices. This goal required a holistic approach to system design in addition to implementing best-in-class gate level design and process parameter selection.

At the circuit level, the MXC architecture applies best-in-class design practices including dynamic voltage scaling (DVS), clock gating and low leakage process in order to obtain the lowest standby power for long battery life.

At the system architecture level, the single-core modem partition provides significant benefit in power reduction by eliminating the need to have more than one processor involved in processing the communication stack. The memory and cache design for the DSP based on StarCore technology was optimized by profiling the protocol stack behavior for a variety of connection states to determine how to achieve lower power consumption. The result is an efficient implementation for all protocol layers (L1, L2, L3), as can be seen in Table 1.

Table 1. Minimum Required DSP Clock Rates

Call Scenario	Minimum Required Clock Rate (MHz)
GSM Voice (EFR)	39
GPRS Class 8	78
EDGE Class 12	104

The operating characteristics of the ARM1136 and the DSP based on StarCore technology for three clock rates are shown in Table 2.

Table 2. Operating Voltage Versus Vdd

Processor	Low	Medium	High
ARM1136	1.2V @ 399 MHz	1.4V @ 466 MHz	1.6V @ 532 MHz
DSP based on StarCore technology	1.2V @ 208 MHz	1.4V @ 225 MHz	1.6V @ 250 MHz

4.1.5 BEST-IN-CLASS SYSTEM MEMORY SUPPORT

The MXC architecture pays special attention to the support and implementation of system memory, as it represents large part of the product cost. The MXC architecture supports a variety of system memory configurations including: SDRAM, DDRAM, NOR Flash, SRAM, CellularRAM(tm) memory and NAND Flash. An on-chip NAND Flash controller relieves the processor core from the burden of performing error-correction and wear-leveling. The external memory bus provides support for x8, x16 and x32 bus widths, including mixed bus width configurations.

Unlike other offerings, the MXC architecture supports a 1.8-volt memory I/O to achieve low power while maintaining high performance. The I/O power savings can be as much as 70 percent when compared to systems using 3.3-volt I/O. This feature, combined with the on-chip L2 cache, offers lower power consumption and higher MIPS per milliwatt compared to the other products using L1 caches with 3.1 I/O.

4.1.6 MULTIMODE CONNECTIVITY: PAN, LAN, WAN

The MXC architecture overcomes the disadvantages of managing separate modems for each wireless network type. As described in the “4.1.1 Single-Core Modem” the margin of reserve performance and the shared memory system enable the DSP to support alternative wireless connectivity options, such as Bluetooth and WLAN networking, without needing to add further processing capability to the architecture.

A significant reduction in the complexity of interprocessor communications is achieved by using the on-chip resources provided by the MXC architecture to support multiple wireless networks. The need to serialize the data and to multiplex multiple traffic and control streams onto a single interface is eliminated completely. The efficient shared memory model featured in the MXC architecture provides a high bandwidth interface with multiple endpoints for each wireless network, which simplifies real-time control and avoids the conflicts and complexities associated with serialization. The result is a simpler interface that is easier to test, consumes less power and provides extra value for the customer in terms of performance and battery life.

The connectivity interface supported in the MXC architecture supports legacy interfaces, such as HCI for Bluetooth technology and IP/Ethernet interworking adaptation for WLAN. The lower layers of these interfaces are simplified to eliminate the serialization aspects and take advantage of shared memory. Future development plans call for an enhanced interface that unifies the software interfaces across a variety of wireless networks. This method of abstraction offers the potential providing applications with a single set of APIs to access all wireless connectivity networks supported on the product.

4.1.7 LOCATION SERVICES

The need to support E911 and the increase in location-based applications using GPS will add yet another processing complex to today's smartphone architectures. The cost and space of these additional processing resources can be alleviated by leveraging the reserve processing capability provided by the DSP based on StarCore technology. The benefit of a cache-based DSP and shared system memory enables an easy upgrade path.

4.1.8 FEATURE SUMMARY

- Single-chip smartphone complex features dedicated ARM11 processor and Single-Core Modem
- Scalable single-core modem supports GSM, GPRS, EDGE Class 12 and WCDMA (3G); support for Bluetooth and WLAN networking is also available
- On-chip, dedicated application processor: ARM1136 @ 400 MHz with 128 KB on-chip L2 cache
- ARM Jazelle(tm) technology for Java(tm) hardware acceleration
- Floating point coprocessor for 3-D graphics
- Programmable (scriptable) Bit-Blit engine
- Hardware support renders viewfinder image from image sensor
- DSP based on StarCore technology with clock speeds up to 208 MHz with four MACs and two AGUs. Up to six instructions per clock cycle delivers over 1,200 peak MIPS.
- Efficient shared system memory provides flexibility to partition tasks between MCU and DSP; support for 1.8-volt I/O saves power; support for SDRAM, DDRAM, SRAM, CellularRAM memory, NOR Flash, NAND Flash
- Reserve performance capability of DSP enables a variety of wireless connectivity options
- Optional support for GPS
- Strong security model: encryption/decryption accelerators, secure boot, restricted access (protected) key management and memory boundary protection
- Flexible LCD display controller supports smart and dumb color LCD panels with sizes ranging up to VGA
- Application processor peripherals include: USB 2.0, MMC/SD, SDIO, I2C, SSI, SPI, UARTx2, GPIO, keypad, IrDA, and external interrupts
- Hardware-compliant application processor platform supports Linux OS, Microsoft Pocket PC, Microsoft SmartPhone, Palm OS, and Symbian OS
- Low power design: DVS, clock gating and low leakage process assures maximum possible standby time; single-core modem eliminates the need for application processor to support mobility management functions; only the DSP core is used to monitor paging channel
- 32 independent DMA channels support a variety of traffic models
- Optimized codecs, multimedia and security libraries available
- Proven communications stack for GSM, GPRS, EDGE and 3G (WCDMA) available for license

4.2 SYSTEM SECURITY

Freescall has applied its experience in secure wireless systems for military and public services to the definition of the MXC architecture. This architecture represents the next generation in system security, comprising both hardware and software required for a wide range of security services and applications. The security framework has a significant intellectual property lineage, derived from Freescall's more than 200 security patents. Secret-key management functions are supported with an isolated on-chip memory that requires authentication to gain access. An on-chip unique hardware ID number is also provided. A secure on-chip boot ROM performs code image validation and is used to establish a point of trust for the application processor environment. Access to on-chip debug facilities can be disabled to prohibit intrusion.

The high assurance boot comprises three elements, including public key infrastructure, a hash function and a component that enables the digital signature calculation. The high assurance boot enables the Flashed code to be verified for integrity before being loaded by the mobile device. The SHA-1 hash accelerator provides a hash or message digest for large memory spaces and supports the digital signature process required for authentication and nonrepudiation. The security control module includes a secure RAM module and security monitor. The secure RAM module has a number of elements, primarily a 168-bit secret key and triple DES encryption, used to prepare sensitive data (passwords, credit card numbers) for off-processor storage. In addition, it provides temporary on-processor storage of decrypted results for real-time use. The security monitor comprises system monitor functions and security support tasks to ensure that secure modes are established and maintained in the processor. These cryptography building blocks are composed to form the complete gamut of security services and applications ranging from low value transactions, through the protection of intellectual property via digital rights management (DRM), to secure, high-value transactions required by enterprises worldwide.

The single-core modem concept provides an addition measure of system security and integrity by isolating the wireless networking portions of the protocol stack onto the DSP and away from the application processor. This partitioning scheme minimizes the exposure of critical low-level communications protocol layers from being modified or corrupted by computer viruses that are prevalent in today's networks. The shared system memory is boundary-protected by a hardware firewall to secure the DSP communications software.

4.3 SMALL FOOTPRINT

The MXC vision encompasses technologies required to realize this new architecture in a single package—a package whose area is less than a 0.5-square inch. The complete package is an assembly of subsystems:

- MXC IC consisting of single-core modem processing core and application processing core
- Memory
- RF/PA
- Power management

This partitioning enables each module to be tested prior to final assembly, optimizing assembly yield and cost.

The interconnect makes direct connection to the IC bond pads. This creates a convergence of the interposer and wire bond or solder bump interconnect found in conventional semiconductor packages and reduces the size and cost of the package.

The interconnect provides:

- One-mil lines and spaces that interconnect the memory and processors in minimal area
- Optimum performance for the RF circuit, with a dielectric constant of 2.0 and a loss tangent <0.002
- Integrated Faraday cages that isolate the RF and digital circuits
- Low inductance power and ground planes directly over the chips, which form a part of the Faraday cages and deliver noise-free power

The high performance interconnect, in conjunction with the close proximity of the processors and memory, allows the application and baseband processing cores to share the memory, further reducing the cost of the smartphone.

A device based on the MXC design can incorporate a broad range of passive technologies within the package, eliminating external passive components. These passive technologies include surface mount components, custom resistor-capacitor substrates and high performance inductors designed in the interconnect. Freescale will leverage its leadership in multiple process technologies with the use of this approach, using optimal technology for each individual function within the package. Freescale's vision of MXC can result in a final product that converges all of the electronics for a complete cell phone into a single component that minimizes design time, reduces overall phone size and enables the incorporation of more smart features in converged mobile devices.

5. Mobile Extreme Convergence Benefits

Consumers have come to expect better value in terms of features, performance and improved battery life, every time they renew a piece of equipment, such as a smartphone, for the same price. And with new categories of devices, the expectations will be even higher. MXC architecture offers cellular phone OEMs and carriers the capability to meet the challenges and expectations of tomorrow's mobile user. Incorporating more features in a smaller, integrated package reduces complexity, which results in a lower bill-of-material cost than other, more traditional, approaches. It can reduce OEMs time to market for new converged mobile products by as much as six months and allow software developers to deploy applications across a broad range of devices.

- **Security designed-in**—Freescale's security systems framework, which is employed in the MXC architecture, can adapt to, respond to and overcome new threats as they emerge. Optimized for secure mobile communications and transactions, the MXC architecture addresses consumers' concerns about m-commerce, carriers' concerns with cloning, configuration protection and theft of services, and content providers' concerns regarding digital rights management.
- **Seamless connectivity for users**—With the advances provided by the MXC architecture, anytime, anywhere communication will evolve to be anyone, anything connectivity. Sleek, fashionable phones morph into mobile wallets and universal remotes. Users need not care how their smart handhelds talk to other devices, only that it works, making their work easier and their lives simpler.
- **Smart power management**—The power management optimizations designed into the MXC architecture enable the far more sophisticated devices to run as long as voice-only phones today, enabling truly mobile, untethered use.
- **Lower costs, higher profits**—The reduction in complexity offered by the MXC architecture reduces the materials required to deliver a product, cutting bill-of-materials costs, making it possible to include smart connectivity in a wide range of devices, with higher margins, at lower prices. Consumers benefit from streamlined devices that do more, and operators benefit when consumers integrate these devices into their lives, actively using data-heavy services.

6. Conclusion

The marathon that is the mobile consumer's life requires the support of products based on a technology that delivers marathon battery life, peace-of-mind security, access to instant entertainment, anywhere-to-anything connectivity and industrial designs that deliver optimal usability for the application. The MXC architecture is just that—it combines smart integration driven by decades of wireless know-how with a clean application environment. There's no power struggle—both worlds function ideally. It converges Smart Speed performance with stamina technology with industry-leading security technology. It will allow manufacturers to converge this postage stamp-sized smartphone core with unique product designs and applications tailored to millions of unique market segments.

Appendix A

The system parameters for the ARM1136 performance profile shown Figure 9 and Figure 10, are provided in Table 3.

Table 3. System Parameters for ARM1136™ Performance Profile

Parameter	Value
MCU clock (MHz)	400
Average CPI	1.2
Cache line size (bytes)	32
External memory bus width (SDRAM and Flash)	x16
SDRAM access parameters	6–1 @ 133 MHz
Average SDRAM page hit rate percentage	33
Flash access parameters	6–1 @ 66 MHz
Average Flash page hit rate percentage	0
Primary data cache miss rate percentage	10
Load/store rate percentage	30
L2 cache line size (bytes)	32
L2 cache “I” average hit rate percentage	70
L2 cache “D” average hit rate percentage	70

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