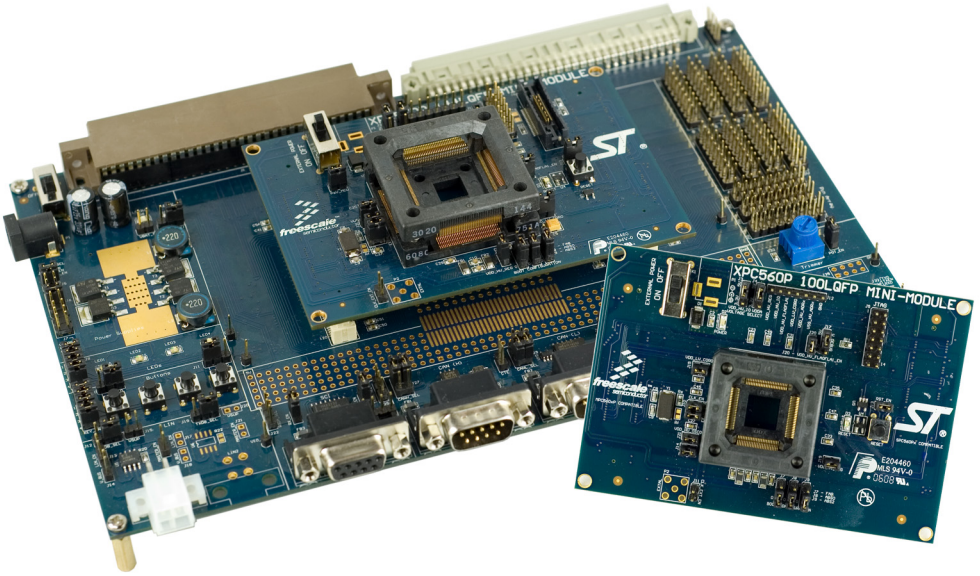
XKT560P EVB User Manual



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1 OVERVIEW

The XKT560P EVB is an evaluation system supporting Freescale MPC560xP microprocessors. The complete system consists of an xPC56XXMB Motherboard and an XDC560P Mini-Module which plugs into the motherboard. Different Mini-Modules are available for evaluating devices with different footprints in the MPC560xP family of microprocessors. The evaluation system allows full access to the CPU, all of the CPU's I/O signals, and the motherboard peripherals (such as CAN, SCI, LIN). The Mini-Module may be used as a stand-alone unit, which allows access to the CPU, but no access to the I/O pins or any motherboard peripherals.

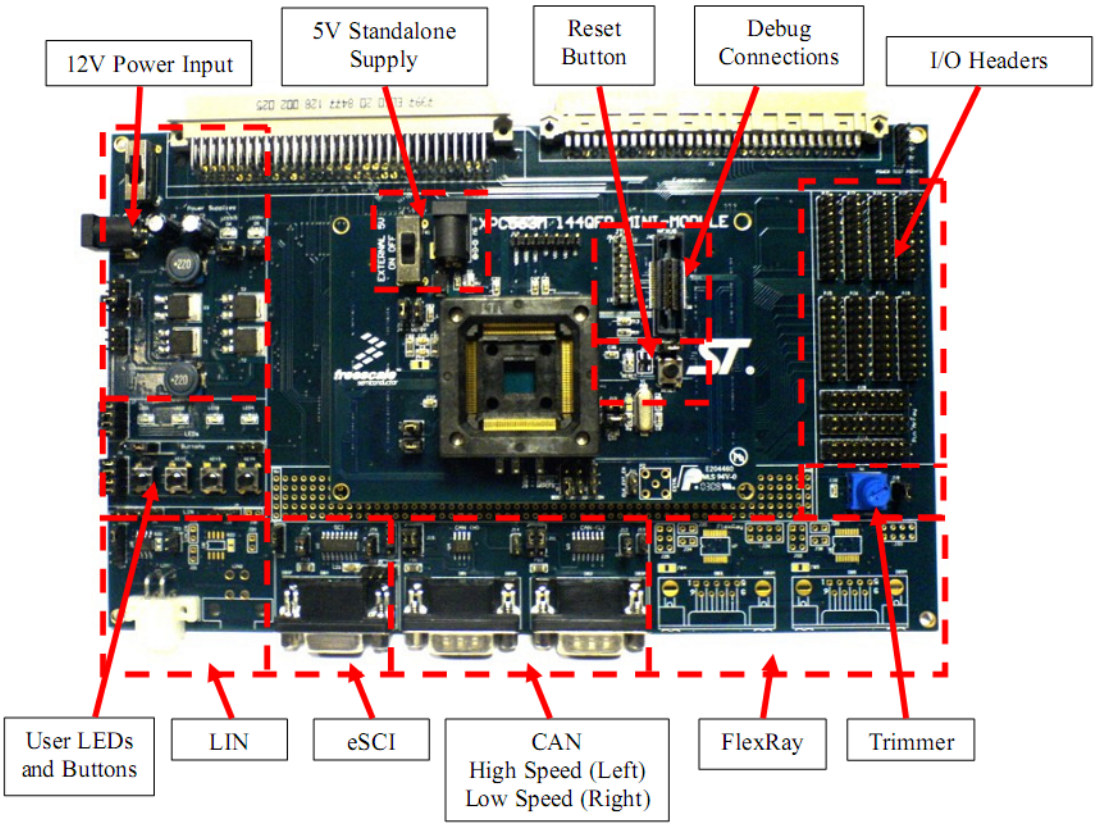


Figure 1-1: Overview of the XKT560P EVB

1.1 Package Contents

An XKT560P Evaluation Kit includes the following items:

- One xPC56XXMB Motherboard
- One XDC560P100S or XDC560P144S Mini-Module
- One xPC56XX Resources CD-ROM
- One P&E USB-ML-PPCNEXUS Hardware Interface Cable
- One USB A-to-B Cable
- Freescale Warranty Card

An XDC560P Adapter Package includes the following items:

- One XDC560P100S or XDC560P144S Mini-Module
- One xPC56XX Resources CD-ROM
- Freescale Warranty Card

1.2 Supported Devices

The XDC560P100S Mini-Module supports the following devices:

- MPC560xP (100LQFP Package)

The XDC560P144S Mini-Module supports the following devices:

- MPC560xP (144LQFP Package)

1.3 Recommended Materials

- Freescale MPC5604P reference manual and datasheet
- xPC56XXMB schematic
- XDC560P100S schematic
- XDC560P144S schematic

1.4 Handling Precautions

Please take care to handle the package contents in a manner such as to prevent electrostatic discharge.

2 HARDWARE FEATURES

The XKT560P EVB is an evaluation system for Freescale's MPC560xP microprocessors. A 38-pin Mictor Nexus port and/or a 14-pin JTAG port are provided on the Mini-Module to allow usage of an external PowerPC Nexus interface such as P&E USB-ML-PPCNEXUS cable and Cyclone MAX automated programmer.

2.1 xPC56XXMB Board Features

- ON/OFF Power Switch w/ LED indicators
- A 12VDC power supply input barrel connector
- Onboard STMicroelectronics L9758 regulator provides three different power voltages simultaneously: 5V, 3.3V, and 1.2V
- Onboard peripherals can be configured to operate at 5V or 3.3V logic levels
- Two CAN channels with jumper enables
  - One CAN channel with High-Speed transceiver and DB9 male connector
  - One CAN channel with Low-Speed Fault Tolerant and High-Speed transceiver (selectable with jumpers) and DB9 male connector
- Two LIN channels with jumper enables
  - One channel with transceiver and pin header connector populated
  - One channel with footprints only
- One SCI channel with jumper enables
  - Transceiver with DB9 female connector
- Two FlexRay channels with jumper enables
  - One channel with transceiver and DB9 male connector
  - One channel with footprint only
- Four user push buttons with jumper enables and polarity selection
- Four user LED's with jumper enables

- One potentiometer for analog voltage input
- Pin array for accessing all I/O signals
- Expansion connectors for accessing all I/O signals
- Development zone with 0.1” spacing and SOIC footprint prototyping
- Specifications:
  - Board Size 5.5” x 9.0”
  - 12VDC Center Positive power supply with 2.5/5.5mm barrel connector

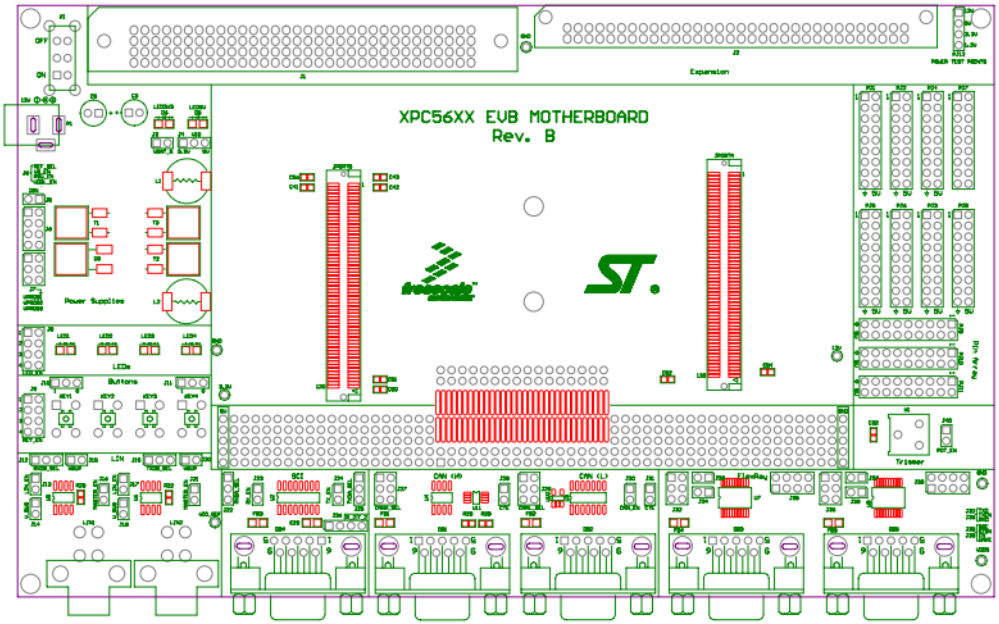


Figure 2-1: xPC56XXMB Top Component Placement

2.2 XDC560P Mini-Module Board Features

- Can be used as a stand-alone board by providing external 5V power supply input
- ON/OFF Power Switch w/ LED indicator

- Reset button with filter and LED indicator
- XDC560P100S has socket for MPC560xP in 100LQFP footprint
- XDC560P144S has socket for MPC560xP in 144LQFP footprint
- Debug ports: 38-pin Mictor Nexus port and/or 14-pin JTAG port
- Direct clock input through SMA connector (footprint only)
- Jumpers for boot configuration

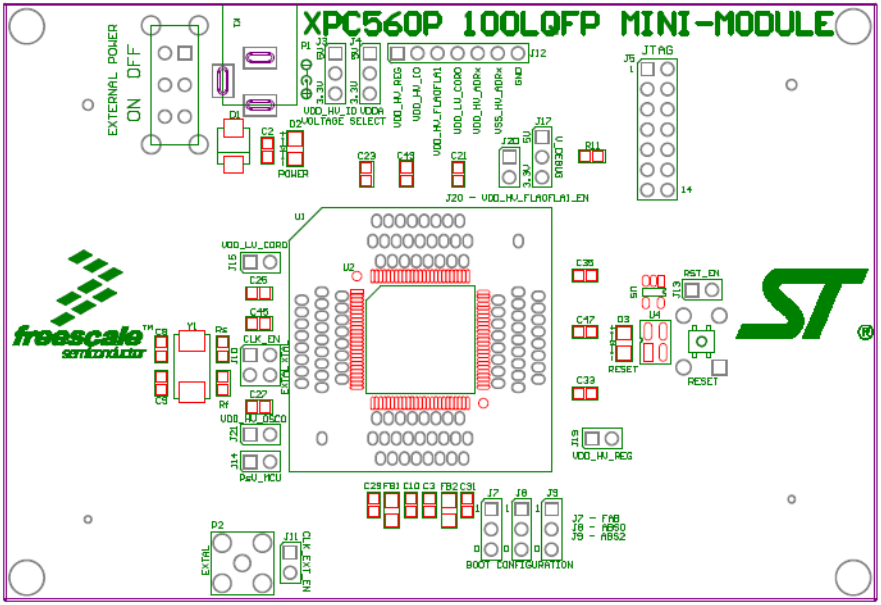


Figure 2-2: XDC560P100S Top Component Placement

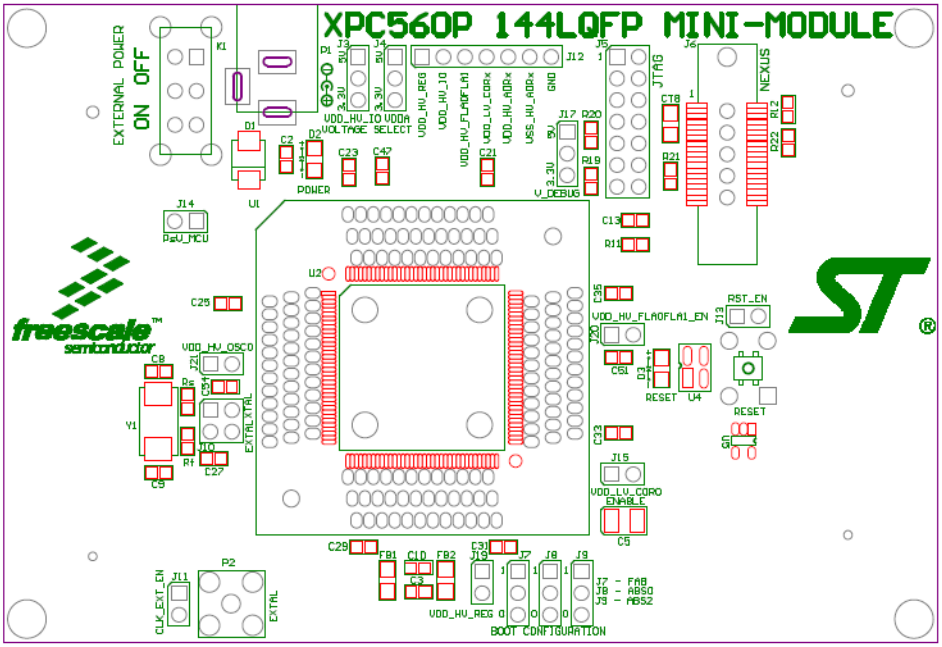


Figure 2-3: XDC560P144S Top Component Placement

2.3 Pin Numbering for Jumpers

Jumpers for both the xPC56XXMB motherboard and the XDC560P Mini-Modules have a rounded corner to indicate the position of pin 1. See examples below for the numbering convention used in this manual for jumper settings.

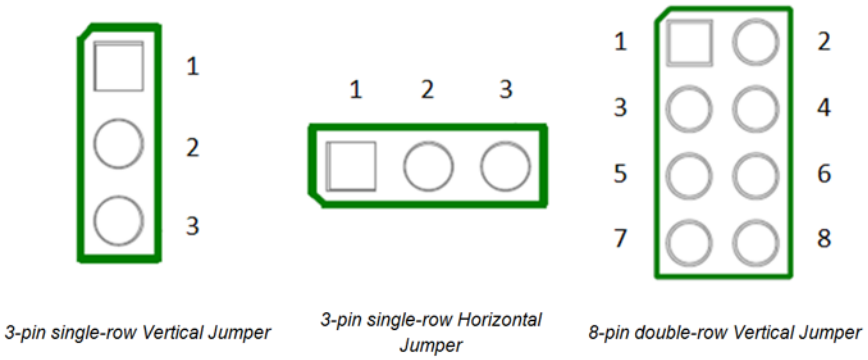


Figure 2-4: Pin Numbering

3 xPC56XXMB HARDWARE & JUMPER SETTINGS

Please note that this section of the manual is written for revision B and C of the xPC56XXMB motherboard. Revision B motherboards are indicated by the “Rev. B” silkscreen text in the center of the motherboard, and Revision C motherboards are indicated by the “Rev. C” silkscreen text in the center of the motherboard.

Revision A motherboards have different jumper numbers. These differences can be found in the table below:

Revision A	Revision B	Revision C	Jumper Description
J3	J6, pins 1+2	-	VSA Tracking Regulator Configuration
-	-	J3	Slew Rate Select
J4	J7	J7	VPROG Regulators Control
J5 (pins 1+2)	J5	-	IGN Control
-	-	J5	Power Reset Pullup Voltage Select
J5 (pins 3+4, 5+6, 7+8)	J6, pins 3+4, 5+6, 7+8	-	Regulators Enable & Standby
-	-	J6	Power Reset Output Enable
J36	J4	J4	VIO Peripherals Logic Level
J37	J3	-	VBat low voltage detection
-	-	J41	Power Reset Pullup Enable
J7	J8	J8	LEDs Enable
J8	J9	J9	Buttons Enable
J9	J10	J10	Buttons Driving Configuration

J40	J11	J11	Buttons Idle Configuration
J22	J13	J13	LIN1 enable
J24	J14	J14	LIN1 VBUS configuration
J6	J15	J15	LIN1 VSUP configuration
J23	J16	J16	LIN1 master selection
J28	J22	J22	LIN1/SCI RxD selection
J27	J25	J25	LIN1/SCI TxD selection
J19	J17	J17	LIN2 enable
J21	J18	J18	LIN2 VBUS configuration
J31	J20	J20	LIN2 VSUP configuration
J20	J21	J21	LIN2 master selection
J30	J12	J12	LIN2/SCI RxD selection
J29	J19	J19	LIN2/SCI TxD selection
J17	J23	J23	SCI RxD Enable
J16	J24	J24	SCI TxD Enable
J27	J25	J25	LIN1/SCI TxD selection
J28	J22	J22	LIN1/SCI RxD selection
J14	J28	J28	CAN (H) Transmit Enable
J15	J27	J27	CAN (H) TxD/RxD Enable
J13	J31	J31	CAN (L) CTE

J12	J30	J30	CAN (L) Enable
J11	J29	J29	CAN (L) TxD/RxD Enable
J25	J32	J32	FlexRay Bus Driver 1 Enable
J26	J35	J35	FlexRay Bus Driver 1 Configuration
J34	J34	J34	FlexRay 1 Terminal Resistor Connection
J35	J33	J33	FlexRay 1 Terminal Resistor Connection
J32	J36	J36	FlexRay Bus Driver 2 Enable
J33	J39	J39	FlexRay Bus Driver 2 Configuration
J38	J38	J38	FlexRay 2 Terminal Resistor Connection
J39	J37	J37	FlexRay 2 Terminal Resistor Connection
J18	J40	J40	POT Enable

3.1 Power Supplies

The xPC56XXMB obtains its power from the 12VDC Center Positive input barrel connector. The following jumpers are used to configure the power supply output:

J3 – VBat low voltage detection (Revisions A & B only)

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J3 – Slew Rate Select (Revision C only)

Jumper Setting	Effect
1+2	Regulator configured for fast slew rate
2+3	Regulator configured for slow slew rate
Off (default)	Regulator configured for medium slew rate

J4 – VIO Peripherals Logic Level

Jumper Setting	Effect
1+2	Onboard peripherals are configured for 3.3V logic
2+3 (default)	Onboard peripherals are configured for 5V logic

J5 – IGN Control (Revisions A & B only)

Jumper Setting	Effect
On (default)	The power regulator is always on
Off	If 5+6 is also OFF on J6, the power regulator is in standby

J5 – Power Reset Pullup Voltage Select (Revision C only)

Jumper Setting	Effect

1+2	If J41 is ON, regulator output reset is pulled up to 5V
2+3	If J41 is ON, regulator output reset is pulled up to 3.3V

J6 – Regulators Enable & Standby (Revisions A & B only)

Jumper Setting	Position	Effect
1+2	On	The ST L9758 tracking regulator VSA tracks the input voltage at its TRACK_REF pin.
	Off (default)	The ST L9758 tracking regulator VSA tracks 5V
3+4	On	VSB, VSC, and VSD tracking regulators are disabled
	Off (default)	VSB, VSC, and VSD tracking regulators are enabled
5+6	On (default)	The power regulator is always on
	Off	The power regulator is in standby if jumpers 1+2 are also in the “off” position
7+8	On	VDLL and VCORE regulators are disabled
	Off (default)	VDLL and VCORE regulators are enabled

J6 – Power Reset Output Enable (Revision C only)

Jumper Setting	Effect

On (default)	If regulator voltages fall below threshold, a reset is sent to the microprocessor
Off	No reset is sent to the microprocessor

J7 – VPROG Regulators Control (Revisions A & B)

Jumper Setting	Position	Effect
1+2	On	VKAM regulator output is programmed to 1V
	Off (default)	VKAM regulator output is programmed to 1.5V
3+4	On	VSTBY regulator output is programmed to 2.6V
	Off (default)	VSTBY regulator output is programmed to 3.3V
5+6	On	VDLL regulator output is programmed to 2.6V
	Off (default)	VDLL regulator output is programmed to 3.3V

J7 – VPROG Regulators Control (Revision C only)

Jumper 1+2	Jumper 3+4	Jumper 5+6	VDD3	VDDL	VKAM
Off	Off	Off	3.3 V	2.6 V	2.6 V
Off	Off	On	3.3 V	3.3 V	3.3 V
Off	On	Off	3.3 V	1.5 V	1.0 V

Off	On	On	3.3 V	3.3 V	1.0 V
On	Off	Off	3.3V standby	3.3 V	1.0 V
On	Off	On	2.0 V	3.15 V	5.0 V
On	On	Off	2.6 V standby	3.3 V	1.0 V
On	On	On	2.6 V standby	3.3 V	1.5 V

J37 – VBat low voltage detection

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J41 – Power Reset Pullup Enable (Revision C only)

Jumper Setting	Effect
On	Regulator output reset is pulled up
Off (default)	Regulator output reset is not pulled up

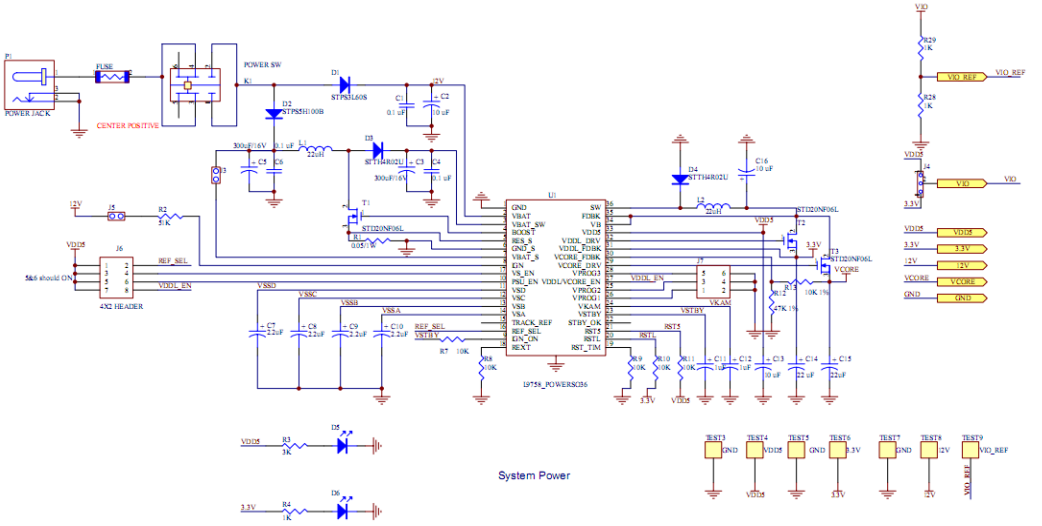


Figure 3-1: Power Supply circuitry schematic (Revisions A & B only)

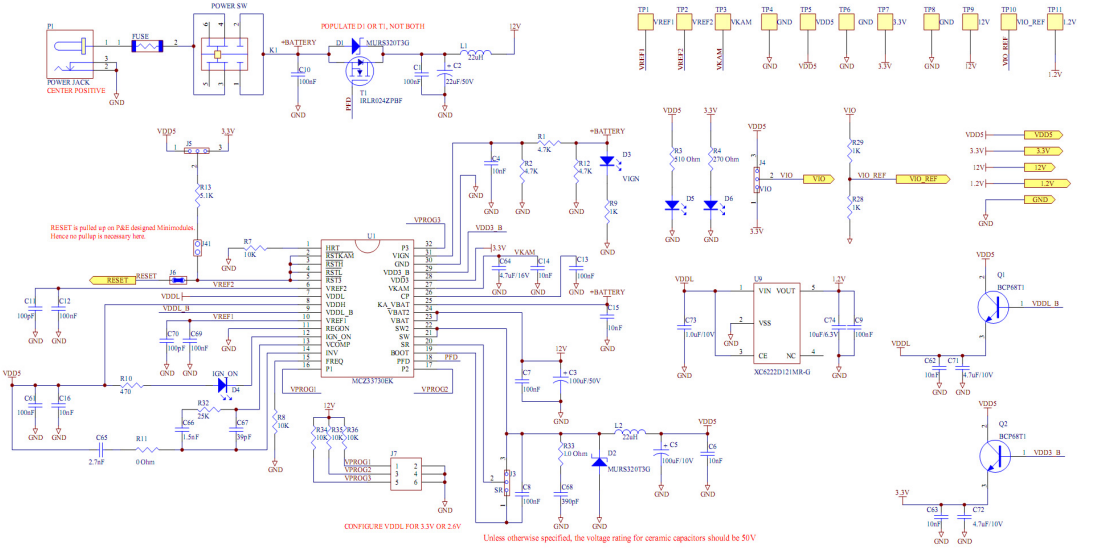


Figure 3-2: Power Supply circuitry schematic (Revision C)

3.2 LEDs

There are four user LEDs available on the xPC56XXMB. All LEDs are active low.

J8 – LEDs Enable

Controls whether the LEDs on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each LED to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	LED1 connected to D[4]
3+4 (default on)	LED2 connected to D[5]
5+6 (default on)	LED3 connected to D[6]
7+8 (default on)	LED4 connected to D[7]

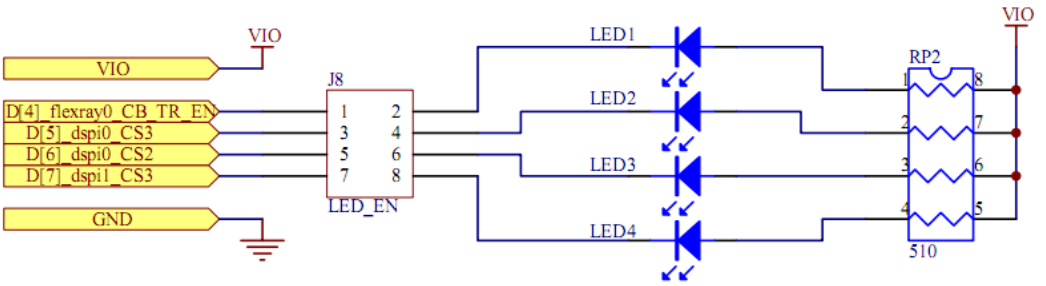


Figure 3-3: LEDs circuitry schematic

3.3 Buttons

There are four user buttons available on the xPC56XXMB.

J9 – Buttons Enable

Controls whether the buttons on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each button to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	KEY1 connected to D[0]
3+4 (default on)	KEY2 connected to D[1]
5+6 (default on)	KEY3 connected to D[2]
7+8 (default on)	KEY4 connected to D[3]

J10 – Buttons Driving Configuration

Selects whether the buttons drive logic high or drive logic low when pressed.

Jumper Setting	Effect
1+2	When pressed, buttons will send logic high to the connected I/O pin
2+3 (default)	When pressed, buttons will send logic low to the connected I/O pin

J11 – Buttons Idle Configuration

Selects whether the I/O pins are pulled logic high or pulled logic low. This controls the defaultlogic level of the I/O pins when the buttons are not

pressed.

Jumper Setting	Effect
1+2 (default)	I/O pins connected to the buttons are pulled up to logic high
2+3	I/O pins connected to the buttons are pulled down to logic low

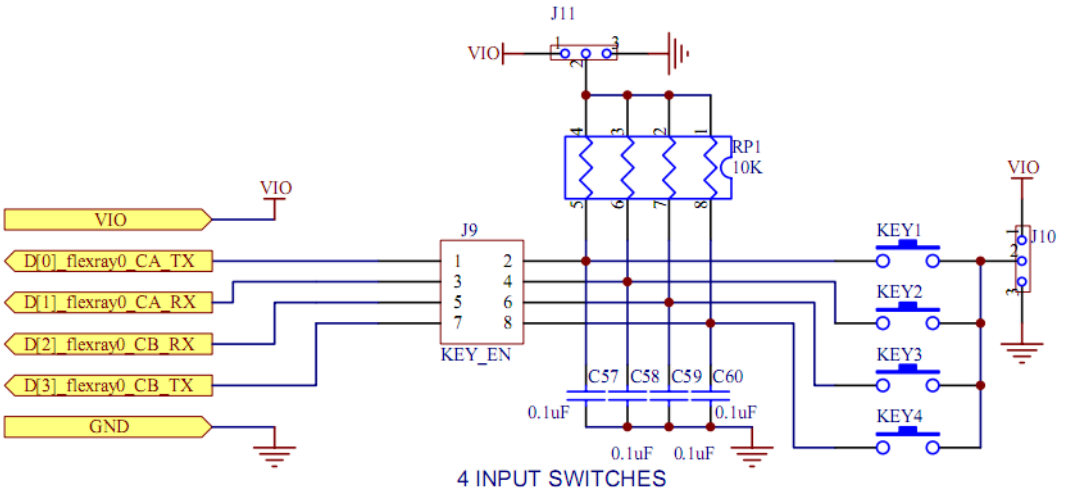


Figure 3-4: Buttons circuitry schematic

3.4 LIN

There are footprints for two LIN connections on the xPC56XXMB. By default, one LIN circuit is assembled (LIN1) and the other circuit is left unpopulated (LIN2).

J13 – LIN1 enable

Jumper Setting	Effect
On	Enables the LIN1 transceiver
Off (default)	Disables the LIN1 transceiver

J14 – LIN1 VBUS configuration

Jumper Setting	Effect
On	LIN1 VBUS is connected to 12V
Off (default)	LIN1 VBUS is not connected to 12V

J15 – LIN1 VSUP configuration

Jumper Setting	Effect
On	LIN1 VSUP is connected to 12V
Off (default)	LIN1 VSUP is not connected to 12V

J16 – LIN1 master selection

Jumper Setting	Effect
On	LIN1 is configured as a master node

Off (default)	LIN1 is configured as a slave node

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the “B[3]” pin on the MPC560xP processor. This should be set if enabling LIN1.
2+3	The SCI RxD pin is connected to the “B[3]” pin on the MPC560xP processor.

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the “B[2]” pin on the MPC560xP processor. This should be set if enabling LIN1.
2+3	The SCI TxD pin is connected to the “B[2]” pin on the MPC560xP processor.

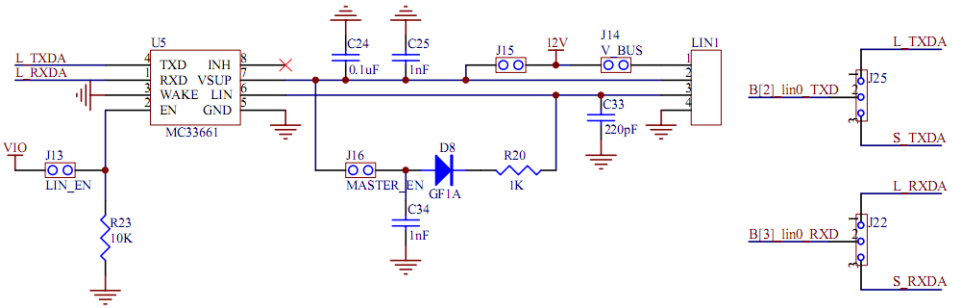


Figure 3-5: LIN1 Schematic

J17 – LIN2 enable

Jumper Setting	Effect
On	Enables the LIN2 transceiver
Off (default)	Disables the LIN2 transceiver

J18 – LIN2 VBUS configuration

Jumper Setting	Effect
On	LIN2 VBUS is connected to 12V
Off (default)	LIN2 VBUS is not connected to 12V

J20 – LIN2 VSUP configuration

Jumper Setting	Effect

On	LIN2 VSUP is connected to 12V
Off (default)	LIN2 VSUP is not connected to 12V

J21 – LIN2 master selection

Jumper Setting	Effect
On	LIN2 is configured as a master node
Off (default)	LIN2 is configured as a slave node

J12 – LIN2/SCI RxD selection

Controls whether the RxD pin on LIN2 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect
1+2	The LIN2 RxD pin is connected to the “F[15]” pin on the MPC560xP processor. This should be set if enabling LIN2.
2+3 (default)	The SCI RxD pin is connected to the “F[15]” pin on the MPC560xP processor.

J19 – LIN2/SCI TxD selection

Controls whether the TxD pin on LIN2 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect

1+2	The LIN2 TxD pin is connected to the “F[14]” pin on the MPC560xP processor. This should be set if enabling LIN2.
2+3 (default)	The SCI TxD pin is connected to the “F[14]” pin on the MPC560xP processor.

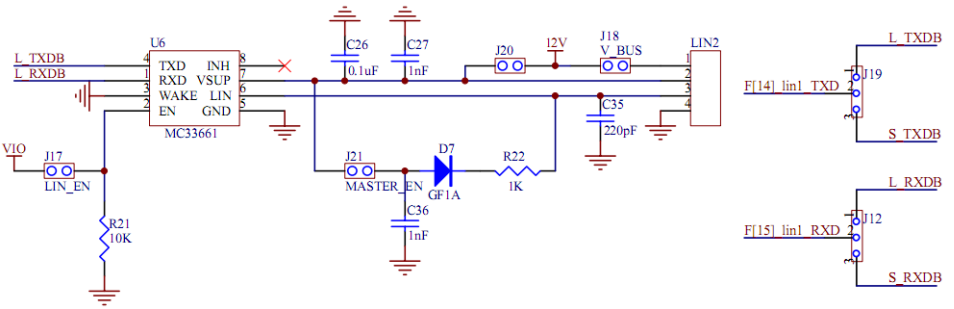


Figure 3-6: LIN2 schematic (Not populated by default)

3.5 SCI

One SCI interface is available on the xPC56XXMB.

J23 – SCI RxD Enable

Jumper Setting	Effect
On (default)	Enables SCI receive
Off	Disables SCI receive

J24 – SCI TxD Enable

Jumper Setting	Effect
On (default)	Enables SCI transmit
Off	Disables SCI transmit

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the “B[2]” pin on the MPC560xP processor.
2+3	The SCI TxD pin is connected to the “B[2]” pin on the MPC560xP processor. This should be set if enabling SCI.

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC560xP processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the “B[3]” pin on the MPC560xP processor.

2+3	The SCI RxD pin is connected to the “B[3]” pin on the MPC560xP processor. This should be set if enabling SCI.

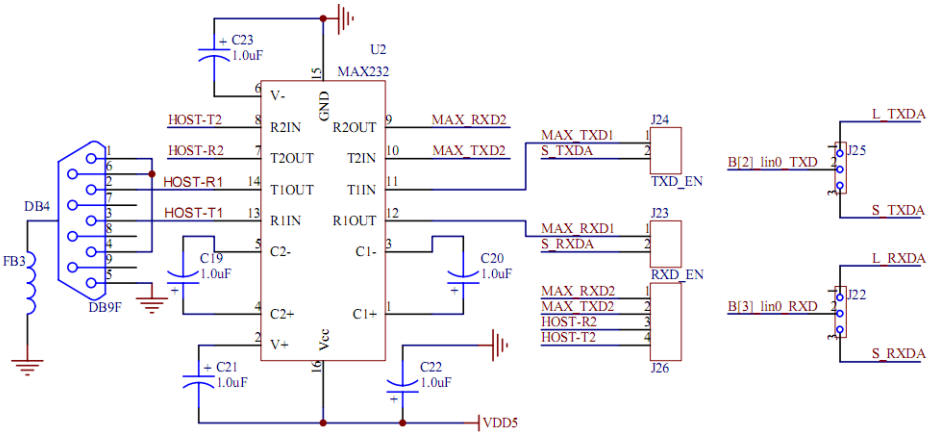


Figure 3-7: SCI schematic

3.6 CAN

Two CAN interfaces are implemented on the xPC56XXMB: a high-speed CAN interface and a low-speed CAN interface.

J28 – CAN (H) Transmit Enable

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J27 – CAN (H) TxD/RxD Enable

Controls which I/O pins on the MPC560xP processor are connected to the TxD and RxD pins on CAN (H). If CAN (H) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3 (default)	The RxD pin of the CAN (H) interface is connected to the “B[1]” pin of the MPC560xP processor.
3+5	The RxD pin of the CAN (H) interface is connected to the “A[15]” pin of the MPC560xP processor.
2+4 (default)	The TxD pin of the CAN (H) interface is connected to the “B[0]” pin of the MPC560xP processor.
4+6	The TxD pin of the CAN (H) interface is connected to the “A[14]” pin of the MPC560xP processor.

J30 – CAN (L) Enable

Jumper Setting	Effect
On (default)	Enables CAN transmission
Off	Disables CAN transmission

J31 – CAN (L) CTE

Jumper Setting	Effect

On	Enables CAN transmission
Off (default)	Disables CAN transmission

J29 – CAN (L) TxD/RxD Enable

Controls which I/O pins on the MPC560xP processor are connected to the TxD and RxD pins on CAN (L). If CAN (L) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3	The RxD pin of the CAN (L) interface is connected to the “B[1]” pin of the MPC560xP processor.
3+5 (default)	The RxD pin of the CAN (L) interface is connected to the “A[15]” pin of the MPC560xP processor.
2+4	The TxD pin of the CAN (L) interface is connected to the “B[0]” pin of the MPC560xP processor.
4+6 (default)	The TxD pin of the CAN (L) interface is connected to the “A[14]” pin of the MPC560xP processor.

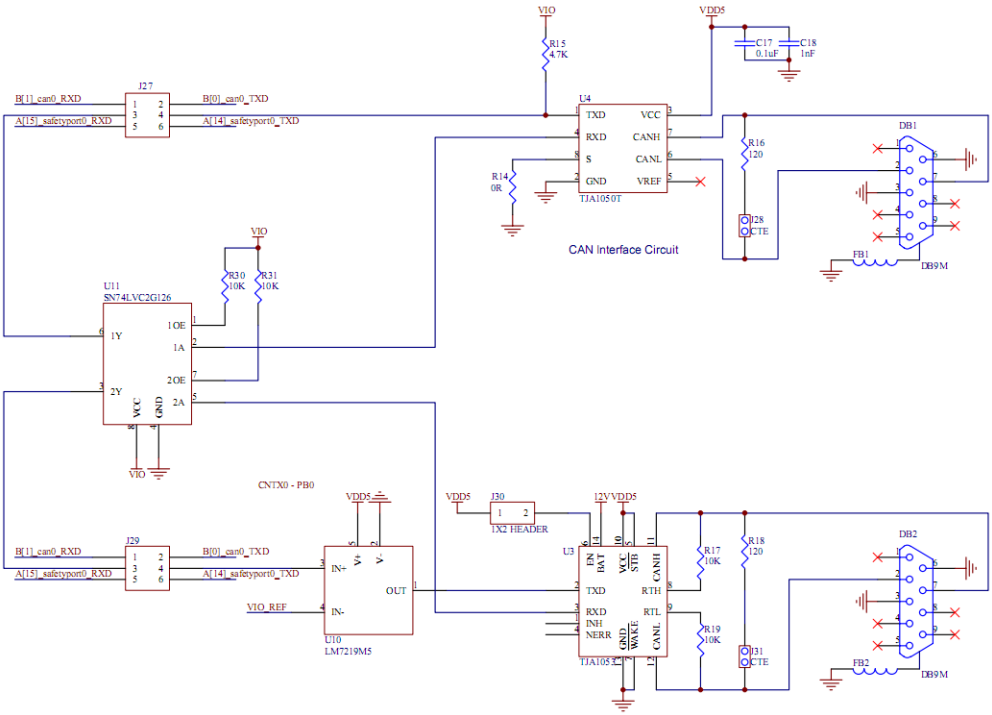


Figure 3-8: CAN schematic

3.7 FlexRay

The xPC56XXMB has footprints for two FlexRay interfaces. However, only one circuit is assembled by default. The FlexRay circuit is comprised of two DB9 connectors. DB3 contains signals for both FlexRay channels and is compatible with major FlexRay tools. DB5 contains the channel B signal, thereby also allowing 2 separate FlexRay connectors for channel A and channel B operation. Currently only the MPC560xP processors support FlexRay.

J32 – FlexRay Bus Driver 1 Enable

Controls which I/O pins on the MPC560xP processor are connected to the

TxD and RxD pins on FlexRay Bus Driver. It is recommended to remove the J40 jumpers to prevent signal distortion.

Jumper Setting	Effect
1+2 (default on)	The TXD pin on the FlexRay Bus Driver is connected to the “D[0]” pin on the MPC560xP processor.
3+4 (default on)	The TXEN pin on the FlexRay Bus Driver is connected to the “C[15]” pin on the MPC560xP processor.
5+6 (default on)	The RXD pin on the FlexRay Bus Driver is connected to the “D[1]” pin on the MPC560xP processor.

J35 – FlexRay Bus Driver 1 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6 (default on)	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8 (default on)	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J33 & J34 FlexRay 1 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

J36 – FlexRay Bus Driver 2 Enable

Controls which I/O pins on the MPC560xP processor are connected to the TxD and RxD pins on FlexRay Bus Driver. It is recommended to remove the J40 and J7 jumpers to prevent signal distortion.

Jumper Setting	Effect
1+2	The TXD pin on the FlexRay Bus Driver is connected to the “D[3]” pin on the MPC560xP processor.
3+4	The TXEN pin on the FlexRay Bus Driver is connected to the “D[4]” pin on the MPC560xP processor.
5+6	The RXD pin on the FlexRay Bus Driver is connected to the “D[2]” pin on the MPC560xP processor.

J39 – FlexRay Bus Driver 2 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V

3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J37 & J38 – FlexRay 2 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

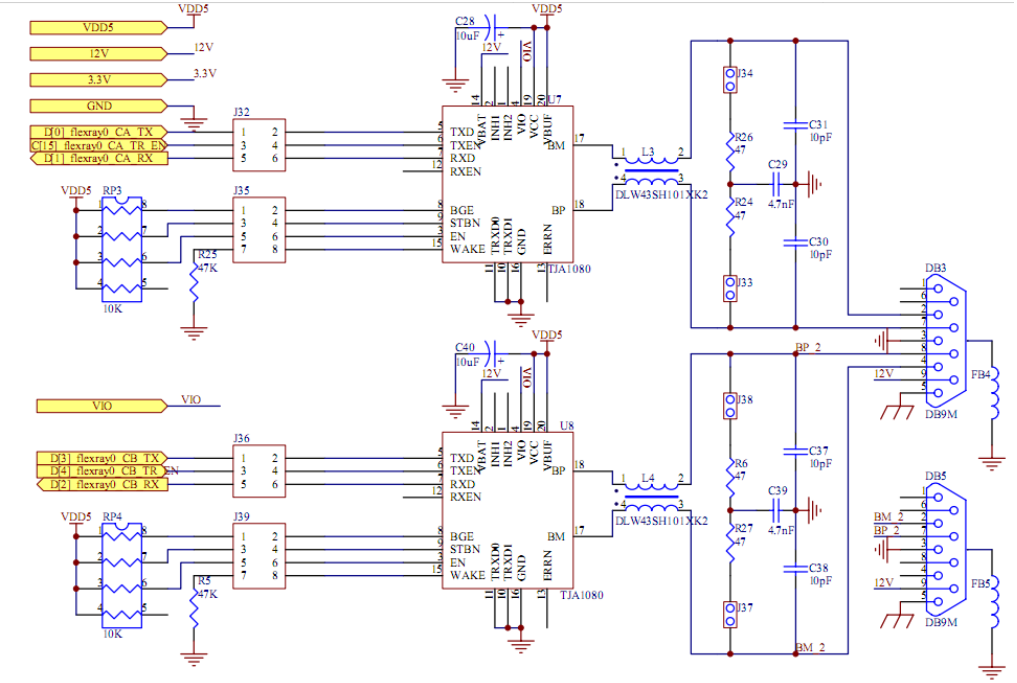


Figure 3-9: FlexRay schematic

3.8 Potentiometer

A potentiometer is available on the xPC56XXMB to allow an analog voltage input.

J40 – POT Enable

Jumper Setting	Effect
On (default)	The potentiometer wiper terminal is connected to the “E[0]” pin on the MPC560xP processor.
Off	The potentiometer wiper terminal is left disconnected.

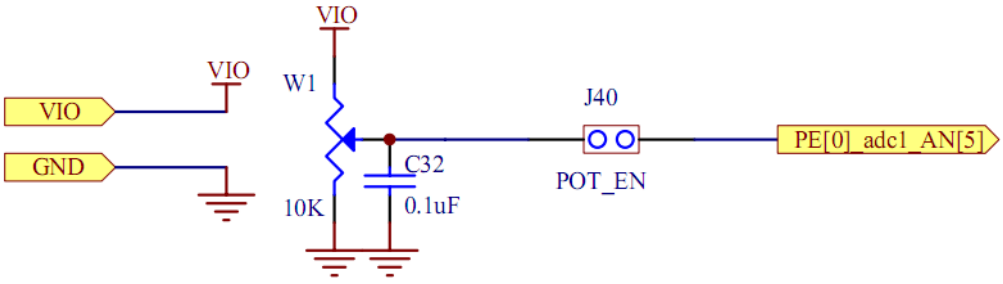
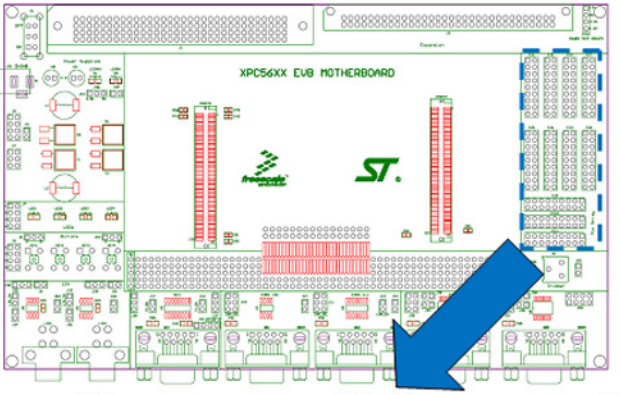


Figure 3-10: Potentiometer schematic

3.9 Pin Mapping

The following is the XKT560P EVB pin assignment for the Pin Array headers:



PJ1

RESET_B	RESET_B
B[1]	A[15]
B[0]	A[14]
C[7]	C[6]
C[5]	C[4]
C[3]	D[6]
B[3]	B[2]
F[15]	F[14]
GND	5V

PJ2

FAB - PA4	ABS0 - PA2
ABS2 - PA3	NMI
X	X
D[5]	X
X	X
D[1]	D[2]
D[0]	D[3]
C[15]	D[4]
GND	5V

PJ4 - Nexus

MCKO - F[7]	EVTO - F[10]
MSEO0 - F[9]	EVTI - F[11]
MSEO1 - F[8]	TDO - B[4]
MDO0	TDI - B[5]
MDO1 - F[6]	TCK
MDO2 - F[5]	TMS
MDO3 - F[4]	X
X	X
GND	5V

PJ7 - Port B

B[0]	B[1]
B[2]	B[3]
B[4]	B[5]
B[6]	B[7]
B[8]	B[9]
B[10]	B[11]
B[12]	B[13]
B[14]	B[15]
GND	5V

PJ5 - Port E

PE[0]	PE[1]
PE[2]	PE[3]
PE[4]	PE[5]
PE[6]	PE[7]
PE[8]	PE[9]
PE[10]	PE[11]
PE[12]	PE[13]
PE[14]	PE[15]
GND	5V

PJ6 - Port F

F[0]	F[1]
F[2]	F[3]
F[4]	F[5]
F[6]	F[7]
F[8]	F[9]
F[10]	F[11]
F[12]	F[13]
F[14]	F[15]
GND	5V

PJ3 - Port C

C[0]	C[1]
C[2]	C[3]
C[4]	C[5]
C[6]	C[7]
C[8]	C[9]
C[10]	C[11]
C[12]	C[13]
C[14]	C[15]
GND	5V

PJ8 - Port D

D[0]	D[1]
D[2]	D[3]
D[4]	D[5]
D[6]	D[7]
D[8]	D[9]
D[10]	D[11]
D[12]	D[13]
D[14]	D[15]
GND	5V

PJ9 - Port A

GND	A[14]	A[12]	A[10]	A[8]	A[6]	A[4]	A[2]	A[0]
5V	A[15]	A[13]	A[11]	A[9]	A[7]	A[5]	A[3]	A[1]

PJ10 - Port G

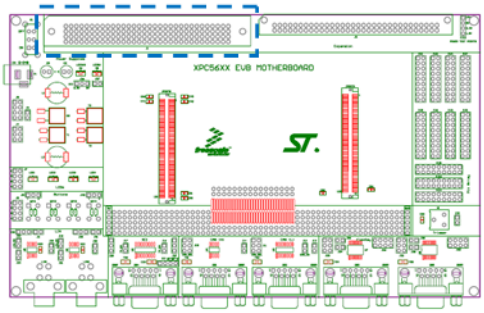
GND	X	X	G[10]	G[8]	G[6]	G[4]	G[2]	G[0]
5V	X	X	G[11]	G[9]	G[7]	G[5]	G[3]	G[1]

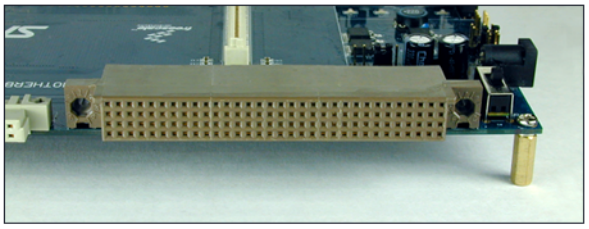
PJ11

GND	X	X	X	X	X	X	X	X
5V	X	X	X	X	X	X	X	X

Figure 3-11: Pin Mapping

3.10 Expansion Port Pin Mapping – DIN41612 (4x32)



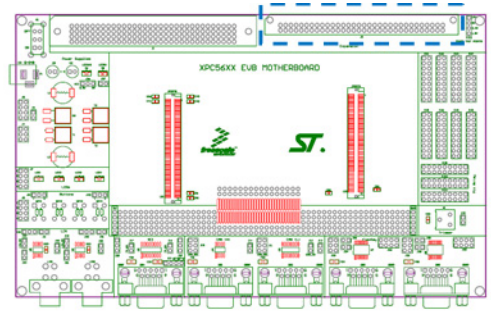


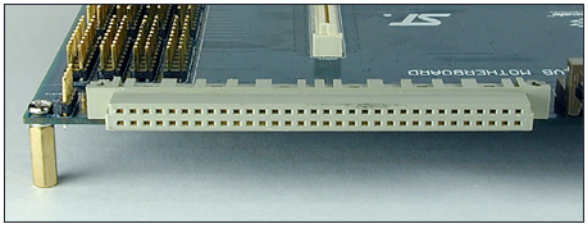
D32	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
C32	C31	C30	C29	C28	C27	C26	C25	C24	C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
B32	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
A32	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

A1	GND	B1	GND	C1	GND	D1	VDD5
A2	B[1] can0_RXD	B2	A[15] safetyport0_RXD	C2	B[0] can0_TXD	D2	A[14] safetyport0_TXD
A3	B[3] lin0_RXD	B3	B[2] lin0_TXD	C3	F[15] lin1_RXD	D3	F[14] lin1_TXD
A4	D[1] flexray0_CA_RX	B4	D[2] flexray0_CB_RX	C4	D[0] flexray0_CA_TX	D4	D[6] dspi0_CS2
A5	D[3] flexray0_CB_TX	B5	C[15] flexray0_CA_TR_EN	C5	D[4] flexray0_CB_TR_EN	D5	C[3] dspi0_CS1
A6	C[7] dspi0_SIN	B6	C[6] dspi0_SOUT	C6	C[5] dspi0_SCK	D6	C[4] dspi0_CS0
A7	D[5] dspi0_CS3	B7	J2 - NC3	C7	J2 - NC4	D7	J2 - NC5
A8	FAB - PA4	B8	ABS0 - PA2	C8	GND	D8	12V
A9	RESET	B9	RSTOUT	C9	J7 - N/C1	D9	J7 - N/C2
A10	ABS2 - PA3	B10	NMI	C10	J11 - N/C12	D10	J11 - N/C13
A11	J2 - NC1	B11	J2 - NC2	C11	J11 - N/C14	D11	J11 - N/C15
A12	C[0] adc1_AN[3]	B12	C[1] adc0_AN[2]	C12	C[8] dspi1_CS1	D12	C[9] dspi2_CS3
A13	C[2] adc0_AN[3]	B13	C[3] dspi0_CS1	C13	C[10] dspi2_CS2	D13	C[11] etimer0_ETC[4]
A14	C[4] dspi0_CS0	B14	C[5] dspi0_SCK	C14	C[12] etimer0_ETC[5]	D14	C[13] etimer1_ETC[1]
A15	C[6] dspi0_SOUT	B15	EPUTA0_L4	C15	C[14] etimer1_ETC[2]	D15	C[15] flexray0_CA_TR_EN
A16	A[0] etimer0_ETC[0]	B16	A[1] etimer0_ETC[1]	C16	G[0] fcu0_F[0]	D16	G[1] fcu0_F[1]
A17	A[2] etimer0_ETC[2]	B17	A[3] etimer0_ETC[3]	C17	G[2] flexpwm0_X[2]	D17	G[3] flexpwm0_A[2]
A18	A[4] etimer1_ETC[0]	B18	A[5] dspi1_CS0	C18	G[4] flexpwm0_B[2]	D18	G[5] flexpwm0_X[3]
A19	A[6] dspi1_SCK	B19	A[7] dspi1_SOUT	C19	G[6] flexpwm0_A[3]	D19	G[7] flexpwm0_B[3]
A20	A[8] dspi1_SIN	B20	A[9] dspi2_CS1	C20	G[8] flexpwm0_FAULT[0]	D20	G[9] flexpwm0_FAULT[1]
A21	A[10] dspi2_CS0	B21	A[11] dspi2_SCK	C21	G[10] flexpwm0_FAULT[2]	D21	G[11] flexpwm0_FAULT[3]
A22	A[12] dspi2_SOUT	B22	A[13] dspi2_SIN	C22	J10 - N/C1	D22	J10 - N/C2
A23	A[14] safetyport0_TXD	B23	A[15] safetyport0_RXD	C23	J10 - N/C3	D23	J10 - N/C4
A24	C[0] adc1_AN[3]	B24	C[1] adc0_AN[2]	C24	D[0] flexray0_CA_TX	D24	D[1] flexray0_CA_RX
A25	C[2] adc0_AN[3]	B25	C[3] dspi0_CS1	C25	D[2] flexray0_CB_RX	D25	D[3] flexray0_CB_TX
A26	0 AN4COM_PE1	B26	0 AN5COM_PE2	C26	D[4] flexray0_CB_TR_EN	D26	D[5] dspi0_CS3
A27	0 AN6COM_PE3	B27	1 AN0COM_PB13	C27	D[6] dspi0_CS2	D27	D[7] dspi1_CS3
A28	1 AN1COM_PB14	B28	1 AN2COM_PB15	C28	D[8] dspi1_CS2	D28	D[9] flexpwm0_X[0]
A29	1 AN3COM_PC0	B29	1 AN4COM_PD15	C29	D[10] flexpwm0_A[0]	D29	D[11] flexpwm0_B[0]
A30	1 AN5COM_PE0	B30	1 AN6COM_PE8	C30	D[12] flexpwm0_X[1]	D30	D[13] flexpwm0_A[1]
A31	1/0 AN11COM_PB9	B31	1/0 AN12COM_PB10	C31	D[14] flexpwm0_B[1]	D31	D[15] adc1_AN[4]
A32	GND	B32	3.3V	C32	GND	D32	VDD5

Figure 3-12: Expansion Port Pin Mapping – DIN41612 (4x32)

3.11 Expansion Port Pin Mapping – DIN41612 (2x32)





B32 A32	B31 A31	B30 A30	B29 A29	B28 A28	B27 A27	B26 A26	B25 A25	B24 A24	B23 A23	B22 A22	B21 A21	B20 A20	B19 A19	B18 A18	B17 A17	B16 A16	B15 A15	B14 A14	B13 A13	B12 A12	B11 A11	B10 A10	B9 A9	B8 A8	B7 A7	B6 A6	B5 A5	B4 A4	B3 A3	B2 A2	B1 A1

A1	GND	B1	VDD5
A2	B[0] can0_TXD	B2	B[1] can0_RXD
A3	B[2] lin0_TXD	B3	B[3] lin0_RXD
A4	B[4] jtag0_TDO/TDOC	B4	B[5] jtag0_TDI/TDIC
A5	B[6] mc_cgl_CLKOUT	B5	B[7] adc0_AN[0]
A6	B[8] adc0_AN[1]	B6	B[9] adc0_adc1_AN[11]
A7	B[10] adc0_adc1_AN[12]	B7	B[11] adc0_adc1_AN[13]
A8	B[12] adc0_adc1_AN[14]	B8	B[13] adc1_AN[0]
A9	B[14] adc1_AN[1]	B9	B[15] adc1_AN[2]
A10	PE[0] adc1_AN[5]	B10	PE[1] adc0_AN[4]
A11	PE[2] adc0_AN[5]	B11	PE[3] adc0_AN[6]
A12	PE[4] adc0_AN[7]	B12	PE[5] adc0_AN[8]
A13	PE[6] adc0_AN[9]	B13	PE[7] adc0_AN[10]
A14	PE[8] adc1_AN[6]	B14	PE[9] adc1_AN[7]
A15	PE[10] adc1_AN[8]	B15	PE[11] adc1_AN[9]
A16	PE[12] adc1_AN[10]	B16	PE[13] dspi3_SCK
A17	PE[14] dspi3_SOUT	B17	PE[15] dspi3_SIN
A18	F[0] flexray0_DBG0	B18	F[1] flexray0_DBG1
A19	F[2] flexray0_DBG2	B19	F[3] flexray0_DBG3
A20	F[4] nexus0_MDO[3]	B20	F[5] nexus0_MDO[2]
A21	F[6] nexus0_MDO[1]	B21	F[7] nexus0_MCKO
A22	F[8] nexus0_MSEO1	B22	F[9] nexus0_MSEO0
A23	F[10] nexus0_EVTO	B23	F[11] nexus0_EVTI
A24	F[12] etimer1_ETC[3]	B24	F[13] etimer1_ETC[4]
A25	F[14] lin1_TXD	B25	F[15] lin1_RXD
A26	J11 - N/C0	B26	J11 - N/C1
A27	J11 - N/C2	B27	J11 - N/C3
A28	J11 - N/C4	B28	J11 - N/C5
A29	J11 - N/C6	B29	J11 - N/C7
A30	J11 - N/C8	B30	J11 - N/C9
A31	J11 - N/C10	B31	J11 - N/C11
A32	GND	B32	3.3V

Figure 3-13: Expansion Port Pin Mapping – DIN41612 (2x32)

4 XDC560P100S HARDWARE & JUMPER SETTINGS

4.1 Boot Configuration

The following jumpers affect the operation of the processor as it initially comes out of the reset state:

J7 – FAB Configuration

Controls whether the processor boots from internal FLASH or from a serial interface (CAN, SCI)

Jumper Setting	Effect
1+2	The MPC560xP processor uses serial boot mode
2+3 (default)	The MPC560xP processor uses internal boot mode

J8 – ABS0 Configuration

This jumper configures the ABS[0] pin.

Jumper Setting	Effect
1+2	The ABS[0] pin is pulled up logic high
2+3 (default)	The ABS[2] pin is pulled down logic low

J9 – ABS2 Configuration

This jumper configures the ABS[2] pin.

Jumper Setting	Effect
1+2	The ABS[2] pin is pulled up logic high
2+3 (default)	The ABS[2] pin is pulled down logic low

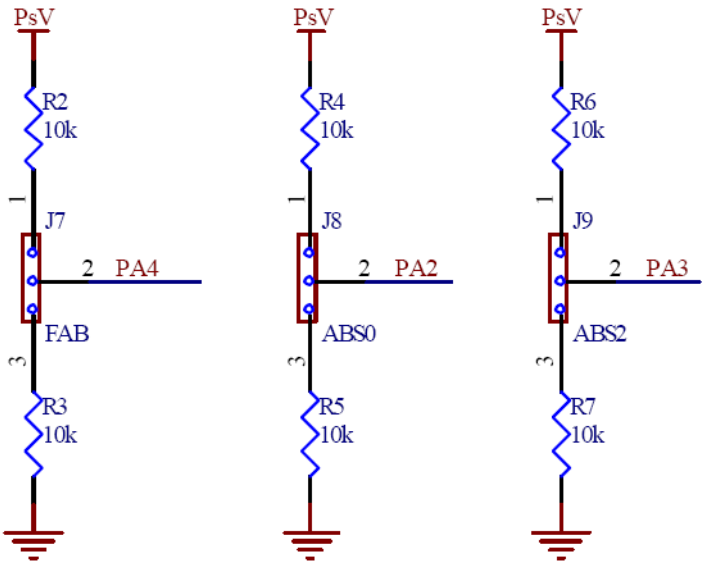


Figure 4-1: Boot Configuration Jumpers

4.2 Power Configuration

When the XDC560P Mini-Module is plugged into the xPC56XXMB motherboard, power is supplied directly by the motherboard. In this setup, the external power supply input available on the Mini-Module should NOT be used.

When the XDC560P Mini-Module is used as a stand-alone board, an external

5V or 3.3V power supply must be used.

The following jumpers affect the power supply pins of the MPC560xP processor:

J3 – Power Supply Voltage Selection

Controls whether the processor is powered using 5V or 3.3V. This selection can only be made if the XDC560P Mini-Module is plugged into the xPC56XXMB motherboard. If the XDC560P Mini-Module is used as a stand-alone board, the processor is powered directly by the external power supply and this jumper setting has no effect.

Jumper Setting	Effect
1+2 (default)	MPC560xP processor is powered by the 5V supply
2+3	MPC560xP processor is powered by the 3.3V supply

J4 – ADC Analog Supply Voltage Enable

Controls whether the reference voltage and analog supply pins for the A/D converter (VDD-REF ADC0, VDD-REF ADC1) is powered by 5V or 3.3V

Jumper Setting	Effect
1+2 (default)	MPC560xP ADC supply pins are connected to 5V
2+3	MPC560xP ADC supply pins are connected to 3.3V

J14 – Power Supply Pins Enable

Controls whether power is provided to the “Power Supply” pins (VDD_HV) on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP Power Supply pins are connected to 5V or 3.3V (determined by J3)
Off	MPC560xP Power Supply pins are unpowered

J15 – 1.2V Core Voltage Enable

Controls whether power is provided to the “VDD 1V2” pins on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD 1V2” pins are connected to 1.2V power
Off	MPC560xP “VDD 1V2” pins are left disconnected

J17 – Debug Port Voltage Configuration

Sets the logic voltage level on the 14-pin JTAG port and 38-pin MICTOR port (if available). These ports are used by external interface hardware to communicate with the processor.

Jumper Setting	Effect
1+2 (default)	Debug port(s) are configured for 5V logic

2+3	Debug port(s) are configured for 3.3V logic

J19 – VREG Voltage Enable

Controls whether power is provided to the “VDD VREG” pins on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD VREG” pins are connected to 3.3V or 5V (determined by J3)
Off	MPC560xP “VDD VREG” pins are left disconnected

J20 – FLA0FLA1 Voltage Enable

Controls whether power is provided to the “VDD” pin 69 on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD” pin 69 is connected to 3.3V or 5V (determined by J3)
Off	MPC560xP “VDD” pin 69 is left disconnected

CT6 – 1.2V Power Generation

Controls whether the 1.2 power supply is generated from the NPN transistor

or supplied directly from the xPC56XXMB motherboard.

Jumper Setting	Effect
Connected	1.2V power is provided directly by the xPC56XXMB motherboard
Disconnected (default)	1.2V power is generated by the NPN transistor circuit on the XDC560P Mini-Module

4.3 System Clock Configuration

The XDC560P Mini-Modules support the usage of crystal clock sources as well as external clock sources.

J10 – Crystal clock source enable

Both of the jumpers below need to be installed to enable the crystal clock source.

Jumper Setting	Effect
1+2 (default)	The MPC560xP “XTAL” signal is connected to the crystal clock source on the XDC560P Mini-Module
3+4 (default)	The MPC560xP “EXTAL” signal is connected to the crystal clock source on the XDC560P Mini-Module

J11 – External clock source enable

The XDC560P Mini-Module contains a footprint for an SMA connector, which

can be used to provide an external clock source to the system.

Jumper Setting	Effect
On	The MPC560xP “EXTAL” signal is connected to the SMA connector on the XDC560P Mini-Module
Off (default)	The SMA connector on the XDC560P Mini-Module is disconnected from the processor

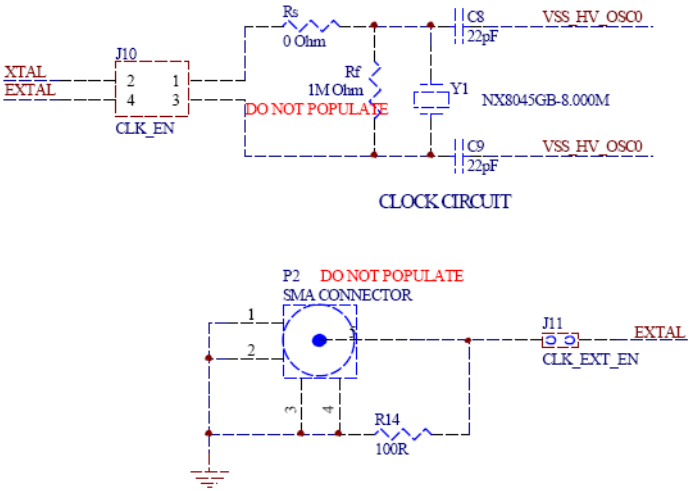


Figure 4-2: System Clock Schematic

4.4 General Configuration

J13 – Reset Enable

A RESET push button on the XDC560P Mini-Module can be used to reset the

processor.

Jumper Setting	Effect
On (default)	The RESET button on the XDC560P Mini-Module is enabled
Off	The RESET button on the XDC560P Mini-Module is disabled

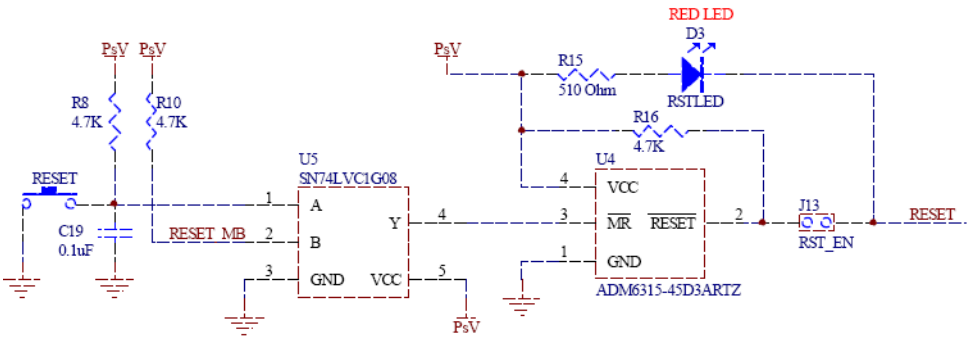


Figure 4-3: Reset circuitry schematic

5 XDC560P144S HARDWARE & JUMPER SETTINGS

5.1 Boot Configuration

The following jumpers affect the operation of the processor as it initially comes out of the reset state:

J7 – FAB Configuration

Controls whether the processor boots from internal FLASH or from a serial interface (CAN, SCI)

Jumper Setting	Effect
1+2	The MPC560xP processor uses serial boot mode
2+3 (default)	The MPC560xP processor uses internal boot mode

J8 – ABS0 Configuration

This jumper configures the ABS[0] pin.

Jumper Setting	Effect
1+2	The ABS[0] pin is pulled up logic high
2+3 (default)	The ABS[2] pin is pulled down logic low

J9 – ABS2 Configuration

This jumper configures the ABS[2] pin.

Jumper Setting	Effect
1+2	The ABS[2] pin is pulled up logic high
2+3 (default)	The ABS[2] pin is pulled down logic low

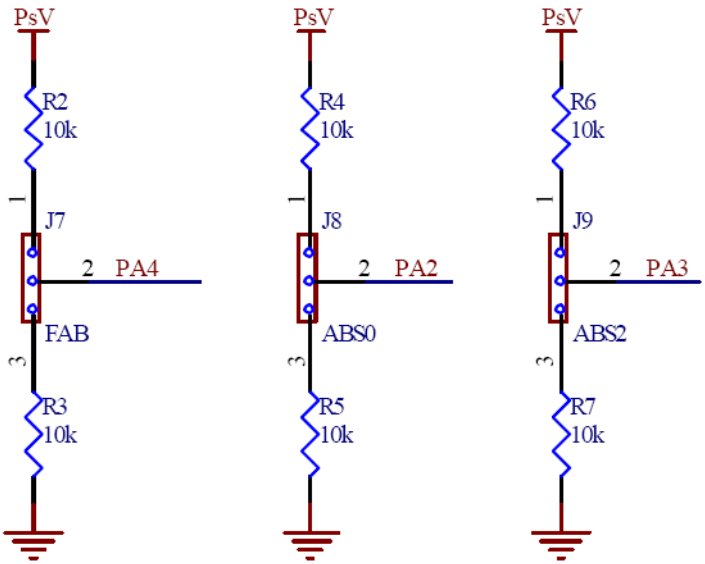


Figure 5-1: Boot Configuration Jumpers

5.2 Power Configuration

When the XDC560P Mini-Module is plugged into the xPC56XXMB motherboard, power is supplied directly by the motherboard. In this setup, the external power supply input available on the Mini-Module should NOT be used.

When the XDC560P Mini-Module is used as a stand-alone board, an external

5V or 3.3V power supply must be used.

The following jumpers affect the power supply pins of the MPC560xP processor:

J3 – Power Supply Voltage Selection

Controls whether the processor is powered using 5V or 3.3V. This selection can only be made if the XDC560P Mini-Module is plugged into the xPC56XXMB motherboard. If the XDC560P Mini-Module is used as a stand-alone board, the processor is powered directly by the external power supply and this jumper setting has no effect.

Jumper Setting	Effect
1+2 (default)	MPC560xP processor is powered by the 5V supply
2+3	MPC560xP processor is powered by the 3.3V supply

J4 – ADC Analog Supply Voltage Enable

Controls whether the reference voltage and analog supply pins for the A/D converter (VDD-REF ADC0, VDD-REF ADC1) is powered by 5V or 3.3V

Jumper Setting	Effect
1+2 (default)	MPC560xP ADC supply pins are connected to 5V
2+3	MPC560xP ADC supply pins are connected to 3.3V

J14 – Power Supply Pins Enable

Controls whether power is provided to the “Power Supply” pins (VDD_HV) on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP Power Supply pins are connected to 5V or 3.3V (determined by J3)
Off	MPC560xP Power Supply pins are unpowered

J15 – 1.2V Core Voltage Enable

Controls whether power is provided to the “VDD 1V2” pins on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD 1V2” pins are connected to 1.2V power
Off	MPC560xP “VDD 1V2” pins are left disconnected

J17 – Debug Port Voltage Configuration

Sets the logic voltage level on the 14-pin JTAG port and 38-pin MICTOR port (if available). These ports are used by external interface hardware to communicate with the processor.

Jumper Setting	Effect
1+2 (default)	Debug port(s) are configured for 5V logic

2+3	Debug port(s) are configured for 3.3V logic

J19 – VREG Voltage Enable

Controls whether power is provided to the “VDD VREG” pins on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD VREG” pins are connected to 3.3V or 5V (determined by J3)
Off	MPC560xP “VDD VREG” pins are left disconnected

J20 – FLA0FLA1 Voltage Enable

Controls whether power is provided to the “VDD” pin 69 on the MPC560xP processor.

Jumper Setting	Effect
On (default)	MPC560xP “VDD” pin 97 is connected to 3.3V or 5V (determined by J3)
Off	MPC560xP “VDD” pin 97 is left disconnected

CT6 – 1.2V Power Generation

Controls whether the 1.2 power supply is generated from the NPN transistor

or supplied directly from the xPC56XXMB motherboard.

Jumper Setting	Effect
Connected	1.2V power is provided directly by the xPC56XXMB motherboard
Disconnected (default)	1.2V power is generated by the NPN transistor circuit on the XDC560P Mini-Module

CT8 – Mictor VEN_IO2 Configuration

Controls whether the VEN_IO2 pin on the 38-pin Mictor port is connected to the PA4 pin on the MPC560xP processor.

Jumper Setting	Effect
Connected	The VEN_IO2 pin is connected to PA4
Disconnected (default)	The VEN_IO2 pin is left disconnected

5.3 System Clock Configuration

The XDC560P Mini-Modules support the usage of crystal clock sources as well as external clock sources.

J10 – Crystal clock source enable

Both of the jumpers below need to be installed to enable the crystal clock source.

Jumper Setting	Effect

1+2 (default)	The MPC560xP “XTAL” signal is connected to the crystal clock source on the XDC560P Mini-Module
3+4 (default)	The MPC560xP “EXTAL” signal is connected to the crystal clock source on the XDC560P Mini-Module

J11 – External clock source enable

The XDC560P Mini-Module contains a footprint for an SMA connector, which can be used to provide an external clock source to the system.

Jumper Setting	Effect
On	The MPC560xP “EXTAL” signal is connected to the SMA connector on the XDC560P Mini-Module
Off (default)	The SMA connector on the XDC560P Mini-Module is disconnected from the processor

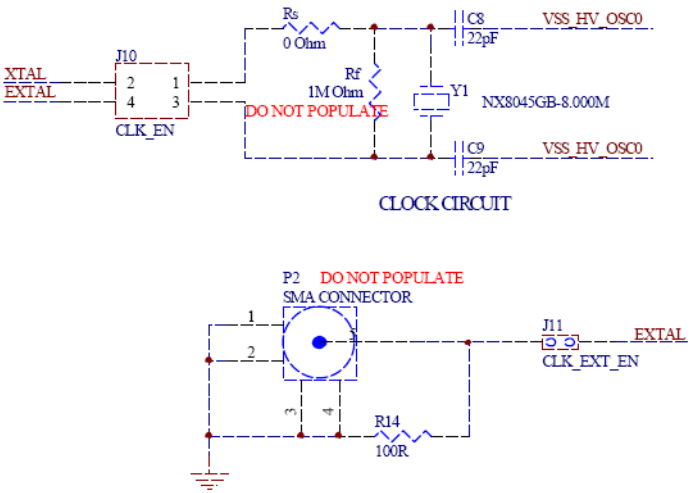


Figure 5-2: System Clock schematic

5.4 General Configuration

J13 – Reset Enable

A RESET push button on the XDC560P Mini-Module can be used to reset the processor.

Jumper Setting	Effect
On (default)	The RESET button on the XDC560P Mini-Module is enabled
Off	The RESET button on the XDC560P Mini-Module is disabled

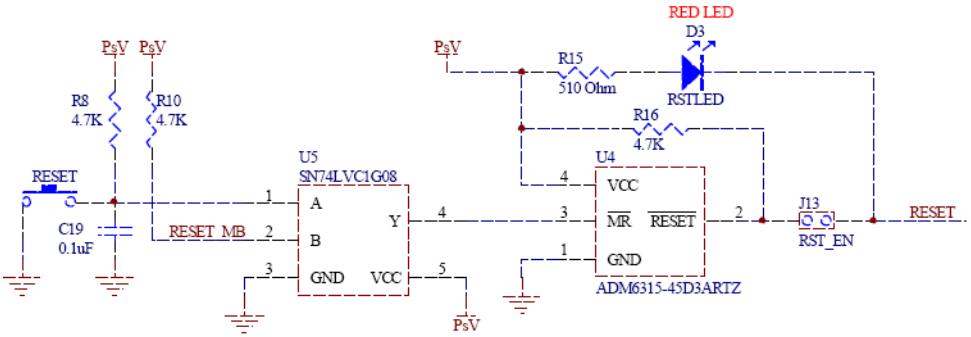


Figure 5-3: Reset circuitry schematic

6 DEBUGGING/PROGRAMMING XKT560P EVB

P&E provides hardware and software tools for debugging and programming the XKT560P EVB system.

P&E's MULTILINK UNIVERSAL and USB QORIVVA MULTILINK are development tools that will enable you to debug your code and program it onto your target. The Cyclone MAX is a more versatile and robust development tool with advanced features and production programming capabilities, as well as Ethernet support.

More information is available below to assist you in choosing the appropriate development tool for your needs.

6.1 Hardware Solutions At A Glance

The MULTILINK UNIVERSAL and USB QORIVVA MULTILINK offer an affordable and compact solution for your development needs, and allows debugging and programming to be accomplished simply and efficiently. Those doing rapid development will find the MULTILINK UNIVERSAL and USB QORIVVA MULTILINK easy to use and fully capable of fast-paced debugging and programming.

The Cyclone MAX is a more complete solution designed for both development and production. The Cyclone MAX features multiple communications interfaces (including USB, Ethernet, and Serial), stand-alone programming functionality, high speed data transfer, a status LCD, and many other advanced capabilities.

Below is an overview of the features and intended use of these Qorivva-compatible hardware interfaces.

6.2 MULTILINK UNIVERSAL and USB QORIVVA MULTILINK Key Features

- Programming and debugging capabilities
- Compact and lightweight
- Communication via USB 2.0
- Supported by P&E software and Freescale's CodeWarrior
- USB QORIVVA MULTILINK supports Freescale Qorivva MPC55xx/56xx. MULTILINK UNIVERSAL supports Freescale HCS08, HC(S)12(X), RS08, ColdFire V1/+V1, ColdFire V2-4, Qorivva

MPC55xx/56xx, and Kinetis ARM.

6.3 Cyclone MAX Key Features

- Advanced programming and debugging capabilities, including:
- PC-Controlled and User-Controlled Stand-Alone Operation
- Interactive Programming via Host PC
- In-Circuit Debugging, Programming, and Testing
- Compatible with Freescale's ColdFireV2/3/4, Power 5xx/8xx, Qorivva MPC55xx/56xx, and ARM7 microcontroller families
- Communication via USB, Serial, and Ethernet Ports
- Multiple image storage
- LCD screen menu interface
- Supported by P&E software and Freescale's CodeWarrior

6.4 Working With P&E's MULTILINK UNIVERSAL or USB QORIVVA MULTILINK

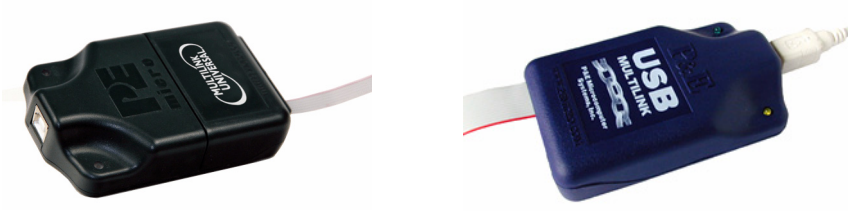


Figure 6-1: MULTILINK UNIVERSAL (left) & USB QORIVVA MULTILINK (right)

6.4.1 Product Features & Implementation

Both P&E's MULTILINK UNIVERSAL and USB QORIVVA MULTILINK connect your target to your PC and allows the PC access to the debug mode. The USB QORIVVA MULTILINK supports Freescale Qorivva MPC55xx/56xx devices, while the MULTILINK UNIVERSAL supports Freescale HCS08, HC(S)12(X), RS08, ColdFire V1/+V1, ColdFire V2-4, Qorivva 55xx/56xx, and Kinetis ARM. For working with Qorivva devices, each connects between a USB port on a Windows 2000/XP/2003/Vista/7 machine and a standard 14-pin JTAG/Nexus connector on the target.

By using one of these interfaces, the user can take advantage of the background debug mode to halt normal processor execution and use a PC to control the processor. The user can then directly control the target's execution, read/write registers and memory values, debug code on the processor, and program internal or external FLASH memory devices. In tandem with the appropriate software, these interfaces enable you to debug, program, and test your code on your board.

6.4.2 Software

The MULTILINK UNIVERSAL and USB QORIVVA MULTILINK interfaces work with Codewarrior as well as P&E's in-circuit debugger and flash programmer to allow debug and flash programming of the target processor. P&E's USB QORIVVA MULTILINK Development Packages include the USB QORIVVA MULTILINK in addition to flash programming software, in-circuit debugging software, a Windows IDE, and register file editor.

6.5 Working With P&E's Cyclone MAX

P&E's Cyclone MAX

6.5.1 Product Features & Implementation

P&E's Cyclone MAX is an extremely flexible tool designed for debugging, testing, and in-circuit flash programming of Freescale's ColdFireV2/3/4, Power 5xx/8xx, Qorivva MPC55xx/56xx, and ARM7 microcontrollers. The Cyclone MAX connects your target to the PC via USB, Ethernet, or Serial Port and enables you to debug your code, program, and test it on your board. After development is complete the Cyclone MAX can be used as a production tool on your manufacturing floor.

For production, the Cyclone MAX may be operated interactively via Windows-based programming applications as well as under batch or .dll commands

from a PC. Once loaded with data by a PC it can be disconnected and operated manually in a stand-alone mode via the LCD menu and control buttons. The Cyclone MAX has over 3Mbytes of non-volatile memory, which allows the on-board storage of multiple programming images. When connected to a PC for programming or loading it can communicate via the ethernet, USB, or serial interfaces.

6.5.2 Software

The Cyclone MAX comes with intuitive configuration software and interactive programming software, as well as easy to use automated control software. The Cyclone MAX also functions as a full-featured debug interface, and is supported by Freescale's CodeWarrior as well as development software from P&E.

P&E's Cyclone MAX is also available bundled with additional software as part of various Development Packages. In addition to the Cyclone MAX, these Development Packages include in-circuit debugging software, flash programming software, a Windows IDE, and register file editor.

Freescale Controller Continuum

68HC08/S08/RS08/(S)12(X) ColdFire® V1/+V1 ColdFire® V2/V3/V4 Qorivva® ARM®

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