User's Manual

EM08JBJGUM/D
Version 2.0
June 3, 2002

MOTOROLA
intelligence everywhere™

digital dna™

M68EM08JBJG

Emulation Module

User's Manual

Important Notice to Users

While every effort has been made to ensure the accuracy of all information in this document, Motorola assumes no liability to any party for any loss or damage caused by errors or omissions or by statements of any kind in this document, its updates, supplements, or special editions, whether such errors are omissions or statements resulting from negligence, accident, or any other cause. Motorola further assumes no liability arising out of the application or use of any information, product, or system described herein: nor any liability for incidental or consequential damages arising from the use of this document. Motorola disclaims all warranties regarding the information contained herein, whether expressed, implied, or statutory, *including implied warranties of merchantability or fitness for a particular purpose*. Motorola makes no representation that the interconnection of products in the manner described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting or license to make, use or sell equipment constructed in accordance with this description.

Trademarks

This document includes these trademarks:

Motorola and the Motorola logo are registered trademarks of Motorola, Inc.

Windows is a registered trademark of Microsoft Corporation in the U.S. and other countries.

Intel is a registered trademark of Intel Corporation.

Motorola, Inc., is an Equal Opportunity / Affirmative Action Employer.

For an electronic copy of this book, visit Motorola's web site at http://e-www.motorola.com/

Table of Contents

Table of Contents

List of Figures

List of Figures

List of Tables

List of Tables

M68EM08JBJG Quick Start Guide

CAUTION: *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

Follow these quick-start steps to configure the M68EM08JBJG emulator module (JBJGEM) and install it in a Motorola Modular Development System (MMDS) or Motorola Modular Evaluation System (MMEVS). For other parts of system installation, see the MMDS or MMEVS hardware manuals.

1. Set the Configuration Headers to their Factory Defaults

CAUTION: *Before you change configuration header settings, remove power.*

To set the JBJGEM configuration headers to their factory defaults (MC68HC908JB16 and MC68HC908JG16 emulation), make sure that:

- A jumper is installed on pins 5 and 6 of configuration header W1
- A jumper is installed on pins 1 and 2 of configuration header W2
- A jumper is installed on pins 1 and 2 of configuration header W3
- A jumper is installed on pins 2 and 3 of configuration header W4
- A jumper is installed on pins 2 and 3 of configuration header W5
- A jumper is installed on pins 3 and 4 of configuration header W6
- A jumper is installed on pins 3 and 4 of configuration header W7
- A jumper is installed on pins 3 and 4 of configuration header W8

2. Install the JBJGEM

Once you have ensured that the configuration headers are set to their factory defaults, you can install the JBJGEM in the MMDS or MMEVS.

CAUTION: *Before you attempt an installation, disconnect any system cable connections and remove power.*

Option 1 - To Install the JBJGEM in an MMDS Station Module

To install the JBJGEM in an MMDS station module:

1. Remove the entire top half of the station-module enclosure.
2. Fit together JBJGEM connectors J4 and J5 (on the bottom of the board) and control-board connectors P11 and P12.
3. Snap the corners of the JBJGEM onto the plastic standoffs.

Option 2 - To Install the JBJGEM in an MMEVS Station Module

To install the JBJGEM in an MMEVS station module:

1. Fit together JBJGEM connectors J4 and J5 (on the bottom of the board) and platform-board connectors P6 and P7.
2. Snap the corners of the EM onto the plastic standoffs.

3. Copy the Personality Files

To complete the installation, you must copy the personality files from the provided diskette to the directory that contains the debugging software. The personality files for the JBJGEM are:

- 00455Vxx.MEM — P&E Personality file for MC68HC908JB16 and MC68HC908JG16 MCU
- 00C55Vxx.MEM — MCUez Personality file for MC68HC908JB16 and MC68HC908JG16 MCU

At this point, the installation is complete. Remake any system cable connections and restore power. For additional instructions, consult the MMDS or MMEVS operations manuals.

Section 1. General Information

1.1 Introduction

This user’s manual explains connection, configuration, and operational information specific to the M68EM08JBJG emulator module (JBJGEM). The JBJGEM lets you emulate and debug target systems based on the MC68HC908JB16 and MC68HC908JG16 microcontroller units (MCU).

This section describes Motorola’s two development systems that use the JBJGEM, and it explains the JBJGEM’s layout.

1.2 Development Systems

The JBJGEM can be part of two Motorola development systems:

- MMDS0508 Motorola Modular Development System (MMDS)
- MMEVS0508 Motorola Modular Evaluation System (MMEVS)

1.2.1 Motorola Modular Development System

The Motorola Modular Development System (MMDS) is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debug.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs, in this case, the JBJGEM

- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.
- 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — CodeWarrior™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; a CodeWarrior software manual, included with the CodeWarrior software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMDS0508 software package; and this EM user's manual (this manual)

MMDS baud rates are selected by the user at 2400, 4800, 9600, 19200, 38400, or 57600.

The JBJGEM gives the MMDS the ability to emulate target systems based on MC68HC908JB16 and MC68HC908JG16 MCUs. By substituting a different EM, MMDS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.2.2 Motorola Modular Evaluation System (MMEVS)

A Motorola Modular Evaluation System (MMEVS) is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module and has connectors for power and for a terminal or host computer

- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs and fits onto the PFB, in this case, the JBJGEM
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — CodeWarrior™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D; the CodeWarrior software manual, included with the CodeWarrior software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMEVS0508 software package; and this emulator user's manual

An MMEVS features automatic selection of the communication baud rate from these choices: 2400, 4800, 9600, 19200, 38400, or 57600.

With a JBJGEM, the MMEVS emulates target systems based on MC68HC908JB16 and MC68HC908JG16 MCUs. By substituting a different EM, the MMEVS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.3 JBJGEM Layout

Figure 1-1 shows the layout of the JBJGEM.

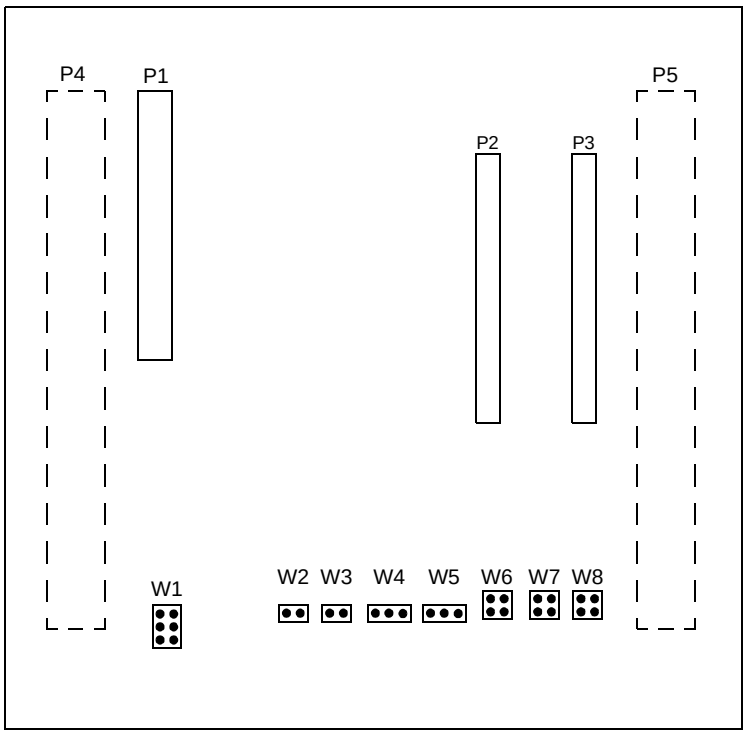


Figure 1-1M68EM08JBJG Emulator Module

The main elements of the JBJGEM are:

- DIN connectors P4 and P5 — Connect the EM to the MMDS control board or the MMEVS platform board
- Connector P1 — Permits connection to a logic analyzer
- Connectors P2 and P3 — Customer-specific interfaces to the target system
- Jumper header W1 — Selects MCU clock source
- Jumper header W2 and W3 — Together select Phase Lock Loop (PLL) filters
- Jumper header W4 and W5 — Together select 3.3V regulator supply capacitors source for analog module
- Jumper header W6, W7 and W8 — Together select power supply source for analog module

The JBJGEM requires a user-supplied 80-lead target cable and target head adapter to connect the target system to connectors P2 and P3.

1.4 JBJGEM Specifications

Table 1-1 lists JBJGEM specifications.

Table 1-1M68EM08JBJG Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to 40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 V dc and +12 V dc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	4.88 X 4.7 inches; 123.7 X 119.25 mm

Section 2. Configuration and Operation

2.1 Introduction

This section explains configuration and operation of the JBJGEM when it is installed in an MMDS or MMEVS. For additional information on system installation or configuration, see the MMDS or MMEVS hardware manuals.

A JBJGEM that is already installed in an MMDS station module can be reconfigured. To do so, you must first switch off station-module power, then follow the guidance in this section. Similarly, a JBJGEM that is already installed on the MMEVS platform board can be reconfigured, provided that platform-board power is disconnected.

CAUTION: *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

2.2 Setting Configuration Jumper Headers

CAUTION: *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring jumper headers with the power on can damage system circuits.*

The JBJGEM has eight configuration jumper headers. **Table 2-1** contains a summary of settings for these headers.

Table 2-1Configuration Jumper Headers

Jumper Header	Type	Description

Table 2-1Configuration Jumper Headers

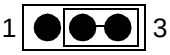
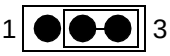
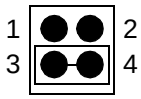
Clock Source Header W1	W1  	Jumper between pins 1 and 2; selects an external clock source for the OSC1 input signal from target head connectors Jumper between pins 3 and 4; selects the clock signal from the MMDS control board or MMEVS platform board Jumper between pins 5 and 6 (factory default); selects the onboard 12MHz oscillator
PLL Filter Headers W2, W3	W2 CGMXFC2  W3 CGMXFC1  	Jumper on (factory default); connects on-board PLL filter to CGMXFC1/2 pin Jumper off; disconnects on-board PLL loop filter to CGMXFC1/2 pin Note: Remove jumpers on W2 and W3 if using external PLL loop filters
On-Chip Voltage Regulator Header W4	W4 VREGA1  	Jumper between pins 1 and 2; selects external supply for VREGA1 input Jumper between pins 2 and 3 (factory default); selects on-chip regulator VREGA0 as VREGA1 input
On-Chip Voltage Regulator Header W5	W5 VREGA0  	Jumper between pins 1 and 2; selects external regulator supply capacitors for on-chip 3.3V regulator (VREGA0) output Jumper between pins 2 and 3 (factory default); selects on-board regulator supply capacitors for on-chip 3.3V regulator (VREGA0) output
Analog Module Voltage Header W7	W7 VDDA  	Jumper between pins 1 and 2; selects analog voltage source from the target system, VDDA, as input for the analog module of M68EM08JBJG Jumper between pins 3 and 4 (factory default); selects on-board, isolated analog voltage source, VDD, as input for the analog module of M68EM08JBJG

Table 2-1Configuration Jumper Headers

Analog Module Voltage Headers W6, W8	W6 VSSA1 1 2 3 4 W8 VSSA0 1 2 3 4	Jumper between pins 1 and 2; selects analog ground source from the target system, VSSA, as input for the analog module of M68EM08JBJG Jumper between pins 3 and 4 (factory default); selects on-board ground, GND, as input for the analog module of M68EM08JBJG

2.2.1 Clock Source Header (W1)

Use jumper header W1 in **Figure 2-1** to determine the clock signal source. The factory configuration (with fabricated jumper between pins 5 and 6) selects the clock signal from the on-board 12Mhz oscillator.

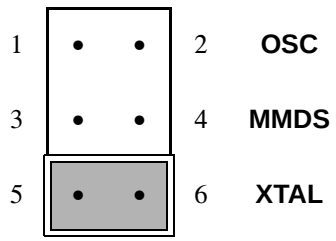


Figure 2-1Clock Source Header W1

Alternatively, two other clock signal sources can be selected, as shown in **Figure 2-1**

- To select the target system as the clock source, install the fabricated jumper between pins 1 and 2. Ensure that the clock source (OSC1) is connected to the EM through the target cable, connector P3 pin 1.
- To select the clock signal from the MMDS control board or MMEVS platform board, install the fabricated jumper bwetween pins 3 and 4.

NOTE: *Only one jumper should be inserted on jumper header W1 at a time. Inserting multiple jumpers in W1 might damage the JBJGEM.*

2.2.2 PLL Filter Headers (W2, W3)

Use jumper headers W2 and W3 to connect on-board PLL loop filters. Remove both W2 and W3 if using external PLL loop filters.

Figure 2.2 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header W2.

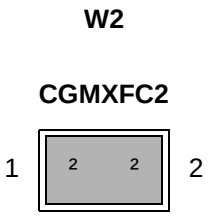


Figure 2-2PLL Filter Header W2

Figure 2.3 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header W3.

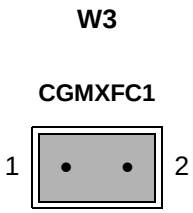


Figure 2-3PLL Filter Header W3

2.2.3 On-Chip 3.3V Regulator Headers (W4, W5)

Use jumper header W4 to select the power source of on-chip 3.3V regulator input for analog modules. Figure 2.4 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header W4 between pins 2 and 3

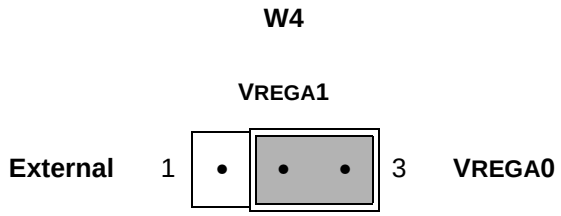


Figure 2-43.3V Regulator Header W4

Use jumper header W5 to select capacitors source of the on-chip 3.3V regulator supply for analog modules.

Figure 2.5 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header W5 between pins 2 and 3

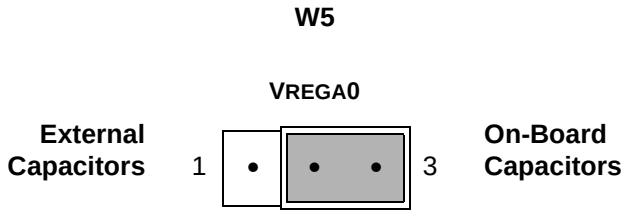


Figure 2-53.3V Regulator Header W5

2.2.4 Analog Module Voltage Headers (W6, W7 & W8)

Use jumper header W7 to select the on-board power supply or an external power supply as the supply of the analog module.

Figure 2.6 shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header W7 between pins 3 and 4.

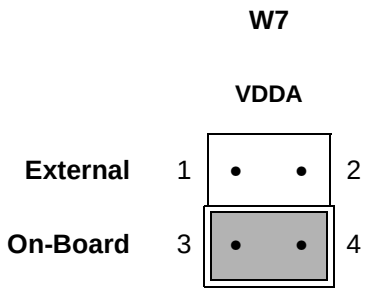


Figure 2-6Configuration Jumper Header W7

Use jumper headers W6 and W8 to select the on-board GND or the external analog ground as the ground connection for the analog module.

Figure 2.7 shows the default factory jumper headers configuration, which has a fabricated jumper installed on jumper header W6 and W8 between pins 3 and 4.

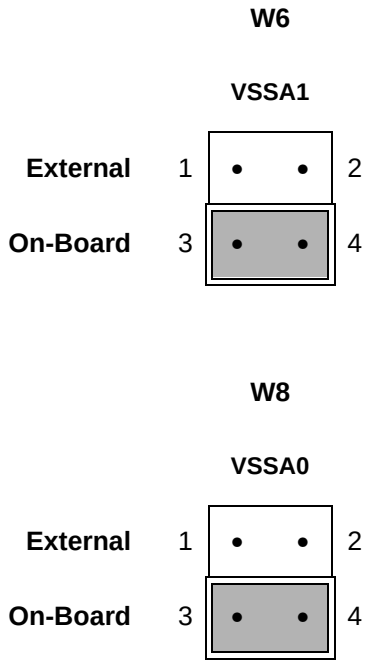


Figure 2-7Configuration Jumper Headers W6 and W8

2.3 Remaining System Installation

When all jumper headers are configured, follow these steps to complete the JBJGEM installation:

Option 1 - To install the JBJGEM in an MMDS station module:

1. Remove the access panel of the station-module enclosure,
2. Insert the EM through the access-panel opening,
3. Fit together EM connectors P4 and P5 (on the bottom of the board) and control-board connectors P11 and P12,
4. Snap the corners of the EM onto the plastic standoffs,
5. Make cable connections to the EM, draping the cables through the side of the access-panel opening, and
6. Replace the access panel, so that cables exit the station-module

Option 2 - To install the JBJGEM on an MMEVS platform board,

1. Fit together EM connectors P4 and P5 (on the bottom of the board) and platform-board connectors P6 and P7.
2. Snap the corners of the EM onto the plastic standoffs.

2.3.1 Personality Files

Copy the personality files from the provided diskette to the host directory that contains the debugging software. The personality files for the JBJGEM are:

- 0045BVxx.MEM — P&E Personality file for MC68HC908JB16 and MC68HC908JG16 MCUs
- 00C5BVxx.MEM — CodeWarrior Personality file for MC68HC908JB16 and MC68HC908JG16 MCUs

2.3.2 System Connections

At this point, make any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

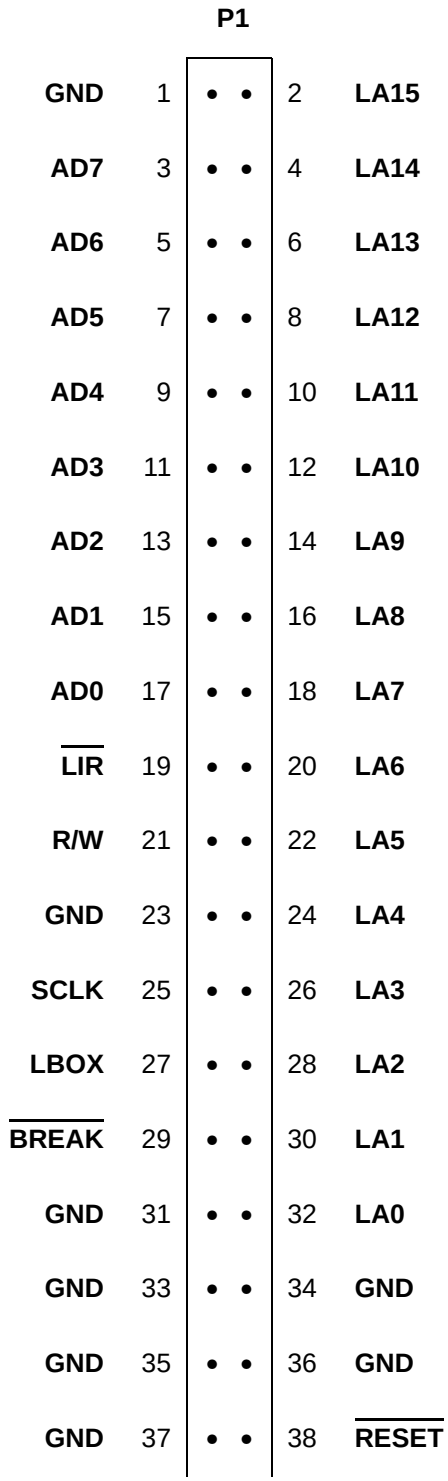
Section 3. Connector Information

3.1 Introduction

This section consists of pin assignments and signal descriptions for M68EM08JBJG target and logic analyzer connectors.

3.2 Logic Analyzer Connector (P1)

Connector P1 is the JBJGEM logic analyzer connector. **Figure 3-1** shows the pin assignments for connector P1. **Table 3-1** gives the signal descriptions.


P1
GND 1 2 LA15
AD7 3 4 LA14
AD6 5 6 LA13
AD5 7 8 LA12
AD4 9 10 LA11
AD3 11 12 LA10
AD2 13 14 LA9
AD1 15 16 LA8
AD0 17 18 LA7
LIR 19 20 LA6
R/W 21 22 LA5
GND 23 24 LA4
SCLK 25 26 LA3
LBOX 27 28 LA2
BREAK 29 30 LA1
GND 31 32 LA0
GND 33 34 GND
GND 35 36 GND
GND 37 38 RESET

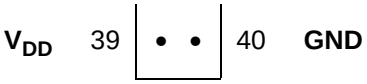


Figure 3-1Logic Analyzer Connector P1 Pin Assignments

Connector Information

Table 3-1Logic Analyzer Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	GROUND
2	LA15	Address bus bit 15 — MCU output address bus
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	LA14	Address bus bit 14 — MCU output address bus
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus.
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	SCLK	System clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus

Table 3-1Logic Analyzer Connector P1 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
33	GND	GROUND
34	GND	GROUND
35	GND	GROUND
36	GND	GROUND
37	GND	GROUND
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1A (max)) used by the EM logic circuits
40	GND	GROUND

3.3 Target Connectors (P2 and P3)

JBJGEM has two target connectors: P2 and P3, each a 2-row by 20-pin connector. **Figure 3-2**, **Table 3-2**, and **Table 3-3** give the pin assignments and signal descriptions for these connectors.

P2

GND	1	•	•	2	**NC**	**OSC1**	1	•	•	2	**NC**
VREGA0	3	•	•	4	**GND**	**VDDA**	3	•	•	4	**NC**
RESET	5	•	•	6	**VREGA1**	**VSSA0**	5	•	•	6	**NC**
PTA1	7	•	•	8	**NC**	**PTA0**	7	•	•	8	**NC**
PTA2	9	•	•	10	**NC**	**GND**	9	•	•	10	**NC**

P3

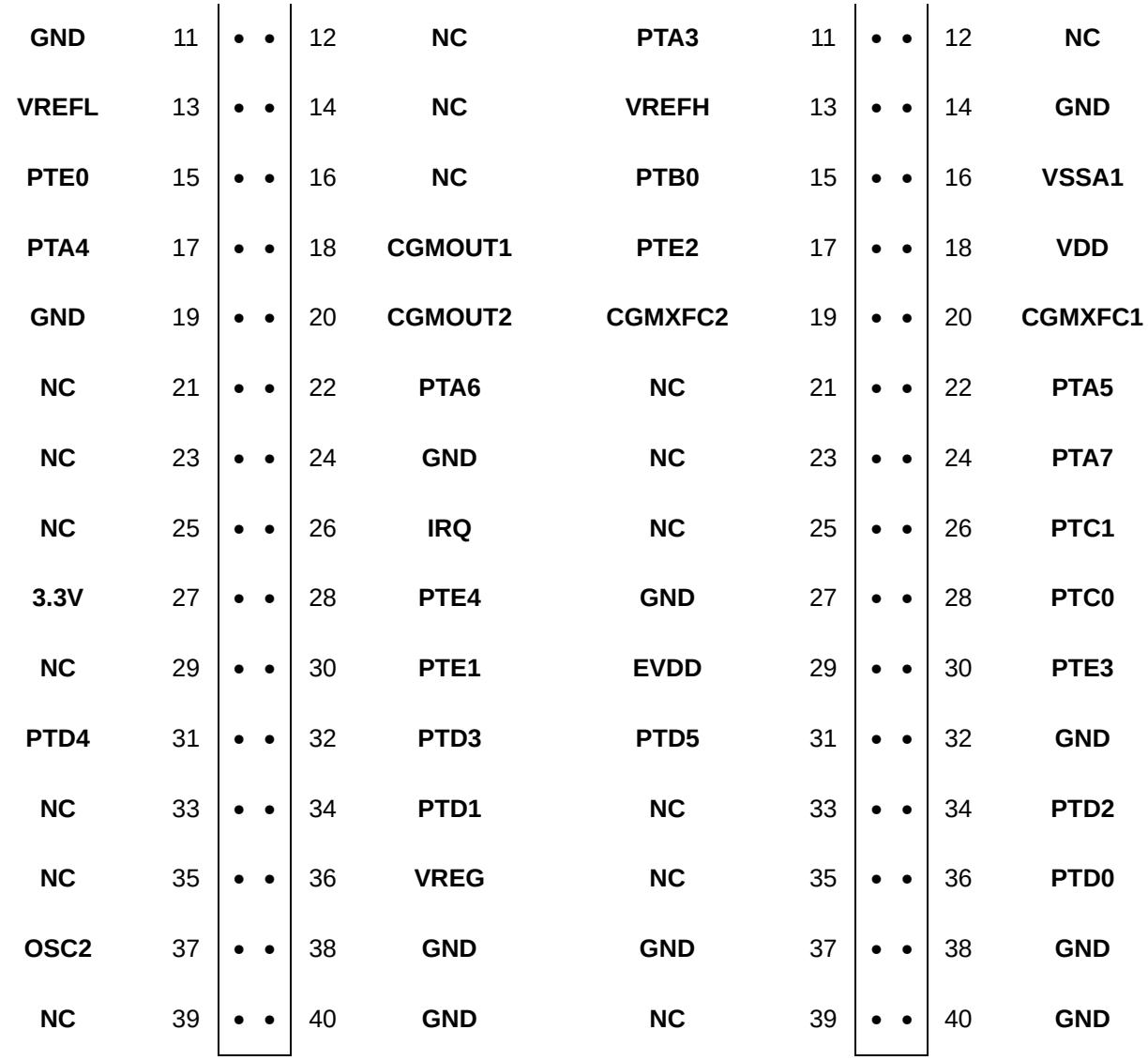


Figure 3-2Target Connectors P2 and P3 Pin Assignments

Table 3-2Target Connector P2 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	EM GROUND — Ground signal of the EM board

Table 3-2Target Connector P2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
2	NC	No connect
3	VREGA0	3.3Vdc output of on-chip regulator for analog module
4	GND	EM GROUND — Ground signal of the EM board
5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
6	VREGA1	3.3Vdc input of on-chip regulator for analog module
7	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
8	NC	No connect
9	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
10	NC	No connect
11	GND	EM GROUND — Ground signal of the EM board
12	NC	No connect
13	VREFL	Reference Low input of ADC module
14	NC	No connect
15	PTE0	PORT E (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
16	NC	No connect
17	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
18	CGMOUT1	CGM clock output pin 1
19	GND	EM GROUND — Ground signal of the EM board
20	CGMOUT2	CGM clock output pin 2
21	NC	No connect
22	PTA6	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	GND	EM GROUND — Ground signal of the EM board
25	NC	No connect
26	$\overline{\text{IRQ}}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt

Table 3-2Target Connector P2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
27	3.3V	JBJGEM 3.3 Volts source — Used for factory testing
28	PTE4	PORT E (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTE1	PORT E (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTD4	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
32	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
33	NC	No connect
34	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
35	NC	No connect
36	VREG	3.3Vdc output of on-chip regulator for MCU operation and USB data driver
37	OSC2	No connect
38	GND	EM GROUND — Ground signal of the EM board
39	NC	No connect
40	GND	EM GROUND — Ground signal of the EM board

Table 3-3Target Connector P3 Signal Descriptions

Pin	Mnemonic	Signal
1	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
2	NC	No connect
3	VDDA	Analog supply pin for analog module
4	NC	No connect
5	VSSA0	GROUND pin for analog module
6	NC	No connect
7	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
8	NC	No connect

Table 3-3Target Connector P3 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
9	GND	EM GROUND — Ground signal of the EM board
10	NC	No connect
11	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	VREFH	Reference High input of ADC module
14	GND	EM GROUND — Ground signal of the EM board
15	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
16	VSSA1	GROUND pin for analog module
17	PTE2	PORT E (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
18	VDD	MMDS/EVS +5V — Used for factory testing
19	CGMXFC2	CGM external filter capacitior pin 2
20	CGMXFC1	CGM external filter capacitior pin 1
21	NC	No connect
22	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
25	NC	No connect
26	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
27	GND	EM GROUND — Ground signal of the EM board
28	PTC0	PORT C (bit 0)— General-purpose I/O lines controlled by software via data direction and data registers
29	EVDD	Target system Voltage high
30	PTE3	PORT E (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
31	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers

Table 3-3Target Connector P3 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
32	GND	EM GROUND — Ground signal of the EM board
33	NC	No connect
34	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
35	NC	No connect
36	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
37	GND	EM GROUND — Ground signal of the EM board
38	GND	EM GROUND — Ground signal of the EM board
39	NC	No connect
40	GND	EM GROUND — Ground signal of the EM board

3.4 Target Cable Assembly

To connect the JBJGEM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-3 shows how one end of the flex cable plugs into the JBJGEM module, and it also shows how the target head connects into the target system.

If the JBJGEM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

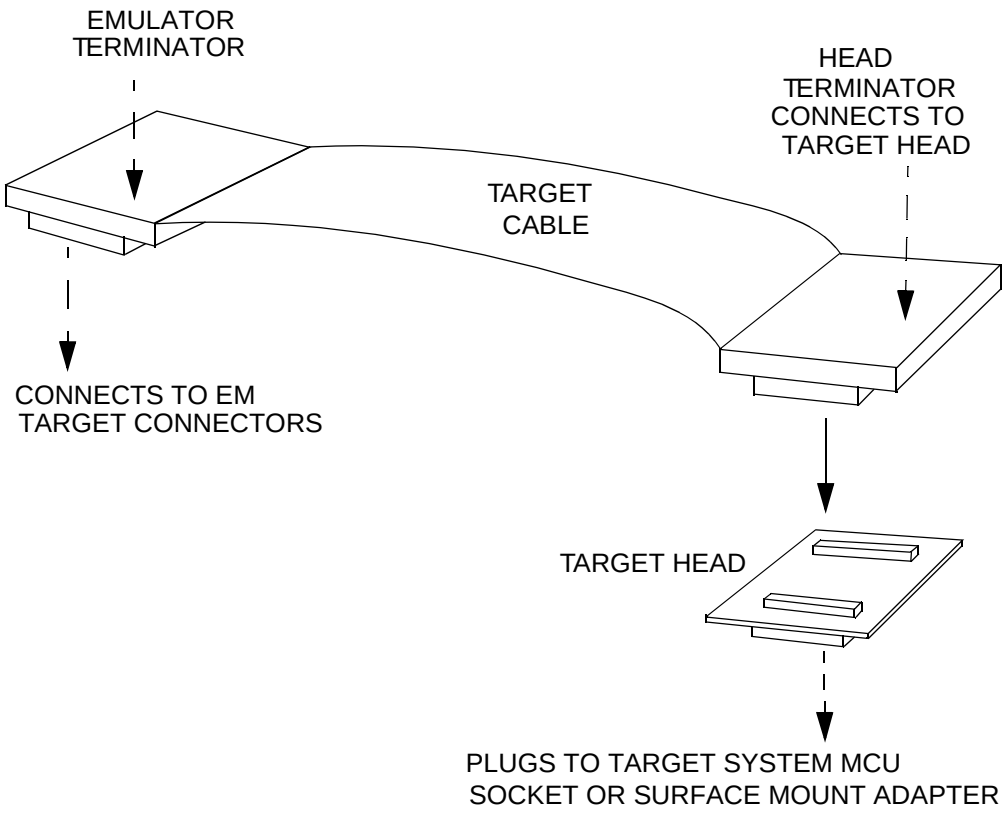


Figure 3-3Target Cable Assembly

Section 4. Limitations

4.1 Introduction

This chapter describes the limitations of the M68EM08JBJG emulator module.

4.2 Electrical Performance of Port A

The Port A is emulated by external circuit. The electrical performance of Port A on JBJGEM is different from Port A of MCU.

4.3 Electrical Performance of Port B

The Port B is emulated by external circuit. The electrical performance of Port B on JBJGEM is different from Port B of MCU.

4.4 Electrical Performance of Port D

The LED driver (Port D) is emulated by external circuit. The electrical performance of Port D on JBJGEM is different from Port D of MCU.

4.5 Electrical Performance of PLL

The electrical performance of PLL measured on JBJGEM may different from the actual performance of MCU. It should not be used as a design reference.

Limitations

HOW TO REACH US:

World Wide Web Address

Motorola: http://www.motorola.com/General/index.html

MOTOROLA