

Product Type	Integrated Communication Processor

Freescale Part #	P5020, P5010
Package	1295 FC PBGA
Crypto Hardware	SEC 4.2

<u>Algorithms</u>	<u>Max Key Size (bits)</u>
DES (ECB, CBC, OFB, CFB)	56
3DES (ECB, CBC, OFB, CFB)	168 (3-keys)
AES (ECB, CBC, CTR, CCM, CMAC, GCM, OFB, CFB, XCBC-MAC)	256
ARC-4	128
MD-5 + HMAC	(up to 512 bit keys)
SHA-1 + HMAC	(up to 512 bit keys)
SHA-224 + HMAC	(up to 512 bit keys)
SHA-256 + HMAC	(up to 512 bit keys)
SHA-384 + HMAC	(up to 512 bit keys)
SHA-512 + HMAC	(up to 512 bit keys)
Kasumi (A5/3, GEA-3, f8, f9)	128
Snow 3G	128
RSA Digital Signature	4096-bit operands
RSA Digital Verify	4096-bit operands
ECC Digital Signature	1023-bit field or modulus size
ECC Digital Verify	1023-bit field or modulus size

Target Applications : Control processing for Routers, Storage Arrays, Industrial Single Board Computers

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FIPS compliant deterministic RNG

Overview:

The P5020 and P5010 are members of the QorlQ family of integrated communications processor from Freescale Semiconductor. The P5020 incorporates 2 64b e5500 Power Architecture CPU cores, 2 DDR3/3L Memory Controllers, 1 10G ethernet and 5 1G Ethernet controllers, along with multiple PCIe and sRIO peripheral bus controllers. The P5010 incorporates 1 64b e5500 Power Architecture CPU cores and 1 DDR3/3L Memory Controller, otherwise the features are the same as the P5020. In addition to these CPUs and interfaces, the P5020 and P5010 integrate a 5Gbps Pattern Matching Engine (regex), and a 5Gbps Crypto Acceleration Engine (SEC 4.2). The algorithms and key lengths supported by the SEC 4.2 are listed in the table above.

On chip 32-bit



In addition to crypto algorithm processing, the SEC 4.2 supports security protocol processing off-load capability, with specific support for protocol header and trailer processing for IPsec, SSL, DTLS, SRTP, MACSec, 802.16e, and 802.11e. The SEC 4.2 is expected to achieve 5000+ public key exchanges per second.

The P5020 & P5010 also provide support for secure boot and platform assurance.

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