i.MX31ADS
Application Development System

User's Manual

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Preliminary

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About This Book

This manual explains how to connect and operate the i.MX31ADS Application Development System.

Audience

The audience for this manual is handheld communication device designers. It is assumed that users are engineers or technicians with experience using development systems.

Organization

The manual consists of three chapters.

- Chapter 1 introduces the user to the features and capabilities of the ADS.
- Chapter 2 provides configuration and set-up information.
- Chapter 3 provide operational information.
- Chapter 4 provides connector locations, functions, pin assignments, and signal descriptions.

Revision History

This is a new document.

Conventions

Units and measures in this manual conform to the International System of Units (SI) as defined by United States National Institute of Standards and Technology Special Publication 811.

Ranges of bits and signals are shown in square brackets: A[15:0].

Individual signals and bits within a range are shown with a numeric designator only: A7.

Logic level 0 is the voltage that corresponds to Boolean 0; logic level 1 is the voltage that corresponds to Boolean 1.

When a signal is asserted, it goes to the active logic state. Active-high signals go to logic level 1; active-low signals go to logic level 0.

When a signal is negated, it goes to the inactive logic state. Active-high signals go to logic level 0; active-low signals go to logic level 1.

Setting a bit refers specifically to establishing logic level 1 on the bit; clearing a bit refers specifically to establishing logic level 0 on the bit. Ranges of bits may be set or cleared by a single operation.

Overbars are used to show active-low or complemented signals and bits in text: $\overline{\text{SIGNAL}}$, $\overline{\text{BIT}}$. Active-low signal names are designated by the suffix “_b”: signal_name_b.

Acronyms and Abbreviations

The following acronyms and abbreviations are used in this manual. This list does not include signal, register, and software mnemonics.

ADS	Application Development System
APMSMC13783	Power Management System
ATA	Hard drive interface spec
CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
CSPI	Serial Peripheral Interface
DCE	Data Communications Equipment
DDR	Double Data Rate
DIN	Deutsches Institut für Normung
DIP	Dual In-line Package
DMA	Direct Memory Access
DTE	Data Terminal Equipment
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Eraseable Programmable Read Only Memory
EPROM	Eraseable Programmable Read Only Memory
FIR	Infra Red
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/Output
IrDA	Infrared Data Association
ISA	Instrumentation, System, and Automation Society
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card

MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random Access Memory
OTG	On the Go
PC	Personal Computer
PCMCIA	Personal Computer Memory Card International Association
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card International Association
PHY	Physical interface
POR	Power On Reset
PSRAM	Pseudo Random Access Memory
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	Smart Digital
SDRAM	Synchronous Dynamic Random Access Memory
SI	Systeme International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPST	Single Pole Single Throw
SSI	Synchronous Serial Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Chapter 1 General Information

1.1 Description

The i.MX31ADS helps you develop multimedia communication applications using the i.MX31's ARM11 MCU and the MC13783 audio and power management chip.

The ADS consists of a Base board, a CPU board, and an MC13783 board. The system supports application software development, target board debugging, and optional circuit cards. The CPU board can be run in stand-alone mode for code development. An LCD display panel, an image sensor, and a separate keypad are supplied with the ADS. The image sensor can be connected to the base board in different orientations.

Figure 1-1 shows the major components of the ADS.

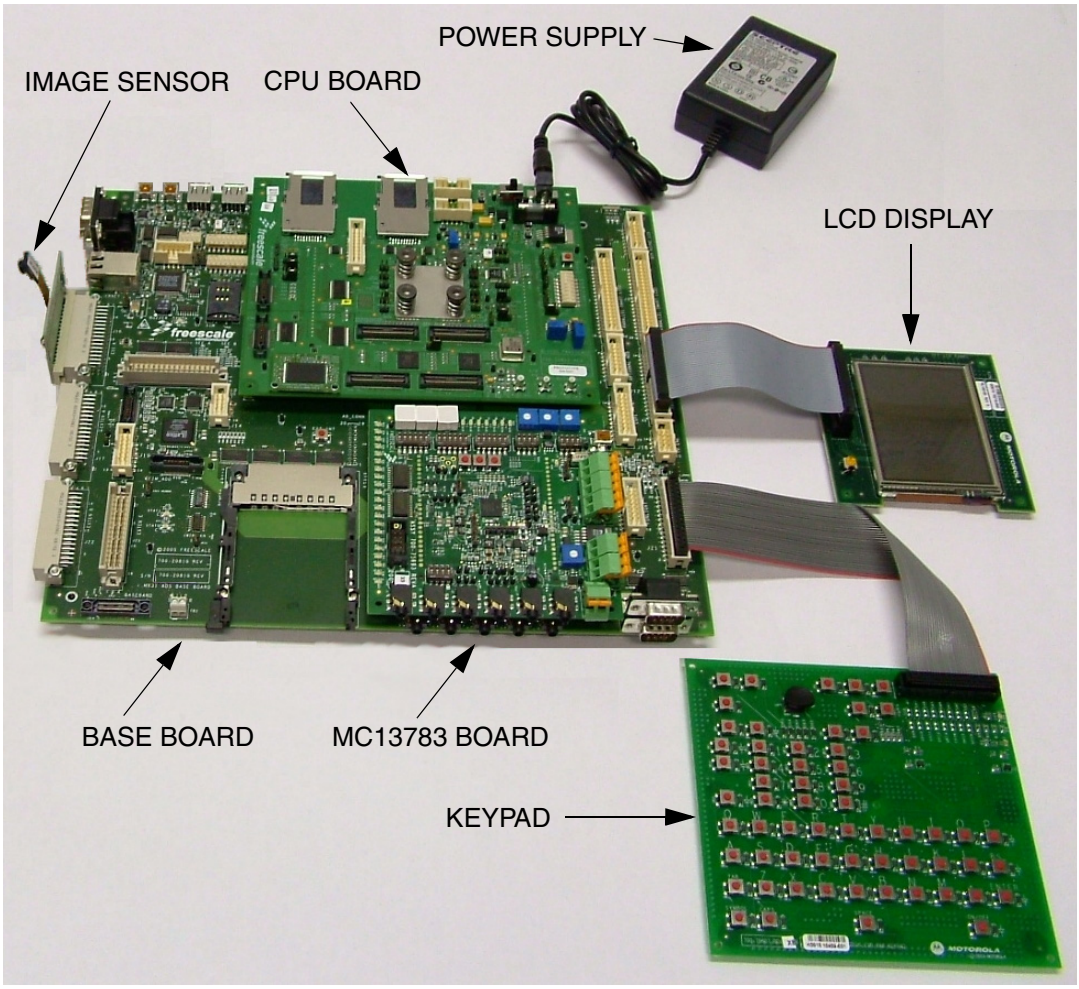


Figure 1-1. i.MX31ADS Application Development System

1.2 i.MX31ADS Features

ADS features include:

- Three board system
  - — Base board with display and interface connectors
  - — CPU board with i.MX31 ARM11 MCU
  - — Power management board with MC13783 chip
- +5.0 VDC, 2.4 A universal power supply
- QVGA LCD display panel with touchscreen capability and LED backlight
- Keypad with 64 push button keys
- Image sensor camera
- Configurable intelligent management of system power
- Separate selectable voltage regulators for running the CPU board in stand-alone mode
- Two selectable system clock sources, 32.768 kHz and 26 MHz
- Onboard CPLD that manages memory-mapped expansion I/O, interrupts, and general-purpose I/O
- Multi-ICE debug support
- 32 MB of 16-bit NOR burst flash memory
- 16 MB of 16-bit PSRAM
- 128 MB of 32-bit DDR SDRAM memory
- Two sets of two memory card connectors, selectable as SD/MMC (on Base board) or MS (on CPU board), with card-sense functionality
- 1G-bit x8 data NOR Flash on a removable card
- SIMM card connector
- PCMCIA connector
- NAND Flash card connector
- Three RS-232 interfaces with DB-9 connectors driven by UART channels internal to the MX31. Each interface has two UART options and power up enable DIP switches. One supports DCE with optional full modem controls, another is DTE with optional full modem controls, and the third is DTE with RTS/CTS controls only.
- An external DUART configured as two RS-232 DCE channels (one DB9 connector, one 10-pin header)
- Two USB host transceivers, one full-speed and one high-speed, with standard USB host connectors
- Three USB OTG transceivers, one full-speed and one high-speed on the Base board, one full-speed on the MC13783 board, with mini AB connectors
- 10 Base-T Ethernet controller with RJ-45 connector with built-in data flow LED indicators
- IrDA Specification 1.4 transceiver supports fast, medium, and slow operating modes
- ATA5 controller with 44-position dual row, 2 mm header for small form-factor disk drives
- I2C interface with one of two selectable MCU interfaces
- CSPI connector

- Two CSI connectors, with different image sensor orientations
- Smart serial LCD display connector
- QVGA LCD display connector with touch screen interface plus companion connector with additional control signals
- Two smart parallel LCD display connectors
- TV encoder connector
- Keypad connector
- Interface connector to baseband processor
- Audio synthesizer chip with microphone and line inputs (3.5 mm jacks); line, voice, and headphone outputs (3.5 mm jacks); and speaker output (screw terminals)
- Eight DIP configuration switches with user-definable functions
- Software-readable CPU and Base board versions
- LED indicators for +5V IN, 3.3V, vibrator output, and synthesizer output.
- Two LED indicators for user-defined function
- Piezoelectric audible alert and vibratory alert
- Three funlight indicators and funlight connector
- Push button Reset (on CPU) or reset control from MC13783
- 1-wire EPROM
- Push button interrupt source
- Two Mictor LA/SW Analysis Connectors (Base board)
- Four Samtec LA Connectors (CPU)
- Three Extension connectors, two are compatible with the MX21 ADS Extension connectors
- Special MC13783 board features
  - Stereo microphone jack, normal microphone jack, external TXIN jack, headphone jack, low level stereo input and output jacks, stereo and mono (ear piece) speaker terminals
  - Main battery emulation from +5V
  - Main battery connection terminals
  - Back up battery emulation (super cap)
  - Coin cell (backup) battery connection terminals
  - Battery charger input terminals
  - Backlight LED indicators
  - Three Push button switches to act as power on/off switches
  - DIP switches to select default power up power and power sequencing.
  - USB mode, USB enable, and WDI disable DIP Switches.
  - Audio clock source selection DIP Switches.
  - Individual test point and LED indicator for each MC13783 voltage
- USB cables, RS-232 serial cable, and two RJ-45 Ethernet cables, network, and crossover

1.3 System and User Requirements

To use the ADS, you need:

- An IBM PC or compatible computer that has:
  - A Microsoft Windows 98, Windows ME, Windows 2000, Windows XP, or Windows NT (version 4.0) operating system
  - A parallel port and a Multi-ICE device (not included)
- A + 5 VDC, 2.4 A power supply with a 2 mm female (inside positive) power connector (included)

CAUTION

Never supply more than +5.5-volts power to the i.MX31ADS.
Doing so can damage board components.

1.4 ADS Specifications

Table 1-1 shows i.MX31ADS specifications.

Table 1-1. Specifications

Characteristic	Specifications
Clock speed	Selectable 32.768 kHz or 26 MHz
Temperature: Operating Storage	 -10° to +50° C -40° to +85° C
Relative humidity	0 to 90% (noncondensing)
Power requirements	4.5V to 5.5 VDC @ 2.4 A
Dimensions	10.75” x 11.875” in (273 mm x 302 mm)

Chapter 2 Configuring and Connecting the ADS

2.1 Introduction

This section contains configuration information, connection descriptions, and other operational information that may be useful during the development process.

2.2 Base Board Configuration

2.2.1 Base Board Configuration Switches

The Base board has one four-switch DIP module (SW1) and two eight-switch DIP modules (SW2 and SW3). Figure 2-1 shows the location of the switches.

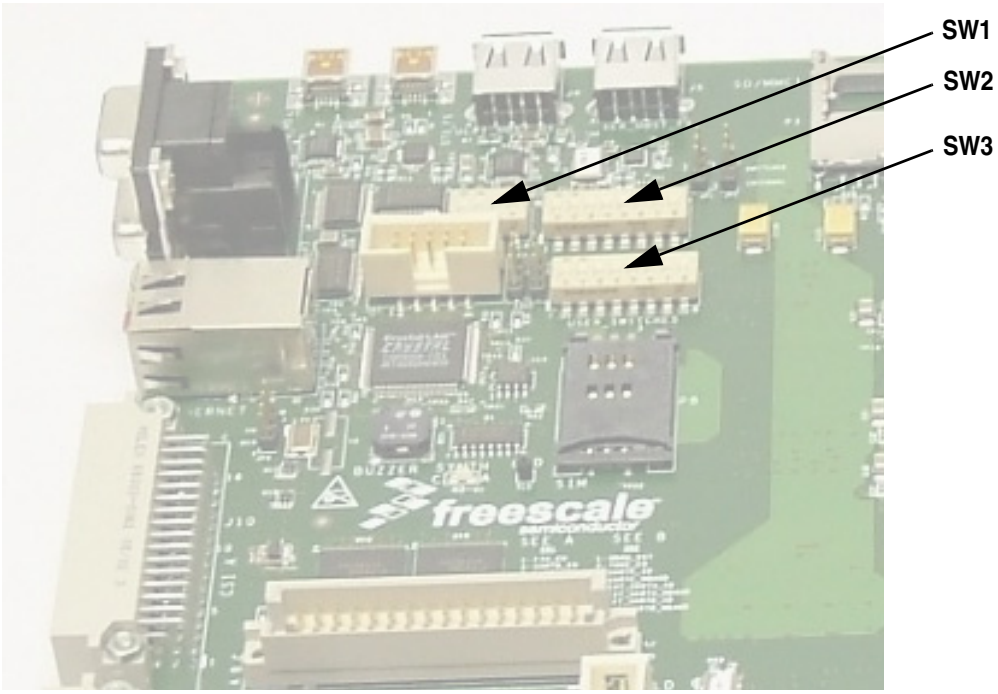


Figure 2-1. Base Board Configuration Switches

2.2.1.1 SW1 – UART Enable Switches

Table 2-1 shows SW1 switch functions. Each ADS UART transceiver can be connected to two different MCU UART channels. CPLD settings determine which UARTs are enabled at start-up (see paragraph 3.3 for more information). The four SPST slide switches in SW1 control the power-up status of the UARTs and the IrDA transceiver. Setting a switch to ON makes the UARTA, UARTB, UARTC, or FIR interface active on ADS power up. Enabling an interface allows it to be used immediately by software without additional configuration. Setting a switch to OFF disables an interface until it is enabled by software.

Table 2-1. Base Board SW1 Switch Function

Switch Designation	i.MX31 UART Channel	Setting	Effect
SW1- 1 FIR EN	UART5	ON	ENABLED
	Default UART	OFF	DISABLED
SW1- 2 UARTB EN	UART3	ON	ENABLED
	Default UART	OFF	DISABLED
SW1- 3 UARTA EN	UART1	ON	ENABLED
	Default UART	OFF	DISABLED
SW1- 4 UARTC EN	UART2	ON	ENABLED
	Default UART	OFF	DISABLED

2.2.1.2 SW2 – RS-232 MBaud, Shut Down, WDI, and Buzzer Enable Switches

Table 2-2 shows SW2 switch functions. The eight SPST slide switches in SW2 control system baud rate, shutdown, watchdog interface, and buzzer enable functions.

Set SW2-1 to ON to enable the MC13783 Watch Dog Interrupt function. When enabled, software must pulse this output within a window of time or the MC13783 will shut down the system.

Set SW2-2 to ON to connect the PWM output to the buzzer circuit.

Set SW2-3, SW2-5, or SW2-7 to ON to shut down the associated RS-232 transceiver. This minimizes current consumption when the transceivers are not used.

Set SW2-4, SW2-6, or SW2-8 to ON to enable the RS-232 transceivers for UARTC and DUART channels A and B to operate at rates up to 1 MBaud. Lower rates can reduce system power consumption and EMI.

Table 2-2. Base Board SW2 Switch function

Switch Designation	Setting	Effect
SW2- 1 WDI Enable	ON	Connects the Watch Dog Reset to MC13783
	OFF	Watch Dog Reset is not connected to MC13783
SW2- 2 Buzzer Enable	ON	PWM output is connected to the buzzer
	OFF	PWM output is not connected to the buzzer
SW2- 3 UARTC Shut Down	ON	UARTC transceiver is shut down
	OFF	UARTC transceiver is enabled
SW2- 4 UARTC MBAUD	ON	UARTC Baud Rate limited to 250kbps
	OFF	UARTC Baud Rate limited to 1Mbps
SW2- 5 Ext UA Shut Down	ON	External UARTA transceiver is shut down
	OFF	External UARTA transceiver is enabled
SW2- 6 Ext UA MBAUD	ON	External UARTA Baud Rate limited to 250kbps
	OFF	External UARTA Baud Rate limited to 1Mbps
SW2- 7 Ext UB Shut Down	ON	External UARTB transceiver is shut down
	OFF	External UARTB transceiver is enabled
SW2- 8 Ext UB MBAUD	ON	External UARTB Baud Rate limited to 250kbps
	OFF	External UARTB Baud Rate limited to 1Mbps

2.2.1.3 SW3 – User Defined Switches

Table 2-3 shows SW3 switch functions. The settings of the eight SPST slide switches in SW3 may be read by software to implement user-defined functions. The switch settings are read on data bits D[7:0].

Table 2-3. SW3 Switch Settings

Switch Designation	Setting	Effect
SW3- 1 User Defined S0	ON	D0 Reads low (zero)
	OFF	D0 Reads high (one)
SW3- 2 User Defined S1	ON	D1 Reads low (zero)
	OFF	D1 Reads high (one)
SW3- 3 User Defined S2	ON	D2 Reads low (zero)
	OFF	D2 Reads high (one)
SW3- 4 User Defined S3	ON	D3 Reads low (zero)
	OFF	D3 Reads high (one)
SW3- 5 User Defined S4	ON	D4 Reads low (zero)
	OFF	D4 Reads high (one)
SW3- 6 User Defined S5	ON	D5 Reads low (zero)
	OFF	D5 Reads high (one)
SW3- 7 User Defined S6	ON	D6 Reads low (zero)
	OFF	D6 Reads high (one)
SW3- 8 User Defined S7	ON	D7 Reads low (zero)
	OFF	D7 Reads high (one)

2.2.2 Base Board Jumper Headers

The Base board has 26 jumper headers. JP1 to JP8, J12, and J14 set ADS operational parameters. JP9 to JP11 and JP13 are used as external signal headers. JP15 to JP26 select voltage sources when MC13783 power management functions are used. Table 2-4 describes the Base board jumpers. Figure 2-2 shows the jumpers on the left side of the board; Figure 2-3 shows the jumpers on the right side of the board.

Table 2-4. Base Board Jumper Headers

Jumper Designation	Pin Connection	Effect
JP1 HS OTG VUSB Source	1-2	FLAG output of Switcher
	2-3	GND
JP2 HS HOST VUSB Source	1-2	FLAG output of Switcher
	2-3	GND
JP3 SERIAL LCD CS	1-2	LCS1
	2-3	SCLK0
JP4 SD1 POWER	1-2	VSD1
	2-3	3.3 VDC (Do not jumper when R28 is installed)
JP5 SD2 POWER	1-2	VSD2
	2-3	3.3 VDC (Do not jumper when R33 is installed)
JP6 I2C – FS OTG PHY	1-2	I2C3 (Secondary function of the CSPI2_CLK and CSPI_SS2 pins)
	2-3	I2C1 (Must be same as JP7)

Table 2-4. Base Board Jumper Headers (continued)

Jumper Designation	Pin Connection	Effect
JP7 I2C – FS OTG PHY	1-2	I2C3 (Secondary function of the CSPI2_CLK and CSPI_SS2 pins)
	2-3	I2C1 (Must be same as JP6)
JP8 NVRAM – Ethernet PHY	1-2	Enable NVRAM to Ethernet PHY
	2-3	Disable NVRAM to Ethernet PHY
JP9 (Signal Input)	1	CODE_TEST_CS_B Input
JP10 (Signal Input)	1	BCLK0 Input
JP11 (Signal Input)	1	BRW_B Input
JP12 Keypad Light Sense	1-2	LIGHT SENSE
	2-3	AD5
JP13 (I2C Connection)	1	I2C1_CLK
	2	I2C1_DAT
	3	SIGNAL GROUND
JP14 1 Wire Enable	1&2	Jumper, 1-wire EEPROM programming enabled No jumper, 1-wire EEPROM programming disabled
JP15 NVCC 1	1-2	PM_VIOLO
	2-3	PM_VIOHI
JP16 NVCC 3	1-2	PM_VIOLO
	2-3	PM_VIOHI
JP17 NVCC 3	1-2	3.3 VDC
	2-3	Selected by JP18
JP18 NVCC 3	1-2	Selected by JP16
	2-3	Selected by JP19
JP19 NVCC 3	1-2	VSD1
	2-3	VSD2
JP20 NVCC 4	1-2	PM_VIOLO
	2-3	PM_VIOHI
JP21 NVCC 5	1-2	PM_VGEN
	2-3	PM_VREF1
JP22 NVCC 6&9	1-2	PM_VGEN
	2-3	PM_VREF1
JP23 NVCC 7	1-2	PM_VIOLO
	2-3	PM_VIOHI
JP24 NVCC 8	1-2	PM_VGEN
	2-3	PM_VREF1
JP25 NVCC 6&9	1-2	PM_SIM
	2-3	Selected by JP26
JP26 NVCC 9	1-2	Selected by JP22
	2-3	3.3 VDC

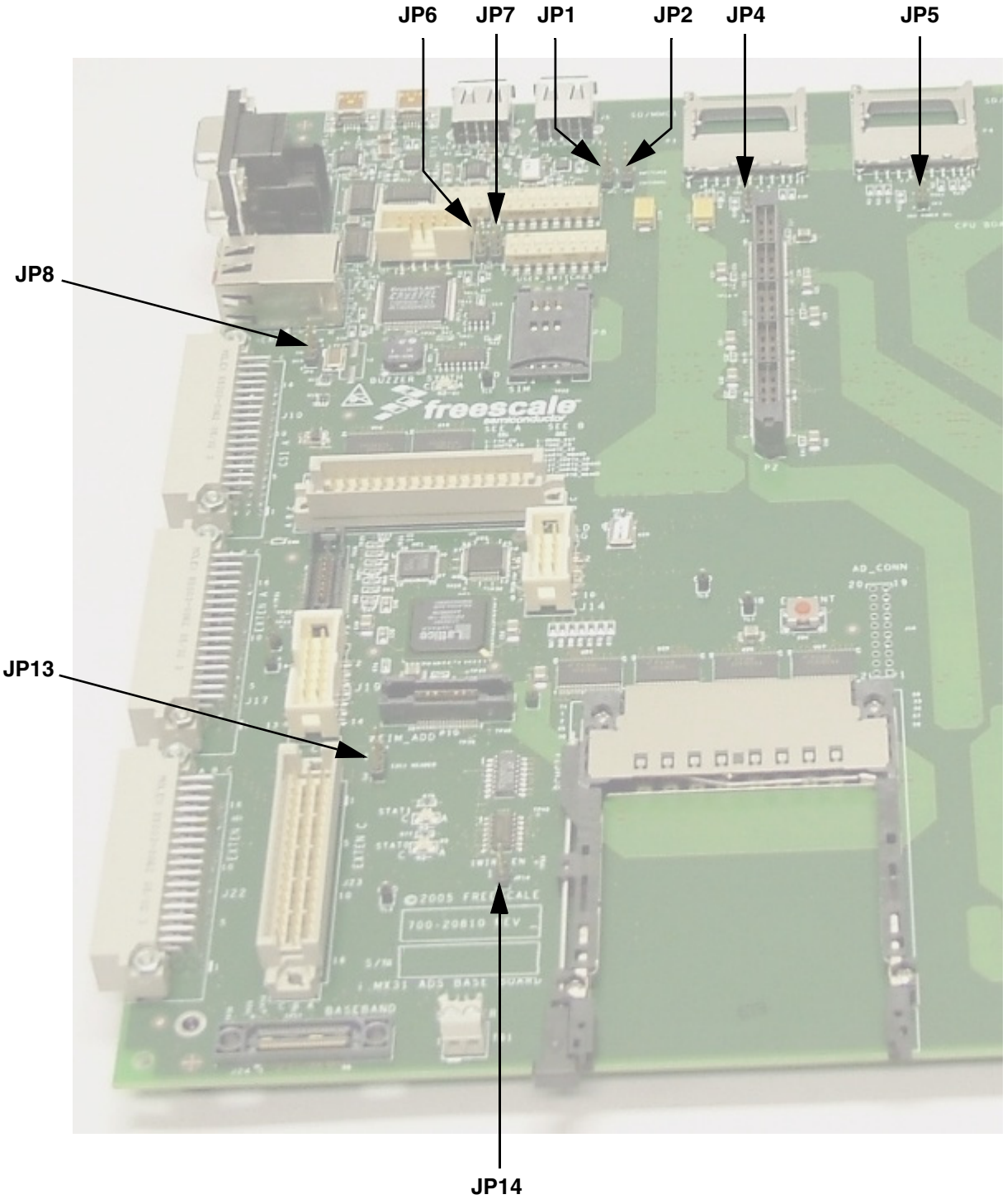


Figure 2-2. Base Board Jumpers — Left Side

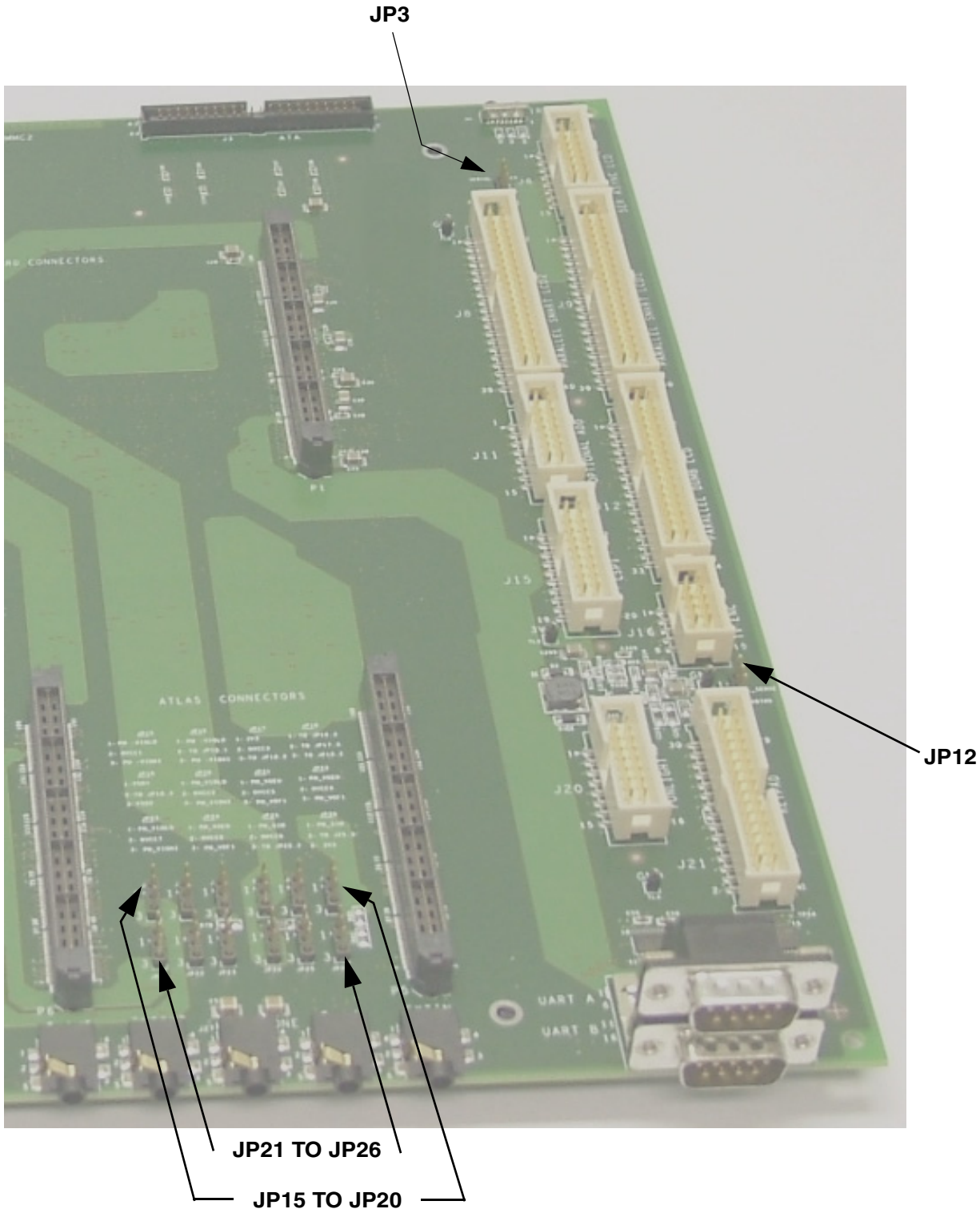


Figure 2-3. Base Board Jumpers — Right Side

2.3 CPU Board Configuration

2.3.1 CPU Board Switches

The CPU board has one SPST slide power switch (S1), a push button reset switch (SW1), and an eight-switch DIP module (SW2). Figure 2-4 shows the location of the switches.

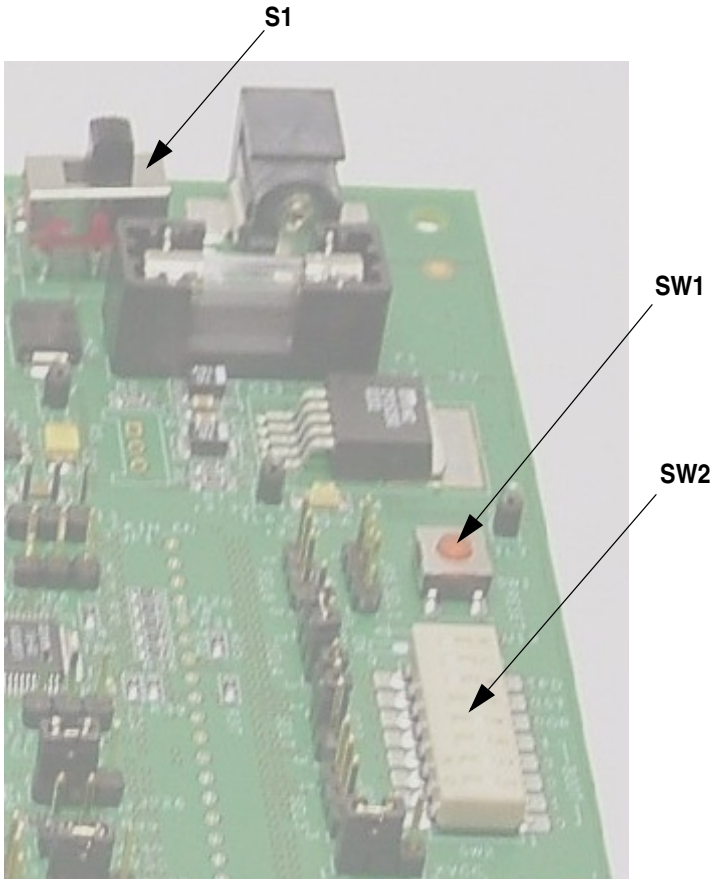


Figure 2-4. CPU Board Switches

2.3.1.1 S1 – Power Switch

Slide S1 to ON to power up the CPU board in stand-alone mode, or to power up the ADS when the CPU board is connected to the Base board.

2.3.1.2 SW1 – Reset Switch

Push SW1 to reset the ADS. SW2-6 and SW2-7 determine the actual effect of SW1.

2.3.1.3 SW2 – Boot Mode Switches

SW2-1 to SW2-5 settings determine where the processor begins program execution. Table 2-5 shows all valid combinations of the switches. Other combinations are reserved and must not be used.

Table 2-5. Boot Mode Switch Settings

Boot Mode Device	BOOT4 SW2-5	BOOT3 SW2-4	BOOT2 SW2-3	BOOT1 SW2-2	BOOT0 SW2-1
UART/USB bootloader	ON	ON	ON	ON	ON
8-bit NAND Flash (2KB page) Int	ON	ON	ON	ON	OFF
8-bit NAND Flash (512B page) Int	ON	ON	ON	OFF	OFF
16-bit NAND Flash (2KB page) Int	ON	ON	ON	OFF	OFF
16-bit NAND Flash (512B page) Int	ON	ON	OFF	ON	ON
16-bit CS0 at D[15:0] Int	ON	ON	OFF	ON	OFF
M-System Disk on Chip	ON	OFF	ON	ON	ON
8-bit NAND Flash (2KB page) Ext	OFF	ON	ON	ON	ON
8-bit NAND Flash (512B page) Ext	OFF	ON	ON	ON	OFF
16-bit NAND Flash (2KB page) Ext	OFF	ON	ON	OFF	OFF
16-bit NAND Flash (512B page) Ext	OFF	ON	ON	OFF	OFF
16-bit CS0 at D[15:0] Ext	OFF	ON	OFF	ON	ON
Test Mode	OFF	OFF	ON	OFF	OFF

2.3.1.4 SW2 – Power-On Reset Switch

SW2-6 ON connects the PB RESET output to the POR pin of the MCU.

SW2-6 OFF disconnects the PB RESET output from the POR pin of the MCU.

2.3.1.5 SW2 – Reset Out Switch

SW2-7 ON connects RESET chip output to the system RESET _OUT line.

SW2-7 OFF disconnects the RESET chip output from the system RESET _OUT line.

2.3.1.6 SW2 – Tamper Detect Switch

SW2-8 ON connects GPIO1_6 pin of the MCU to ground, for use as a tamper detect switch.

SW2-8 OFF disconnects GPIO1_6 pin of the MCU from ground and allows the signal to be pulled high.

2.3.2 CPU Board Jumper Headers

The CPU board has 38 jumper headers. JP1, JP2. JP22, and JP26 determine the source of the system reset signal and clock. JP6 and JP10 control the LA and JTAG interfaces. JP3 to JP5, JP12, JP13, JP16, JP17, JP20, JP23, JP28, JP31, JP32, and JP35 to JP38 select power options. The remaining two-pin jumpers provide access to 1 Ohm shunt resistors for current/power measurement. Table 2-6 describes the CPU board jumpers. Jumpers that are critical to stand-alone and APMS operation are shaded. Figure 2-5 shows the locations of the jumpers on the board.

CAUTION

To avoid damage to the ADS, remove the CPU board power jumper shunts when the MC13783 power management system is used. . Do not interchange them with other shunts. Before connecting the MC13783 board, move the power shunts to the Base board and use them to set MC13783 output voltages for the NVCC power rails.

Table 2-6. CPU Board Jumper Headers

Jumper Designation	Pin Connection	Effect
JP1 CKIH Enable	1-2	Use on-board 26 MHz oscillator
	2-3	Use TV encoder oscillator
	NC	Use external clock source connected to J12
JP2 Reset Source Select	1-2	Connect MCU POR_B to MCU RESET_IN_B (use for stand-alone mode)
	2-3	Connect PM_RST_B and RST_OUT_B to MCU RESET_IN_B
JP4 NVCC SEL8	1-2	Select 2.7 VDC Source for NVCC8 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC8 (remove when APMS is used)
JP5 NVCC SEL1	1-2	Select 2.7 VDC Source for NVCC1 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC1 (remove when APMS is used)
JP6 LA DATA enable	1-2	Disable Data to Base board LA connectors (use for stand-alone mode)
	2-3	Enable Data to Base board LA connectors (does not include DRAM bus)
JP7 NVCC5 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP8 QARM Shunt	1&2	Remove jumper to measure voltage drop across two 20 mOhm resistors (jumper is not required for normal operation)
JP9 NVCC8 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP10 SJC_MOD JTAG Mode Select	1&2	Jumper, ARM JTAG interface enabled No jumper, ARM JTAG interface disabled, other JTAG can be used
JP11 NVCC6 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP12 QARM Power Select	1-2	Use on-board voltage regulators (use for stand-alone mode)
	2-3	Use MC13783 power
JP13 NVCC SEL6 & 9	1-2	Select 2.7 VDC Source for NVCC6&9 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC6&9 (remove when APMS is used)
JP14 NVCC3 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP15 NVCC9 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP16 NVCC SEL4	1-2	Select 2.7 VDC Source for NVCC4 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC4 (remove when APMS is used)
JP17 QPER Power Select	1-2	Use on-board voltage regulators (use for stand-alone mode)
	2-3	Use MC13783 power
JP18 NVCC1 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)

Table 2-6. CPU Board Jumper Headers (continued)

Jumper Designation	Pin Connection	Effect
JP19 QL2 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP20 QL2 Power Select	1-2	Use on-board voltage regulators (use for stand-alone mode)
	2-3	Use MC13783 power
JP21 NVCC4 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP22 CLK_SEL CPU Clock Select	1-2	Use 26 MHz clock (CKIH)
	2-3	Use 32 kHz clock (CKIL)
JP23 NVCC SEL7	1-2	Select 2.7 VDC Source for NVCC7 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC7 (remove when APMS is used)
JP24 NVCC10 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP25 NVCC7 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP26 CKIL_EN Clock Input Select	1-2	Use on-board 26 MHz oscillator
	2-3	Use MC13783 board 32 KHz clock
	NC	Use external clock source connected to J10
JP27 XVCC Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP28 NVCC SEL5	1-2	Select 2.7 VDC Source for NVCC5 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC5 (remove when APMS is used)
JP29 NVCC2 Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP30 FVCC Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP31 SVCC Connect	1&2	Jumper, SVCC connected to UVCC and MVCC (normal connection) No jumper, SVCC floating (disables ADS).
JP32 XVCC Power Select	1-2	Use on-board voltage regulators (use for stand-alone mode)
	2-3	Use MC13783 power
JP33 QPER Shunt	1&2	Remove jumper to measure voltage drop across 20 mOhm resistor (jumper is not required for normal operation)
JP34 IOQVDD Shunt	1&2	Remove jumper to measure voltage drop across 1 Ohm resistor (jumper is not required for normal operation)
JP35 FVCC Power Select	1-2	Use on-board voltage regulators (use for stand-alone mode)
	2-3	Use MC13783 power
JP36 NVCC SEL3	1-2	Select 2.7 VDC Source for NVCC3 (remove when APMS is used)
	2-3	Select 1.8 VDC Source for NVCC3 (remove when APMS is used)
JP37 FUSE_VDD Select	1-2	Select 1.8 VDC fuse pin voltage
	2-3	Select 3.3 VDC fuse pin voltage (do not use when R227 is installed)
JP38 DRAM VDD_SEL	1-2	Connect DRAM to NVCC2 (use for stand-alone mode)
	2-3	Connect DRAM to MC13783 board PM_BKUP_DDR

JP12, JP17, and JP 20 select either the on-board regulators or APMS, and all must be set the same. JP32 and JP35 also select either the on-board regulators or APMS, and both must be set the same, but

JP32 and JP35 setting does not have to be the same as JP12, JP17, and JP20 setting. JP31 must be in place for the ADS to operate. The JP38 shunt must connect pins 1 and 2 in stand-alone operation, but either setting can be used in APMS operation.

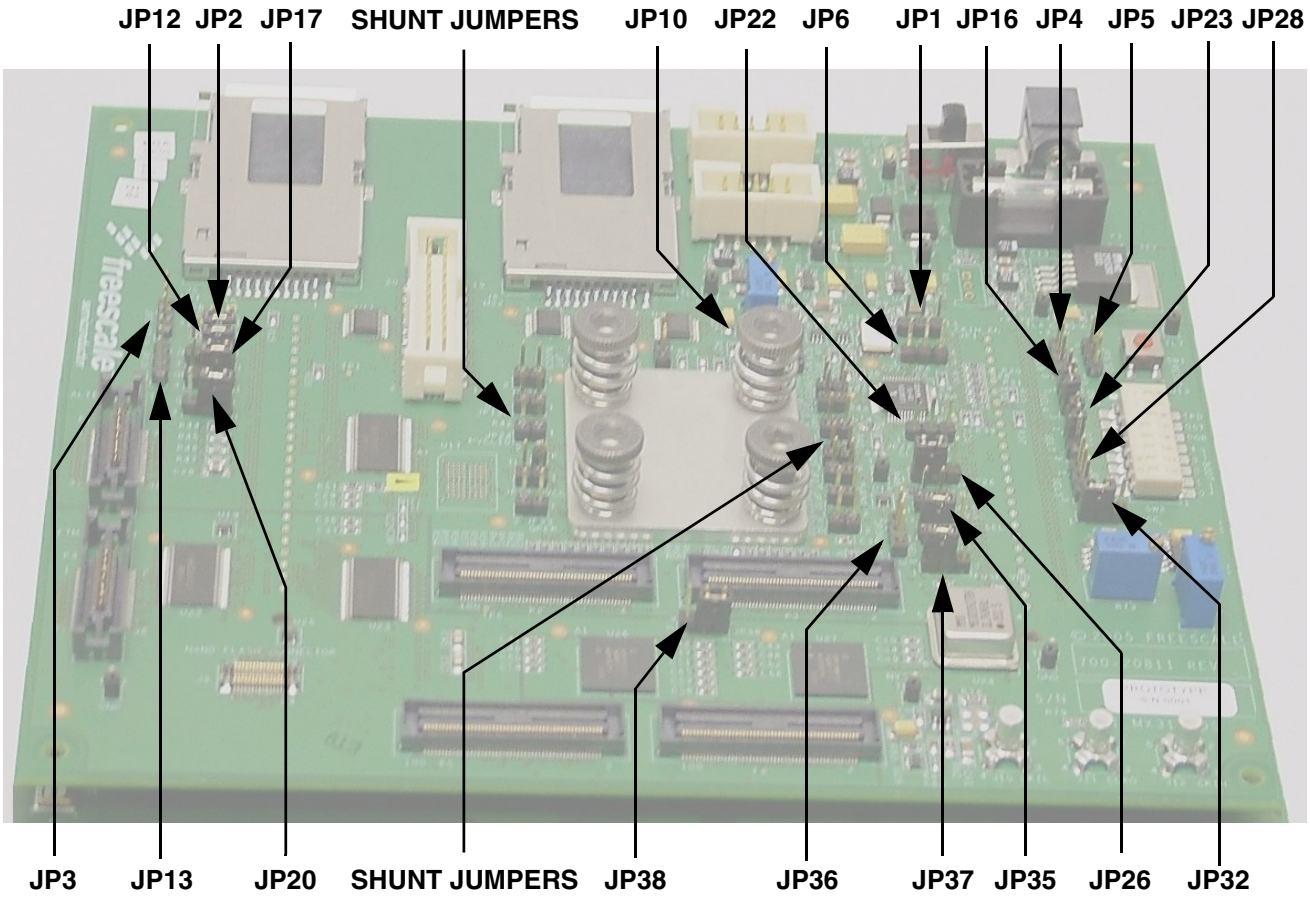


Figure 2-5. CPU Board Connectors

2.4MC13783 Board Configuration

2.4.1MC13783 Board Switches

The MC13783 board has three user-definable push button switches (S1, S2, and S3), and six DIP switches. SW4 controls USB port functions. SW5 switch settings determine the source of back-up power. SW6 settings control the on-board USB port. SW7 settings control the on-board buffers. SW8 settings control board clocks. SW9 settings control power-up voltage levels. Figure 2-6 shows the locations of the MC13783 board switches.

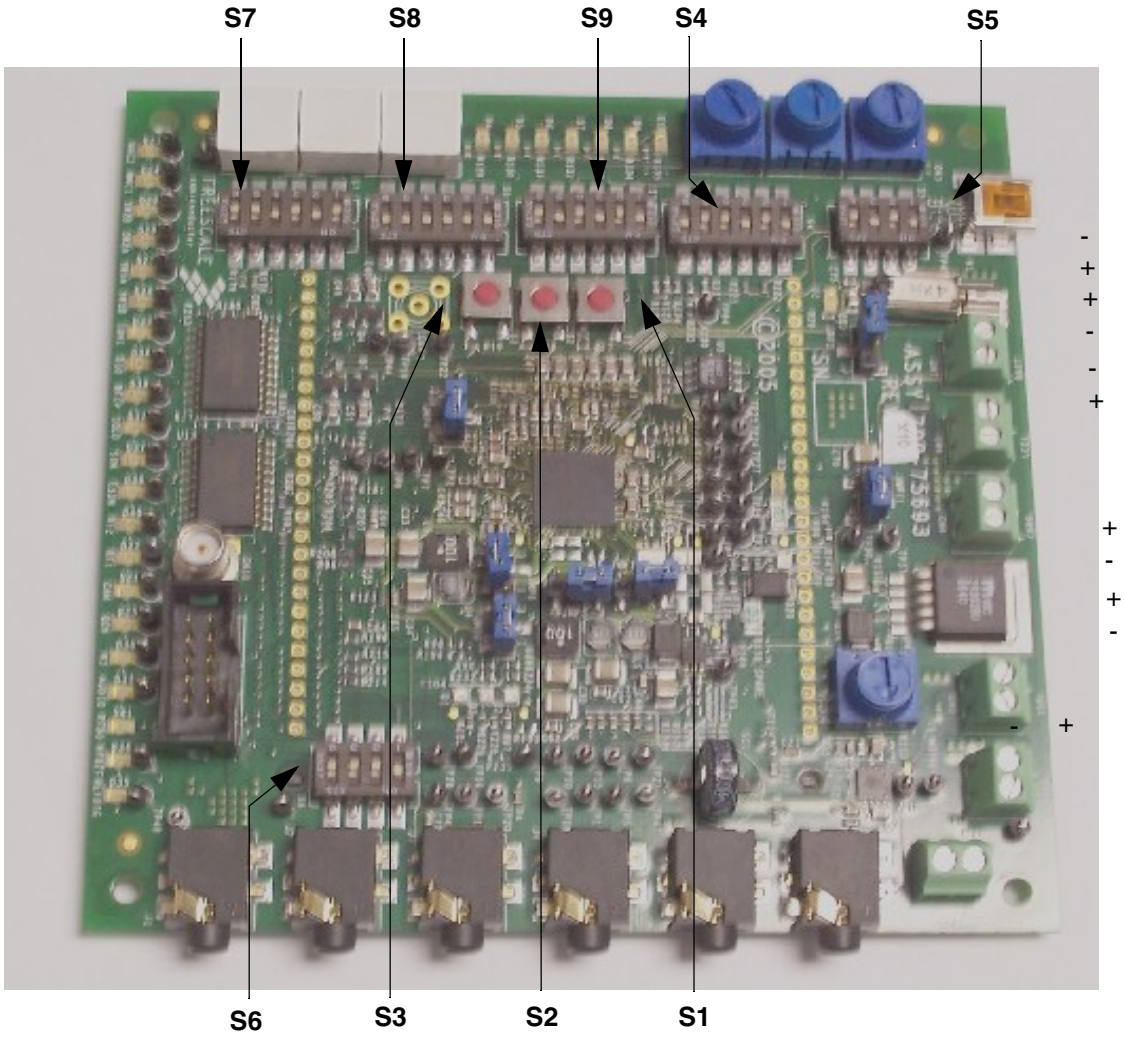


Figure 2-6. MC13783 Board Switches

2.4.1.1 S1, S2, S3 – User Defined Push Buttons

The three push button switches are connected to the ON1B, ON2B, and ON3B inputs of the MC13783 and the signals are also routed to the Base board connector. The lines are pulled up on the board. Pushing a switch grounds the line.

2.4.1.2 S4 – USB Function Select, USB Enable, WDI Enable Switches

The first four SPST slide switches in S4 control USB port function. Table 2-7 shows valid switch combinations (other combinations must not be used).

Table 2-7. MC13783 Board S4 USB Mode Select

S4-1	S4-2	S4-3	S4-4	USB Mode Selected
OFF	OFF	ON	OFF	Differential, unidirectional (6 wire)
ON	OFF	OFF	ON	Differential, bidirectional (4 wire)
OFF	ON	OFF	ON	Single ended, unidirectional (6 wire)
OFF	OFF	OFF	ON	Single ended, bidirectional (4 wire)

S4-5 ON enable MC13783' USB OTG transceiver, OFF disables it.

S4-6 ON pulls up the WDI input to MC13783 disabling that function. MC13783 will not shut down due to a WDI time-out. OFF the WDI input of MC13783 must be pulsed periodically.

Note: SW2-1 on the Base board also affects the WDI signal.

2.4.1.3 S5 – Backup Source Select Switch

The four SPST slide switches in S5 control MC13783 back-up power. Table 2-8 shows valid switch combinations (other combinations must not be used). The Super Cap back up source is on the board. Set S5-1 and S5-3 to ON to charge the Super Cap. R150 controls peak charge and R108 controls charge rate. Set S5-3 to OFF when charging is complete. Set S5-4 to ON to allow the Super Cap to discharge. The rate of discharge is controlled by R26. Connection to an external lithium cell is optional. If a lithium cell is used, it must be connected to CN9 and S5-2 must be set to ON. Otherwise S5-2 must be OFF.

Table 2-8. MC13783 Board S5 Backup Source Select

S5-1	S5-2	S5-3	S5-4	Function
ON	OFF	ON	OFF	Charge SC1
ON	OFF	OFF	OFF	Hold charge
ON	OFF	OFF	ON	Discharge SC1
OFF	ON	OFF	OFF	External Li Cell (CN9)

2.4.1.4 S6 – USB Buffer Control Switch

Two of the four SPST slide switches in S6 control the MC13783 USB interface buffers. Table 2-9 shows the valid switch combinations.

CAUTION

To avoid damage to the ADS, use only the valid switch settings.

Table 2-9. MC13783 Board SW6 USB UDATVP and USBOVM Direction Select

S6-1	S6-2	S6-3	S6-4	Function
OFF	OFF	X	X	DO NOT USE
OFF	ON	X	X	Buffer drives from MC13783 to ADS
ON	OFF	X	X	UTXENB controls buffer direction

Table 2-9. MC13783 Board SW6 USB UDATVP and USBOVM Direction Select

ON	ON	X	X	DO NOT USE

2.4.1.5 S7 – Audio Buffer Enable and Direction Select Switch

Pairs of the six SPST slide switches in S7 enable the on-board audio buffers and determine the direction of data. Table 2-10 shows the valid switch combinations.

CAUTION

To avoid damage to the ADS, use only the valid switch settings.

Table 2-10. MC13783 Board SW7 Buffer Enable and Direction Select

S7-1	S7-2	S7-3	S7-4	S7-5	S7-6	Function
ON	OFF					GPO1_BUFF controls FS1 and BCL1 buffer direction
OFF	ON					FS1 and BCL1 buffers drive from MC13783 to ADS
OFF	OFF					FS1 and BCL1 buffers drive from ADS to MC13783
ON	ON					DO NOT USE
		ON	OFF			GPO2_BUFF controls TX2, FS2, and BCL2 buffer direction
		OFF	ON			FS2, and BCL2 buffers drive from MC13783 to ADS
		OFF	OFF			FS2, and BCL2 buffers drive from ADS to MC13783
		ON	ON			DO NOT USE
				ON	X	TX2, FS2 and BCL2 buffers enabled
				OFF	X	TX2, FS2 and BCL2 buffers disabled
				X	ON	TX1, FS1 and BCL1 buffers enabled
				X	OFF	TX1, FS1 and BCL1 buffers disabled

2.4.1.6 S8 – CLIA and CLIB Source Select Switch

The six SPST slide switches in S8 control the source of the CLIA and CLIB audio bus clock inputs of the MC13738. Table 2-11 shows the switch functions.

CAUTION

Be careful not to enable more than one source for either CLIA or CLIB.

Table 2-11. MC13783 Board SW8 CLIA and CLIB Source Select

S8-1	S8-2	S8-3	S8-4	S8-5	S8-6	Function
ON	X	X	X	X	X	CLIA from J6 goes to CLIA of MC13783
X	ON	X	X	X	X	CLIA from J6 goes to CLIB of MC13783
X	X	ON	X	X	X	CLIB from J6 goes to CLIA of MC13783
X	X	X	ON	X	X	CLIB from J6 goes to CLIB of MC13783
X	X	X	X	ON	X	CN10 goes to CLIA
X	X	X	X	X	ON	CN10 goes to CLIB

2.4.1.7 S9 – MC13783 Power-up Mode Select Switch

The six SPST slide switches in S9 control the logic levels of the MC13783 PUMS[3:1] inputs during power-up, which determine operating power levels and start sequencing. The switches operate in pairs. Setting the low-number switch to ON grounds the input; setting the high-number switch to ON pulls the input up. When both switches are set to OFF, the input floats.

CAUTION

Setting both switches in a pair to ON also grounds the associated input, but uses significant VATLAS current. Do not use this setting.

Table 2-12 shows S9 switch functions. For information about the effect of the PUMS inputs and operating modes, see the MC13783 manual on the ADS CD.

Table 2-12. MC13783 Board SW9 MC13783 Power-up Mode Select

S9-1	S9-2	S9-3	S9-4	S9-5	S9-6	Function
OFF	OFF					PUMS1 floats (selects power-up voltage levels)
ON	OFF					PUMS1 grounded (selects power-up voltage levels)
OFF	ON					PUMS1 pulled up (selects power-up voltage levels)
ON	ON					DO NOT USE
		OFF	OFF			PUMS2 floats (selects power-up voltage levels)
		ON	OFF			PUMS2 grounded (selects power-up voltage levels)
		OFF	ON			PUMS2 pulled up (selects power-up voltage levels)
		ON	ON			DO NOT USE
				OFF	OFF	PUMS3 floats (selects power-up sequence)
				ON	OFF	PUMS3 grounded (selects power-up sequence)
				OFF	ON	PUMS3 pulled up (selects power-up sequence)
				ON	ON	DO NOT USE

2.4.2MC13783 Board Jumper Headers

The MC13783 board has seven jumper headers. JMP1, JMP3, JMP9, and JMP10 are not implemented. JMP2 selects use of a vibratory or light (LED) alarm. JMP4 selects the source of the TXIN signal. JMP5 to JMP8 control whether the outputs of the switching supplies on the MC13783 are connected in parallel. JMP11 selects a power source for the MC13783 chip. Table 2-13 shows Jumper functions. Figure 2-7 shows the jumper locations.

CAUTION

The settings of SW1 A/B control jumpers JMP5 and JMP7 must be the same.
The settings of SW2 A/B control jumpers JMP6 and JMP8 must be the same.

Table 2-13. MC13783 Board Jumper Headers

Jumper Designation	Pin Connection	Effect
JMP2 Alarm Select	1-2	Vibrator
	2-3	LED

Table 2-13. MC13783 Board Jumper Headers (continued)

Jumper Designation	Pin Connection	Effect
JMP4 TXIN Select	1-2	TXOUT
	2-3	J7
JMP5 SW1 A/B Supply Combination	1-2	SW1A and SW1B operate independently
	2-3	Combine SW1A and SW1B output
JMP6 SW2 A/B Supply Combination	1-2	SW2A and SW2B operate independently
	2-3	Combine SW2A and SW2B output
JMP7 SW1 A/B Supply Combination	1-2	SW1A and SW1B operate independently
	2-3	Combine SW1A and SW1B output
JMP8 SW2 A/B Supply Combination	1-2	SW2A and SW2B operate independently
	2-3	Combine SW2A and SW2B output
JMP11 Power Source Select	1-2	On-board regulator (U4)
	2-3	External power (CN7)

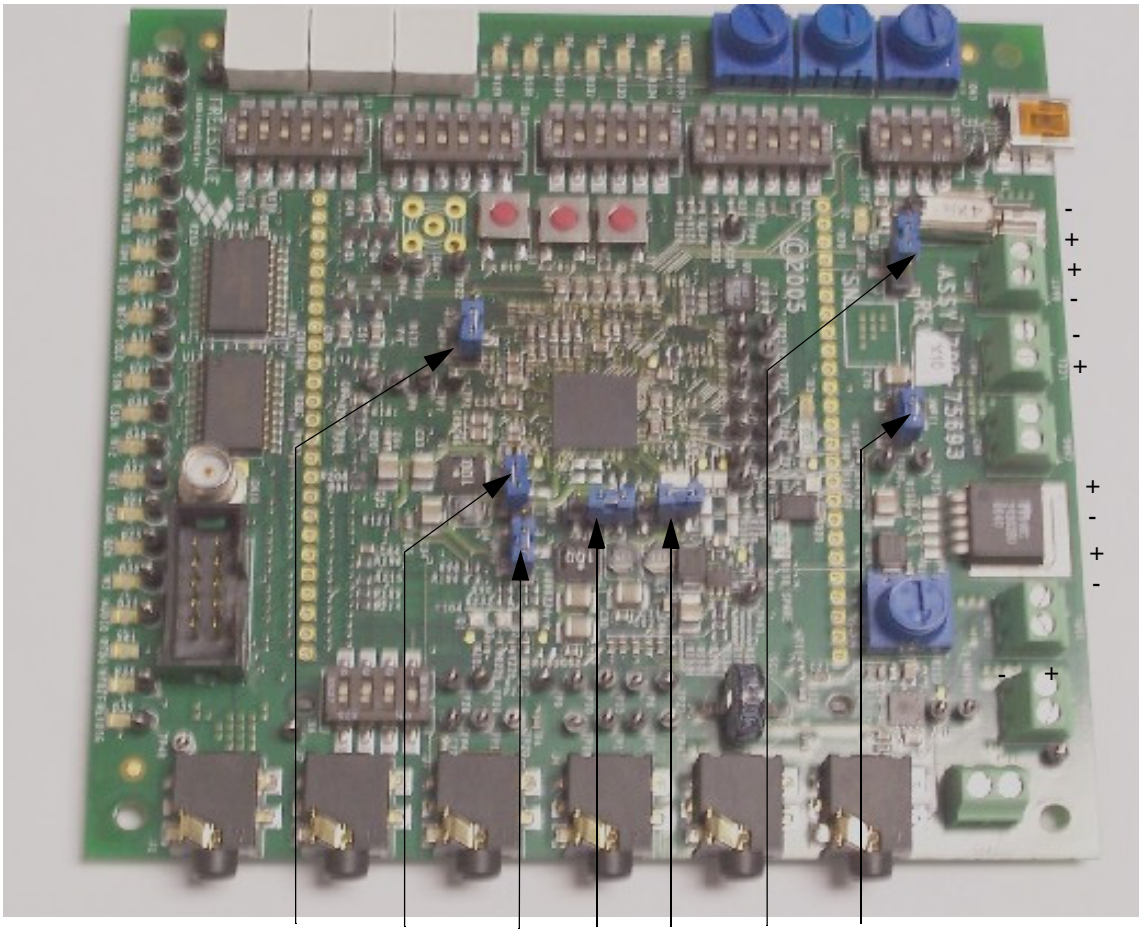


Figure 2-7. MC13783 Board Jumper Headers

2.5 ADS Set-up

2.5.1 CPU Board Regulator Power Configuration

CAUTION

Use this procedure to select NVCC power from on-board regulators only when the CPU board is operated without the MC13783 board. Configuring the power jumpers incorrectly can damage the ADS. See paragraph 2.3.2 for more information about power jumper settings. To use the CPU board with MC13783 power management, refer to paragraph 2.5.2.

1. Remove MC13783 Card if it is placed
2. If installed remove the following Baseboard jumpers J15, JP16, JP17, J18, JP19, J20, J21, J22, J23, J24, JP25 and J26. Use these jumpers in step 3.
3. Configure jumpers JP4, JP5, JP13, JP16, JP23, JP28, and JP36 for the desired voltage levels.

NOTE

The jumpers are perpendicular to the other three-pin jumpers on the board.

4. Proceed to paragraph 2.5.3.

2.5.2MC13783 Power Configuration

CAUTION

Use this procedure to select NVCC power only when the CPU board is operated with the MC13783 board. Configuring the power jumpers incorrectly can damage the ADS. See paragraph 2.2.2 for more information about power jumper settings. To use the CPU board without MC13783 power management, refer to paragraph 2.5.1.

1. Remove jumpers JP4, JP5, JP13, JP16, JP23, JP28, and JP36 from the CPU board.

NOTE

The jumpers are perpendicular to the other three-pin jumpers on the board.

2. Install the jumpers from 1 on Baseboard jumpers J15, J18, J20, J21, J22, J23, J24, and J25.

2.5.3 Select QVCC and PLL Voltages

CAUTION

The CPU board regulators can be used with or without the MC13783 board, but all the jumpers must be configured the same way.

3. Jumper pins 1 and 2 of JP12 (QARM), JP17 (QPER), JP20 (QL2), JP32 (XVCC), and JP35 (FVCC SEL) to select the regulators on the CPU board (see paragraph 2.3.2).
4. Jumper pins 2 and 3 of JP12 (QARM), JP17 (QPER), JP20 (QL2), JP32 (XVCC), and JP35 (FVCC SEL) to select the voltage sources on the MC13783 board (see paragraph 2.3.2).

2.5.4 Select CPU Clock Source

1. Use JP22 to select which clock to enable (26 MHz CKIH or 32 kHz CKIL).
2. Use either JP1 or JP26 select the source for that clock.

2.5.5 Set Other CPU Board Jumpers

1. Configure JP37, Fuse Pin Voltage (FUSE_VDD) (see paragraph 2.3.2)
2. Configure JP6, Base Board LA DATA Enable
3. Configure JP2, Reset Configuration
4. Configure JP38, DRAM Power (VDD SEL)
5. Configure JP31, SVCC
6. Configure JP10, JTAG Mode (SJC_MOD)

2.5.6 Set CPU Board Switches

1. Set Boot Mode Switches, SW2-1 through SW2-5
2. Set Push Button Reset Connection Switches, SW2-6 and SW2-7
3. Set POR RESET, SW2-6
4. Set RESET OUT, SW2-7
5. Set Tamper Detect, SW2-8
6. When using the CPU board in standalone mode, proceed to paragraph 2.5.12.

2.5.7 Set Base Board Jumpers

1. Configure JP1, HS OTG VUSB Source
2. Configure JP2, HS HOST VUSB Source
3. Configure JP3, SERIAL LCD CS
4. Configure JP4 SD1 POWER
5. Configure JP5, SD2 POWER
6. Configure JP6 and JP7, I2C connection – FS OTG PHY
7. Configure JP8, NVRAM – Ethernet PHY Enable
8. Configure JP12, Keypad LIGHT SENSE
9. Configure JP14, 1WIRE Enable

2.5.8 Set Base Board Switches

1. Set SW1 – UART EN Switches
2. Set SW2- RS-232 MBAUD, Shut Down, WDI, and Buzzer Enable Switches
3. Set SW3 – User Defined Switches

2.5.9 Connect the CPU Board to the Base Board

1. Place the Base board on a flat work surface.
2. Install the CPU board as shown in Figure 2-8 (the connectors are keyed so the CPU board cannot be connected incorrectly).

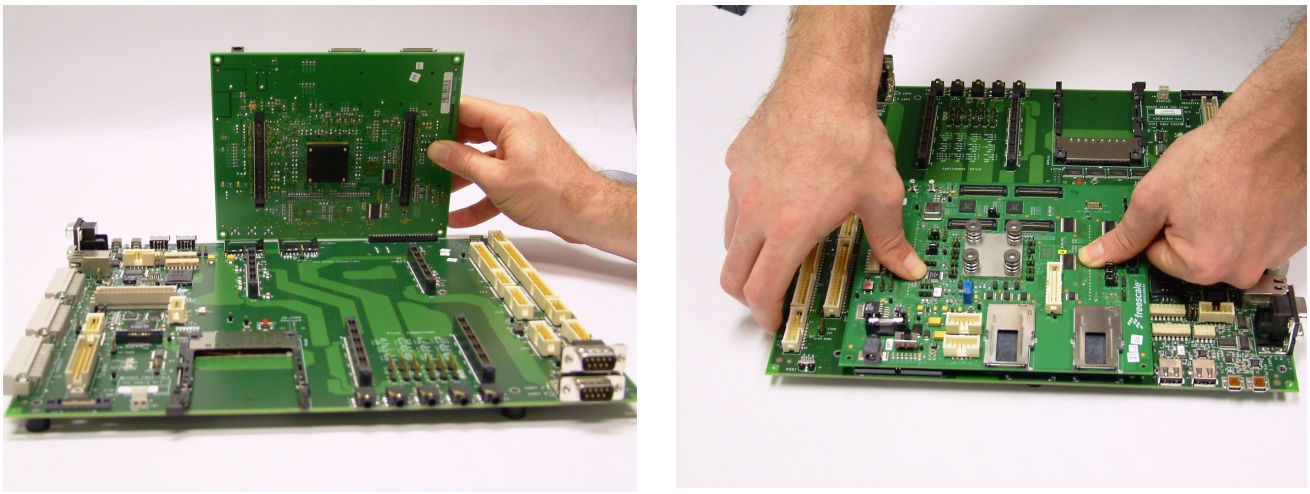


Figure 2-8. Connecting the CPU Board to the Base Board

2.5.10 Configure the MC13783 Board

If you are not using the MC13783 board, proceed to paragraph 2.5.12. See paragraph 2.4 for information about MC13783 board jumpers and switches.

1. Set JMP2, Vibrator/LED Select.
2. Set JMP4, TXIN Select.
3. Set JMP5, SW1A/B Combination (setting must match JMP7).
4. Set JMP6, SW2A/B Combination (setting must match JMP8).
5. Set JMP7, SW1A/B Combination (setting must match JMP5).
6. Set JMP8, SW2A/B Combination (setting must match JMP6).
7. Set JMP11, Power Select (typically set for operation from on-board regulator U4)
8. Set USB Mode Selection Switches S4-1 to S4-4.
9. Set Backup Source Selection Switches S5-1 to S5-4 (typically S5-1 ON, S5-2 OFF, S5-3 ON, S5-4 OFF).
10. Set USB Buffer Direction Selection Switches S6-1 to S6-2 (typically S6-1 ON, S6-2 OFF).
11. Set Buffer Enable and Direction Selection Switches S7-1 to S7-6 (typically S7-1 OFF, S7-2 ON, S7-3 OFF, S7-4 ON, S7-5 OFF, S7-6 OFF).
12. Set CLIA, CLIB Source Selection Switches S8-1 to S8-6 (typically S8-1 ON, S8-4 ON, all others OFF).
13. Set Power Up Mode Selection Switches S9-1 to S9-6 (typically S9-1 ON, S9-2 OFF, S9-3 ON, S9-4 OFF, S9-5 ON, S9-6 OFF).

2.5.11 Connect the MC13783 Board to the Base Board

1. Make sure the power jumpers on the Base board are correctly configured.
2. Install the MC13783 board as shown in Figure 2-9 (the connection is keyed so that it cannot be connected incorrectly).

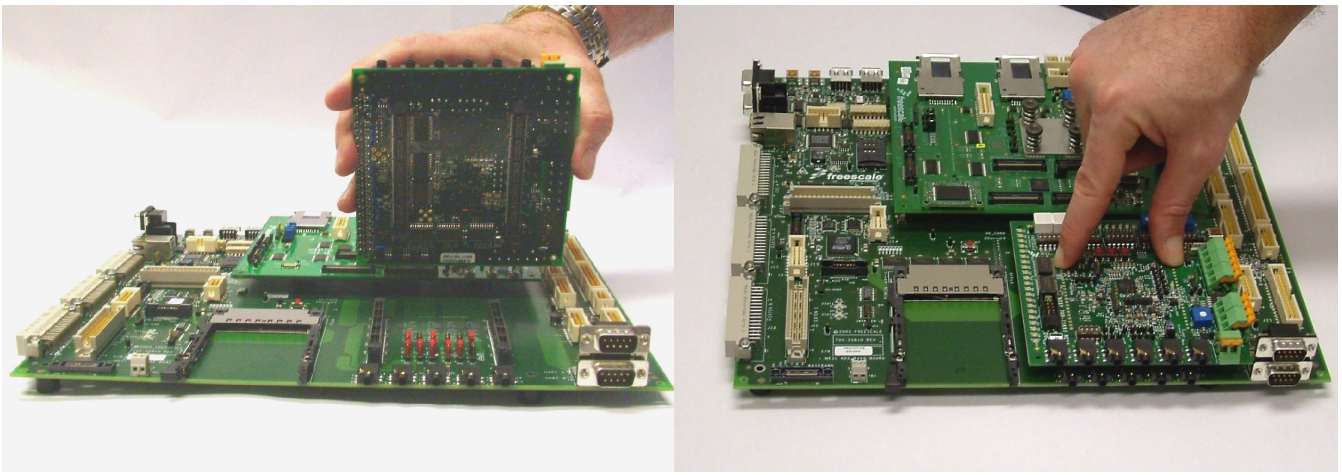


Figure 2-9. Connecting the MC13783 Board to the Base Board

2.5.12 Connect Power to the CPU Board

1. Connect the female end of the A/C cable to the power supply module.
2. Attach any necessary power adaptor plugs to power supply module plug it into an A/C outlet.
3. Connect the barrel connector into J3 on the CPU board.

2.5.13 Turn System Power On

1. On the CPU board, slide S1 to the ON position.
2. D1 illuminates, indicating that external power is applied.

Chapter 3 ADS Operation

This chapter describes how the ADS functions.

3.1 Functional Block Diagram

Figure 3-1 shows the functional blocks of the ADS in their approixmate locations in the system.

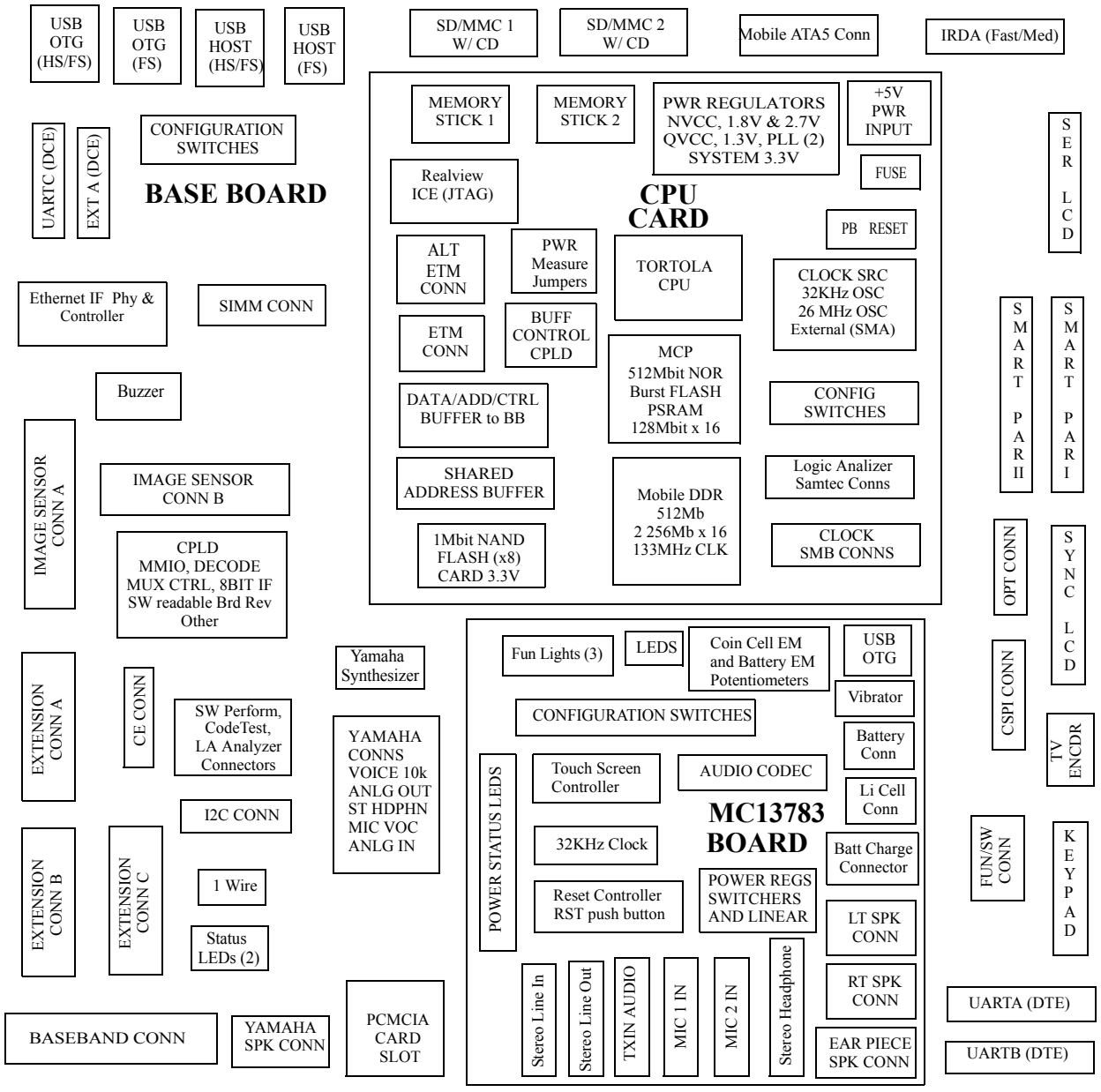


Figure 3-1. ADS Functional Block Diagram

3.2 ADS Memory Map

Table 3-1 shows the memory map for the ADS. None of the memories take up the entire address space of the associated chip selects, software can access the same physical memory location at more than one range of addresses. For instance, DDR SDRAM occupies only 128MB of the 256MB space available to $\overline{\text{CSD0}}$, so it appears in two different ranges of addresses.

Table 3-1. ADS Memory Map

Peripheral	Chip Select	Address Range (HEX)	Actual Memory Size
DDR SDRAM	$\overline{\text{CSD0}}$ ($\overline{\text{CS2}}$)	0x8000_0000 to 0x8FFF_FFFF	128M BYTES
Burst FLASH	$\overline{\text{CS0}}$	0xA000_0000 to 0xA7FF_FFFF	32M BYTES
PSRAM	$\overline{\text{CS5}}$	0xB60_0000 to 0xB7FF_FFFF	16M BYTES
Ethernet Controller	$\overline{\text{CS4}}$	0xB402_0000 to 0xB402_FFFF*	64K BYTES
External DUART	$\overline{\text{CS4}}$	0xB401_0000 to 0xB401_001F*	32 BYTES
YMU782B synth	$\overline{\text{CS4}}$	0xB403_0000 to 0xB403_0001*	2 BYTES
CPLD & MMIO	$\overline{\text{CS4}}$	0xB400_0000 to 0xB400_00IC	58 BYTES
* For I/O operations only D[15:0] are used			

3.3 Peripheral Bus Control CPLD

The ADS requires glue logic for peripheral bus address decoding, board control and status signals, board revision registers, and other functions. This glue logic is implemented with a CPLD. The following paragraphs describe the CPLD.

3.3.1 Features

The key features provided by the CPLD include:

- A16-bit slave interface to the CPU data bus
- Address decode and control for the Ethernet controller
- Address decode and control for the external UART controller
- Address decode for the audio synthesizer
- Control and status registers for various board functions
- Control and multiplexing for a variety of interrupt sources

3.3.2 CPU Interface

The interface connects the i.MX31 through the CPLD to peripherals with asynchronous and synchronous protocols. The signal involved with this are listed in Table 3-2. The CPU provides several chip-select signals that can be configured for different memory types. The CPLD uses chip-select signal CS4, with the following requirements:

- CS4 must occupy a 32 Mbyte window in the address space
- CS4 must be configured for 16-bit bus width, asynchronous transfers
- CS4 assertion window must be at least 150 ns
- Byte enables must be asserted at CS4 assertion time
- Byte enables must be negated at least 1/2 clock before CS4 negation during write cycles
- Multiplexed transfers and synchronous transfers are not supported

Table 3-2. CPU Signal Interface

Signal	Direction	Description
A[25:0]	In	Address bus (not all address lines are used)
D[15:0]	In/Out	Data bus
CS4_B	In	Chip select 4 used for peripheral access
BE0_B	In	Byte Enable 0, which corresponds with D[7:0]
BE1_B	In	Byte Enable 1, which corresponds with D[15:8]
OE_B	In	Output Enable
RW_B	In	Read/write signal
RSTIN_B	In	Reset signal
DMAREQ	Out	DMA Request to CPU

3.3.3 Peripheral Interface

The CPLD's peripheral interface provides address decode and control for the CS8900A Ethernet controller, the SC16C652 DUART, and the YMU782B audio synthesizer.The signals involved with this activity are listed in Table 3-3.

Table 3-3. Peripheral Interface Signals

Signal	DIR	Description
PBA[2:0]	Out	Peripheral Bus Address
PBD[7:0]	In/Out	Peripheral Bus Data, used for DUART, board version, switches
IOR_B	Out	I/O Read is asserted during I/O read transfers and DMA transfers
IOW_B	Out	I/O Write is asserted during I/O write transfers
MEMR_B	Out	Memory read to Ethernet controller is asserted during memory read transfers.
MEMW_B	Out	Memory write to Ethernet controller is asserted during memory write transfers.
AEN	Out	DMA Address enable, asserted during Ethernet controller DMA transfers
ENET_DMAREQ	In	DMA request from Ethernet controller
ENET_DMACK_B	Out	DMA acknowledge to Ethernet controller
ENET_CS_B	Out	Ethernet chip select
UA_CS_B	Out	UART A chip select
UB_CS_B	Out	UART B chip select
SYNTH_CS	Out	Synthesizer chip select

3.3.3.1 Peripheral Bus Cycles

The following peripheral bus cycles are implemented.

Table 3-4. Bus Cycles

Cycle	Transfer size	Description
IOREAD	Byte, Word	Used to read 8/16-bit data from peripheral registers with IOR_B signal.
IOWRITE	Byte, Word	Used to write 8/16-bit data to peripheral registers with IOW_B signal.
MEMREAD	Byte, Word	Used to read 8/16-bit data from peripheral memory using MEMR_B signal.
MEMWRITE	Byte, Word	Used to write 8/16-bit data to peripheral memory using MEMW_B signal.
DMAREAD	Word	Used during Ethernet DMA transfers to read 16-bit data from Ethernet controller memory buffer using ENET_DMACK_B signal.

3.3.3.2 DMA Operation

The CS8900A supports DMA slave transfers for received data frames. The CPLD supports these DMA transfers using a single DMAREQ signal to the processor and a special DMA address space in the memory map. The ENET_DMAREQ signal from the CS8900A is forwarded to the CPU I/F and used as a qualifier for DMA transfers. A qualified read transfer to the DMA address space generates the ENET_DMACK_B signal to the CS8900A.

3.3.3.3 SC16C652C UART Decode

The CPLD provides address decodes and data path control for the SC16C652C DUART. Data is transferred through the CPLD to and from the SC16C652C. The CPLD hardware provides byte steering logic to transfer the correct byte to the SC16C652C during data transfers.

3.3.3.4 SCS8900A Ethernet Decode

The CPLD provides address decode and control for the CS8900A Ethernet controller. Both 16-bit I/O mode and memory mode are supported. Memory mode operation allows direct access to the CS8900A internal registers and frame buffer. A single DMA request line is provided for DMA transfers from the CS8900A buffer to system memory for increased performance.

Accesses to the CS8900A must satisfy the following requirements.

- Provide a transition of the SBHE input after reset. This is done with a dummy byte read to an odd location, as for example a byte read to $B400_0007.
- All reads and writes to the CS8900A must be 16-bits.
- For memory mode operation, the base address register must be set to $1000. This is a 20-bit register, and the upper 4 bits must be 0.

3.3.3.5 YMU782B Audio Synthesizer Decode

The CPLD provides address decode and data path control for the YMU782B audio synthesizer. Data is transferred through the CPLD to and from the YMU782B. The CPLD provides byte steering logic to transfer the correct byte to the YMU782B during data transfers. All reads and writes to the YMU782B must be eight bits.

3.3.4 UART Multiplexing

UARTC has one DTR line from the UART transceiver. This line is muxed to either MCU UART1 or UART2. The muxing is determined by the UARTC_SEL field in the BCTRL2 register.

3.3.5 CPLD Memory Map

Table 3-5. CPLD Memory Map

Name	Description	Address
VERSION	Version Register	B400_0000
BSTAT2	Board Status Register 2	B400_0002
BCTRL1	Board Control Register 1 set address	B400_0004
	Board Control Register 1 clear address	B400_0006
BCTRL2	Board Control Register 2 set address	B400_0008
	Board Control Register 2 clear address	B400_000A
BCTRL3	Board Control Register 3 set address	B400_000C
	Board Control Register 3 clear address	B400_000E
BCTRL4	Board Control Register 4 set address	B400_0010
	Board Control Register 4 clear address	B400_0012
BSTAT1	Board Status Register 1	B400_0014
ISR	Interrupt Status Register	B400_0016
ICSR	Interrupt Current Status Register	B400_0018
IMR	Interrupt Mask Register set address	B400_001A
	Interrupt Mask Register clear address	B400_001C
SC16C652	External UART Port A	B401_0000
	External UART Port B	B401_0010
CS8900A	Ethernet controller I/O base address	B402_0000
	Ethernet controller Memory base address	B402_1000
	Ethernet controller DMA base address	B402_2000
YMU782B	Audio synthesizer port	B403_0000

3.3.6 Register Descriptions

The CPLD has general control registers and interrupt control registers. The number of ADS interrupt sources is larger than the number of MCU GPIO pins. All ADS interrupts are routed through the CPLD where some of them are grouped. An Interrupt Mask Register can disable each interrupt source.

3.3.6.1 Version Register

The version register has three fields that show the version of the CPLD, the CPU board, and the Base board. The CPLD version is an 8-bit programmed field that is changed when the CPLD design changes. The CPU and BASE fields are implemented as two 4-bit fields and configured with external input signals connected to pull up and pull down resistors. They represent the revision of the PCB which changes by letter revs, marked in etch on the back side of the PCB. The first revision is A and the revision code will read back 0000b. The next revision, B, will read back 0001b and so on. The CPU and BASE fields are muxed on the peripheral data bus.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	PBC								CPU				BASE			
OPER	R								R				R			

Figure 3-2. Version Register

3.3.6.2 Board Status Register 1 (BSTAT1)

BSTAT1 contains several bits that represent the board status from different places on the board. These registers are read only.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	ATLAS_ IN	PTT	FLIP_ SENSE2	FLIP_ SENSE1	SD2_ WP	SD1_ WP	PWR_ RDY	ATA_ DASP	ATA_ CBLID	ATA_ IOCS16	LIGHT_ SENSE	KP_ ON	NF_ DET
OPER	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
RESET	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-
IN/OUT	-	-	-	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN

Figure 3-3. Board Status Register 1 (BSTAT1)

3.3.6.3 Board Status Register 2 (BSTAT2)

Table 3-6. Board Status Register 1 Bit Definitions

Name	Description	Settings
NF_DET Bit 0	**NAND Flash Detect —** indicates Nand Flash card insertion.	0 = Nand Flash card is inserted 1 = Nand Flash card is not inserted
KP_ON Bit 1	**Keypad On/Off —** indicates if keypad is on/off	0 = Keypad is ON 1 = Keypad is OFF
LIGHT_SENSE Bit 2	**Light sense —** This signal reflects the light sense output from the keypad	0 = Light sense is 0 1 = Light sense is 1
ATA_IOCS16 Bit 3	**ATA IOCS16 —** This bit reflects the status of pin IOCS16 on the ATA connector	0 – IOCS16 state is 0 1 – IOCS16 state is 1
ATA_CBLID Bit 4	**ATA CBLID —** This bit reflects the status of pin CBLID on the ATA connector	0 = CBLID state is 0 1 = CBLID state is 1
ATA_DASP Bit 5	**ATA DASP —** This bit reflects the status of pin DASP on the ATA connector	0 = DASP state is 0 1 = DASP state is 1
PWR_RDY Bit 6	**Power Ready—** Power ready indication from MC13783 board.	0 = MC13783 power is not ready 1 = MC13783 power is ready
SD1_WP Bit 7	**SD1 Write Protect —**This bit reflects the Write Protect on SD1 card.	0 = SD1 card is Write Protected 1 = SD1 card is not Write Protected
SD2_WP Bit 8	**SD2 Write Protect —**This bit reflects the Write Protect on SD2 card.	0 = SD2 card is Write Protected 1 = SD2 card is not Write Protected
FLIP_SENSE1 Bit 9	**Flip Sense 1 —** This bit reflects the status of pin Flip_Sense1 on the keypad connector	0 = Flip Sense 1 on keypad is 0. 1 = Flip Sense 1 on keypad is 1.
FLIP_SENSE2 Bit 10	**Flip Sense 2 —** This bit reflects the status of pin Flip_Sense2 on the keypad connector	0 = Flip Sense 2 on keypad is 0. 1 = Flip Sense 2 on keypad is 1.
PTT Bit 11	**PTT button —** This bit reflects the status of pin PTT on the keypad connector	0 = PTT signal on keypad is 0. 1 = PTT signal on keypad is 1.
ATLAS_IN Bit 12	**ATLAS IN —** This bit indicates if the power management board (MC13783) is placed on the board.	0 = MC13783 board is placed 1 = MC13783 board is not placed
RSV Bits 13:15	Reserved for future use	Always reads 0

BSTAT2 contains several bits that represent the board status from different places on the board. These registers are read only.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DMA_REQ	DSW							
OPER	R	R	R	R	R	R	R	R	R							

Figure 3-4. Board Status Register 2 (BSTAT2)

Table 3-7. Board Status Register 1 Bit Definitions

Name	Description	Settings
DSW Bits 7:0	Debug switch—This 8-bit field contains the value of the debug DIP switch.	0 (each bit) = switch is closed 1 (each bit) = switch is open
DMA_REQ Bit 8	DMA Request – this bit reflects the DMA request to CPU from the Ethernet controller	0 = DMA Request is low 1 = DMA Request is high
RSV Bits 9:15	Reserved—These bits are reserved for future use.	Always read as 0

3.3.6.4 Board Control Register 1 (BCTRL1)

BCTRL1 contains several fields to control various board functions. This register is implemented as a set register and a clear register. To set a bit, write a 1 to the bit at the set address. To clear a bit, write a 1 to the bit at the clear address.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	LCDON	BEND	CCTL2			CCTL1			LED1_B	LED0_B	IRDA_EN_B	UCE_EN_B	UB_EN_B	UA_EN_B	XUART_RST	ENET_RST
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
IN/OUT	OUT/OD	-	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT

Figure 3-5. Board Control Register 1 (BCTRL1)

Table 3-8. Board Control Register 1 Bit Definitions

Name	Description	Settings
ENET_RST Bit 0	**Ethernet Reset —** Reset the Ethernet controller. This bit must be set for the desired duration of the reset signal, then cleared to remove the reset signal.	0 = Ethernet controller reset signal negated. 1 = Ethernet controller reset signal asserted.
XUART_RST Bit 1	**External UART Reset —** Reset external UART controller. This bit must be set for the desired duration of the reset signal, then cleared to remove the reset signal.	0 = UART controller reset signal negated. 1 = UART controller reset signal asserted.
UA_EN_B Bit 2	**UART A Enable —** Enable UART A transceiver.	0 = UART A transceiver enabled. 1 = UART A transceiver disabled
UB_EN_B Bit 3	**UART B Enable —** Enable UART B transceiver	0 = UART B transceiver enabled. 1 = UART B transceiver disabled
UCE_EN_B Bit 4	**UART C Enable —** Enable UART C transceiver.	0 = UART C transceiver enabled 1 = UART C transceiver disabled
IRDA_EN_B Bit 5	**IRDA Enable —** Used to enable the IRDA transmitter.	0 = IRDA transmitter enabled 1 = IRDA transmitter disabled
LED0_B Bit 6	**LED 0 on —** Used to turn LED 0 on. This is used as a general purpose status indicator.	0 = LED 0 is off 1 = LED 0 is on.
LED1_B Bit 7	**LED 1 on —** Used to turn LED 1 on. This is used as a general purpose status indicator.	0 = LED 1 is off. 1 = LED 1 is on.
CCTL1[2:0] Bits 8-10	**CSI1 Control —** CSI1 control provides a three bit field for control of user defined functions on the CSI connector	xxx = User defined function.
CCTL2[2:0] Bits 11-13	**CSI2 Control —** CSI2 control provides a three bit field for control of user defined functions on the CSI connector	xxx = User defined function.
BEND Bit 14	Internal register used as endian indicator	x = Internal function
LCDON Bit 15	**LCD ON —** Used to turn the QVGA dumb LCD display on.	0 = LCD is off 1 = LCD on

3.3.6.5 Board Control Register 2 (BCTRL2)

BCTRL2 contains several bits that control various board functions. This register is implemented as a set register and a clear register. To set a bit, write a 1 to the bit at the set address. To clear a bit, write a 1 to the bit at the clear address.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	VCC_EN	VPP_EN	CT_CS	LCDIO_EN	LCD_RST2	LCD_RST1	LCD_RST0	IRDA_MOD	ATA_SEL	ATA_EN	CSI_EN	UMODENC	UMODENA	USELC	USELB	USELA
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	1
IN/OUT	OUT	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT	OUT	OUT	OUT	OUT	OUT/OD	OUT/OD	OUT/OD

Figure 3-6. Board Control Register 2 (BCTRL2)

Table 3-9. Board Control Register 2 Bit Definitions

Name	Description	Settings
USELA Bit 0	**UART A SELECT —** Select UART A source on the CPU.	0 = the source is UART1 signals 1 = the source is UART5 signals
USELB Bit 1	**UART B SELECT —** Select UART B source on the CPU.	0 = the source is UART3 signals 1 = the source is UART4 signals
USELC Bit 2	**UART C SELECT —** Select UART C source on the CPU	0 = the source is UART2 signals 1 = the source is UART1 signals
UMODENA Bit 3	**UART A MODEM Enable —** Enable UART A MODEM signals.	0 = UART C MODEM signals enabled 1 = UART C MODEM signals disabled
UMODENC Bit 4	**UART C MODEM Enable —** Enable UART C MODEM signals	0 = UART C MODEM signals enabled 1 = UART C MODEM signals disabled
CSI_EN Bit 5	**CSI Enable —** Enable the CSI Interface.	0 = CSI enabled 1 = CSI disabled
ATA_EN Bit 6	**ATA_Enable —** Enable the ATA interface.	0 = ATA enabled 1 = ATA disabled
ATA_SEL Bit 7	**ATA Select —** Select CPU signals connected to the ATA interface.	0 = group A is connected to ATA interface 1 = group B is connected to ATA interface
IRDA_MOD Bit 8	**IRDA Mode —** Select IRDA Transceiver bandwidth	A transition from high to low while IRDA_TXD is low – SIR/MIR bandwidth A transition from high to low while IRDA_TXD is high – FIR bandwidth
LCDRST0 Bit 9	**LCD 0 Reset —** Reset the smart parallel LCD #1	0 = smart parallel LCD #1 reset signal negated 1 = smart parallel LCD #1 reset signal asserted
LCDRST1 Bit 10	**LCD 1 Reset —** Reset the smart parallel LCD #2	0 = smart parallel LCD #2 reset signal negated 1 = smart parallel LCD #2 reset signal asserted
LCDRST2 Bit 11	**LCD 2 Reset —** Reset the smart serial LCD	0 = smart serial LCD reset signal negated 1 = smart serial LCD reset signal asserted
LCDIO_EN Bit 12	**LCD GPIO Enable —** Enable GPIO1 and GPIO2 interface with the LCD connectors	0= connection with GPIO1 and GPIO2 is enabled 1= connection with GPIO1 and GPIO2 is disabled
CT_CS Bit 13	**Code Test Chip Select —** Select the Code Test emulator	0= Code Test selected 1= Code Test not Selected
VPPEN Bit 14	**VPP Enable —** Enable VPP power for the PCMCIA.	0= PCMCIA VPP power is off 1= PCMCIA VPP power is VCC power (3.3V)
VCCEN Bit 15	**VCC Enable —** Enable VCC power for the PCMCIA.	0= PCMCIA VCC power is off 1= PCMCIA VCC power is 3.3V

3.3.6.6 Board Control Register 3 (BCTRL3)

BCTRL3 contains several bits that control various board functions. This register is implemented as a set register and a clear register. To set a bit, write a 1 to the bit at the set address. To clear a bit, write a 1 to the bit at the clear address.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	SPI3_ RESET	VESIM_ EN	VSIM_ EN	SYNTH_ RST	CARD2_ SEL	CARD1_ SEL	FSH_ VBUS_ EN	OTG_ VBUS_ EN	OTG_ HS_ EN	FSH_ MOD	HSH_ EN	HSH_ SEL	FSH_ EN	FSH_ SEL	OTG_ FS_ EN	OTG_ FS_ SEL
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	1	0	0	1	1	1	0	1	0	1	0	1	1
IN/OUT	OUT	OUT/ OD	OUT/ OD	OUT	OUT	OUT	OUT/ OD	OUT/ OD	OUT/ OD	OUT	OUT	OUT	OUT	OUT	OUT	OUT

Figure 3-7. Board Control Register 3 (BCTRL3)

Table 3-10. Board Control Register 3 Bit Definitions

Name	Description	Setting
OTG_FS_SEL Bit 0	**USB OTG Full Speed Select—**Select source of the USB OTG Full speed interface.	0 = MC13783 board 1 = CPU
OTG_FS_EN Bit 1	**USB OTG Full Speed Enable —** Enable the USB OTG Full speed interface on the CPU	0 = OTG Full Speed Interface enabled 1 = OTG Full Speed Interface disabled
FSH_SEL Bit 2	**USB Full Speed Host Select —** Select source of the USB Full speed Host interface	0 = Group A on the CPU 1 = Group B on the CPU
FSH_EN Bit 3	**USB Full Speed Host Enable —** Enable the USB Full speed Host interface	0 = Full Speed Host Interface enabled 1 = Full Speed Host Interface disabled
HSH_SEL Bit 4	**USB High Speed Host Select —** Select The source of the USB High speed Host interface.	0 = Group A on the CPU 1 = Group B on the CPU
HSH_EN Bit 5	**USB High Speed Host Enable —** Enable the USB High speed Host interface.	0 = High Speed Host Interface enabled 1 = High Speed Host Interface disabled
FSH_MODE Bit 6	**USB Full Speed Host Mode —** Selects Single ended/ differential mode on USB Host Full Speed interface.	0 = Differential mode 1 = Single ended mode
OTG_HS_EN Bit 7	**USB OTG High Speed Enable —** Enable the USB OTG High speed interface on the CPU.	0 = OTG High Speed Interface enabled 1 = OTG High Speed Interface disabled
OTG_VBUS_EN Bit 8	**USB OTG VBUS Enable —** Enable VBUS regulator on USB OTG interface PHY.	0 = OTG VBUS regulator is enabled 1 = OTG VBUS regulator is disabled
FSH_ VBUS_EN Bit 9	**USB Full Speed Host VBUS Enable —** Enable USB Full speed Host interface PHY VBUS regulator	0 = Full Speed Host VBUS regulator is enabled 1 = Full Speed Host VBUS regulator is disabled
CARD1_SEL Bit 10	**Card1 Select —** Select MUX pin for SD1 / MS1 lines	0 = lines dedicated to SD1 interface 1 = lines dedicated to MS1 interface
CARD2_SEL Bit 11	**Card2 Select —** Select MUX pin for PCMCIA & SD2 / MS2 lines	0 = lines dedicated to PCMCIA &SD2 interface 1 = lines dedicated to MS2 interface
SYNTH_RST Bit 12	**Audio Synthesizer Reset —** Enable Audio Synthesizer reset signal	0= Reset audio Synthesizer 1= Normal operation
VSIM_EN Bit 13	**VSIM Enable —** Enable VSIM regulator on the MC13783 board.	0 = VSIM regulator is disabled 1 = VSIM regulator is enabled
VESIM_EN Bit 14	**VESIM Enable —** Enable VESIM regulator on the MC13783 board.	0 = VESIM regulator is disabled 1 = VESIM regulator is enabled
SPI3_RESET Bit 15	**CSPI3 Connector Reset —** Enable reset signal on CSPI3 connector	0 = CSPI3 is reset 1 = Normal operation

3.3.6.7 Board Control Register 4 (BCTRL4)

BCTRL4 contains several bits to control various board functions. This register is implemented as a set register and a clear register. To set a bit, write a 1 to the bit at the set address. To clear a bit, write a 1 to the bit at the clear address.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	PCMCIA_ EN	VIB_ EN	USER_ OFF	REGEN_ SEL	CSI_ MSB_EN
OPER	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
IN/OUT	-	-	-	-	-	-	-	-	-	-	-	OUT	OUT/ OD	OUT/ OD	OUT/ OD	OUT/ OD

Figure 3-8. Board Control Register 4 (BCTRL4)

Table 3-11. Board Control Register 4 Bit Definitions

Name	Description	Settings
CSI_MSB_EN Bit 4	**CSI MSB Enable —** Enable CSI_Data[3:0] from CSI interface	0 = CSI_Data[3:0] enabled 1 = CSI_Data[3:0] disabled
REGEN_SEL Bit 1	**Regulator Enable Select —** Select predefined programming for MC13783 regulators	0 = REGEN_SEL active 1 = REGEN_SEL not active
USER_OFF Bit 2	**User Off Indication —** Confirm user off mode after a power fail	0 = normal operation 1 = user off confirmation
VIB_EN Bit 3	**Vibrator Enable —** Enable the vibrator regulator on the MC13783 board	0 = Vibrator regulator disabled 1 = Vibrator regulator enabled
PCMCIA_EN Bit 4	**PCMCIA Enable —** Enable the PCMCIA buffer	0 = PCMCIA buffer enabled 1 = PCMCIA buffer disabled
RSV Bits 5:15	**Reserved —** For future use	Always reads 0

3.3.6.8 Interrupt Status/Clear Register (ISCR)

The ISCR reflects the status of each ADS interrupt source. The register may be read at any time.

There are two types of interrupt requests, level-triggered and edge-triggered.

Edge triggered interrupt requests are generated when the source signal changes active state. These interrupts are enabled by setting the associated control bit in the ISCR. Clearing a control bit leaves the status bit unaffected.

Level triggered interrupt requests are generated when a specified active level (high or low) is detected. An interrupt service routine must restore the interrupt signal to the inactive state at the source. Writing to level sensitive interrupt status bits has no effect. It is assumed that the reset state of all level sensitive interrupts is inactive.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RES	CE_ INT2	CE_ INT1	SYNTH_ IRQ	XUART_ INTB	XUART_ INTA	OTG_ FS_ INT	ENET_ INT	RES	RES	RES	RES	FSH_ OVR	OTG_ FS_ OVR	PB_ IRQ	LOW BAT
OPER	-	R	R	R	R	R	R	R	-	-	-	-	R/W1C	R/W1C	R/W1C	R/W1C
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-9. Interrupt Status/Clear Register (ISCR)

Table 3-12. Interrupt Status/Clear Register Bit Definitions

Name	Description	Settings
LOW_BAT Bit 0	**Low Battery —** Low Battery signal from MC13783 has changed state	0 = No interrupt pending 1 = Interrupt active, write a one to clear
PB_IRQ Bit 1	**Push button IRQ —** Push button switch circuit output has changed state	0 = No interrupt pending 1= Interrupt active, write a one to clear
OTG_FS_OVR Bit 2	**USB OTG Full Speed Over Current —** USB OTG Full Speed Over Current bit has changed state	0 = No interrupt pending 1= Interrupt active, write a one to clear
FSH_OVR Bit 3	**USB Full Speed Host Over Current —** USB Full Speed Host interface overcurrent bit has changed state.	0 = No interrupt pending 1 = Interrupt active, write a one to clear
RES Bits 4,5,6,7, & 15	Reserved for future use	N/A
ENET_INTI Bit 8	**Ethernet Interrupt —** Ethernet controller interrupt request	0 = No interrupt from Ethernet controller 1 = Interrupt from Ethernet controller
OTG_FS_INT Bit 9	**USB Host Full Speed Interrupt —** USB Host full speed interface interrupt request	0 = No interrupt from USB Host full speed interface 1 = Interrupt from USB Host full speed interface.
XUART_INTA Bit 10	**External UART A interrupt —** External UART A interrupt request	0 = No interrupt from External UART A 1 = Interrupt from External UART A
XUART_INTB Bit 11	**External UART B interrupt —** External UART B interrupt request	0 = No interrupt from External UART B 1 = Interrupt from External UART B
SYNTH_IRQ Bit 12	**Audio Synthesizer IRQ –** Audio Synthesizer interrupt request	0 = No interrupt from Audio Synthesizer 1 = Interrupt from Audio Synthesizer
CE_INT1 Bit 13	**Communication Engine Interrupt 1 —** CE bus interrupt request 1	0 = No interrupt from CE_INT1 1 = Interrupt from CE_INT1
CE_INT2 Bit 14	Communication Engine Interrupt 2— CE bus interrupt request 2	0 = No interrupt from CE_INT2 1 = Interrupt from CE_INT2

3.3.6.9 Interrupt Signal Status Register (ISSR)

This register shows the state of each edge triggered interrupt source. This register is a read only register.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	FSH_ OVR	OTG_ FS_ OVR	PB_ IRQ	LOW_BAT

Figure 3-10. Interrupt Signal Current State Status Register (ISCSSR)

Table 3-13. Interrupt Signal Status Register Bit Definitions

Name	Description	Settings
LOW_BAT Bit 4	**Low Battery—** Low Battery Indicator signal from MC13783 Board.	0 = Low Battery indication 1 = Normal operation
PB_IRQ Bit 5	**Push Button IRQ —** Push button switch circuit.	0 = Push button is pressed 1 = Push button is not pressed
OTG_FS_OVR Bit 6	**USB OTG Full Speed Over Current —** USB OTG Full Speed Over Current indication.	0 = Over Current indication 1 = No Over Current indication
FSH_OVR Bit 7	**USB Full Speed Host Over Current —** The USB Full Speed Host interface Over current indication.	0 = Over Current indication 1 = No Over Current indication

3.3.6.10 Interrupt Mask Register (IMR)

The IMR enables and disables the corresponding interrupt source. Setting a control bit enables the associated interrupt source; clearing a bit disables (masks) the associated interrupt source. When an interrupt is masked, the associated status register bit still indicates whether an interrupt is pending. However, a masked interrupt source cannot cause the GPIO pin it is associated with to generate an interrupt request signal. Modifying the IMR to enable an interrupt that is pending causes an interrupt request to be generated immediately.

This register is implemented as a set register and a clear register. To set a bit, write a 1 to the bit at the set address. To clear a bit, write a 1 to the bit at the clear address.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RES	CE_ INT2	CE_ INT1	SYNTH_ IRQ	XUART_ INTB	XUART_ INTA	OTG_ FS_ INT	ENET_ INT	RES	RES	RES	RES	FSH_ OVR	OTG_ FS_ OVR	PB_ IRQ	LOW_BAT
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-11. Interrupt Mask Register (IMR)

3.4 GPIO Interrupt Grouping and Non-registered Interrupts

Some interrupt signals are not associated with a CPLD register but are routed to a GPIO pin inside the CPLD. The SD and Memory Stick detect functions are compared in a logical OR because only one type can implemented at a time. Table 3-14 shows interrupt grouping and Table 3-15 shows status bit descriptions.

Table 3-14. GPIO Interrupt Grouping

GPIO Pin	Interrupt Sources
GPIO1_1	SD1_DET + MS1_DET
GPIO1_2	SD2_DET + MS2_DET
GPIO1_3	PRI_INT (MC13783)
GPIO1_4	XUART_INTA, XUART_INTB, ENET_INT, LOW_BAT, PB_IRQ, OTG_FS_OVR, OTG_FS_INT, FSH_OVR, SYNTH_IRQ, CE_INT1, CE_INT2

Table 3-15. GPIO Interrupt Bit Descriptions

Name	Description	Settings
GPIO1_1	SD1 OR MS1 memory card detect status	0 = No Card is inserted 1 = A card has been detected
GPIO1_2	SD2 OR MS2 memory card detect status	0 = No Card is inserted 1 = A card has been detected
GPIO1_3	AMC13783 Primary Interrupt output status bit	0 = No interrupt pending 1 = Interrupt active
GPIO1_4	Registered Interrupt Status bit	0 = No interrupt pending 1 = Interrupt active

3.5 On-Board Memory

The ADS has several on-board memory devices. A single MCP contains both a 16M x 16 Burst NOR Flash and an 8M x16 Burst PSRAM (see Figure 3-12). The ADS is also equipped with 32M x 32 of DDR SDRAM (see Figure 3-13) made up from two 32M x 16 parts. A plug in card with 1G bit storage capacity and an 8 bit data bus interface is also included. It is described later in this chapter.

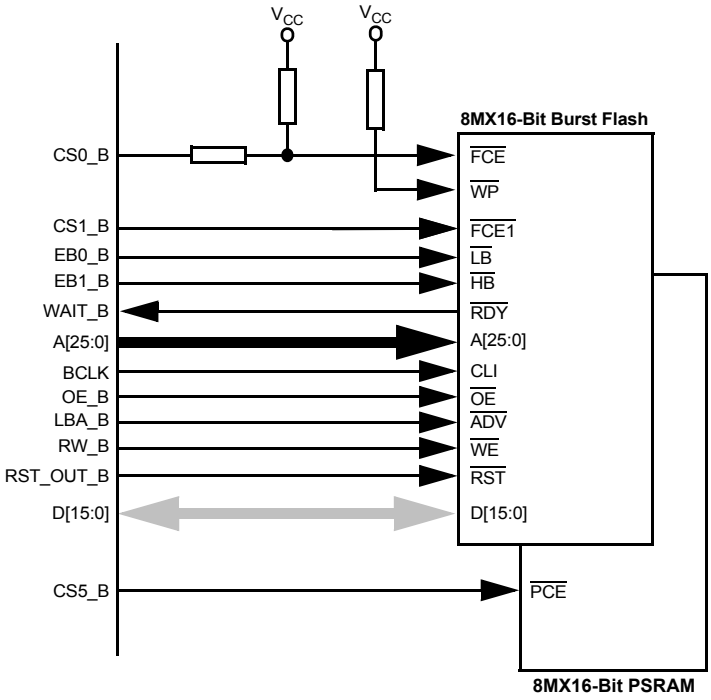


Figure 3-12. Burst Flash and PSRAM Interface

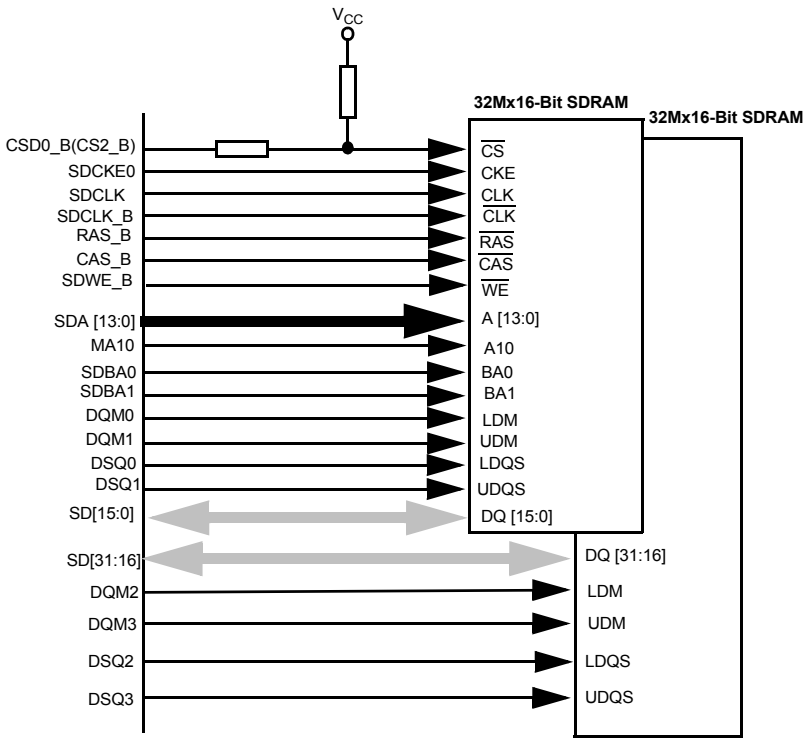


Figure 3-13. DDR SDRAM Interface

3.6 Using a NAND Flash Card

CAUTION

To avoid circuit damage, do not plug-in the NAND Flash card with power applied to the board.

Your i.MX31 ADS comes with a NAND Flash card installed. Should it ever be removed connect P1 of the NAND Flash module to J9 on the CPU board. Screws have been added to better hold the card in place and these will need to installed too. The card provided with the ADS uses an 8 bit interface and has 1 gigabits of storage. For details on the NAND Flash interface, refer to the specification document on the documentation CD.

3.7 USB On-The-Go Interface (FS/LS)

The ADS provides a USB OTG Full Speed/Low Speed interface that uses a Phillips ISP1301BS USB transceiver connected to J2, a mini AB USB connector. The interface can function as either a USB host or USB device. The interface provides power to the USB bus in host mode. This power may be supplied by the Phillips part or from the external +5 volt power source through a MIC2536 power switch. For details on the operation of this USB interface, refer to the i.MX31 data sheet. Figure 3-14 shows this USB interface connection. Note that if MC13783' OTG transceiver is used, this interface cannot be used.

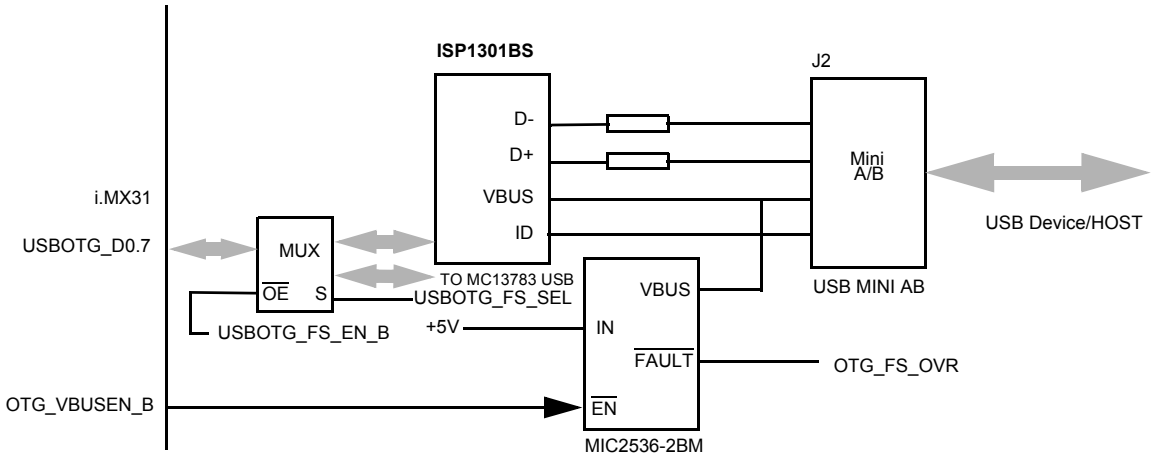


Figure 3-14. USB OTG (FS/LS) Interface

3.8 USB On-The-Go ULPI Interface (HS)

The ADS provides a USB OTG High Speed (480M bps) interface that uses a Phillips ISP1504 USB ULPI transceiver connected to J1, a mini AB USB connector. It can also operate at Full Speed or Low Speed. The interface can function as either a USB host or USB device. The interface provides power on the USB bus in host mode. This power may be supplied by the Phillips part or from the external +5 volt power source through a MIC2536 power switch. For details on the operation of this USB interface, refer to the i.MX31 data sheet. Figure 3-15 shows this USB interface connection.

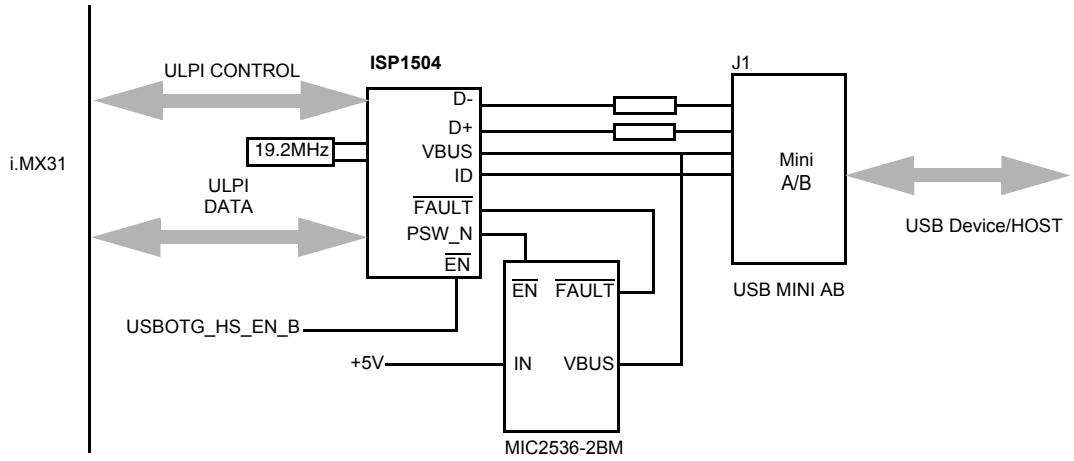


Figure 3-15. USB OTG HS ULPI Interface

3.9 USB HOST ULPI Interface (HS)

The ADS provides a USB High Speed (480M bps) interface that uses a Phillips ISP1504 USB ULPI transceiver connected to a type A USB connector, J4. It can also operate at Full Speed or Low Speed. The interface can function only as a USB host. The interface provides power on the USB bus. This power may be supplied by the Phillips part or from the external +5 volt power source through a MIC2536 power switch. For details on the operation of this USB interface, refer to the i.MX31 data sheet. Figure 3-16 shows the USB HOST interface connection.

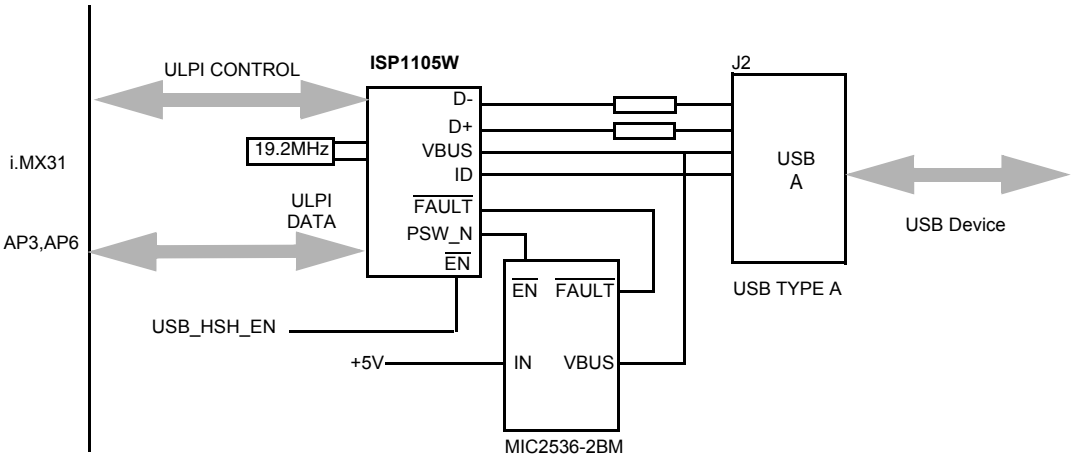


Figure 3-16. USB HS HOST ULPI Interface

3.10 USB HOST Interface (FS/LS)

The ADS provides a USB HOST interface that uses a Phillips ISP1105W USB transceiver connected to a type A USB connector, J5. It can operate at Full Speed or Low Speed. The interface can function only as a USB host. The interface provides power on the USB bus. This power is supplied by from the external +5 volt power source through a MIC2536 power switch. For details on the operation of this USB interface, refer to the i.MX31 data sheet. Figure 3-17 shows the USB interface connection.

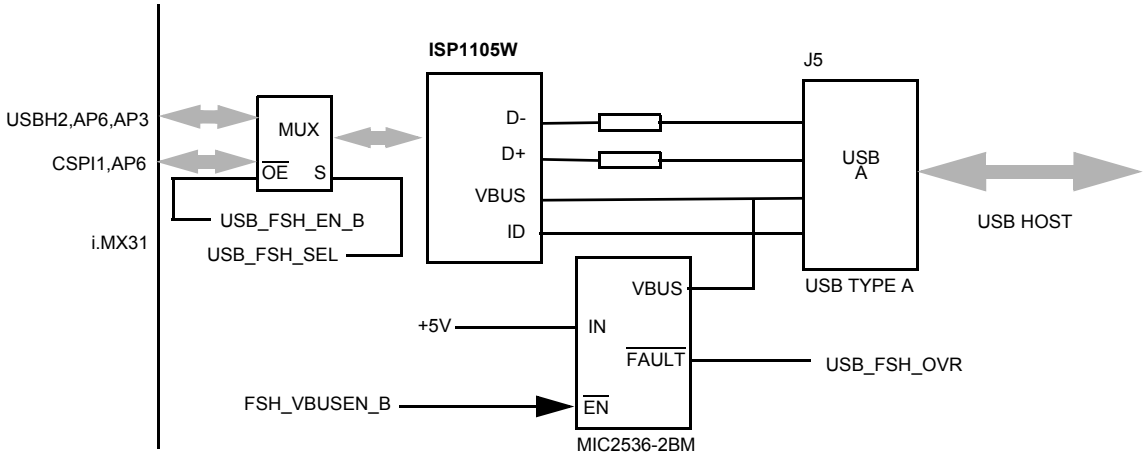


Figure 3-17. USB FS/LS HOST Interface

3.11 UART (Internal) and IrDA Interfaces

The ADS has three RS-232 compatible UART Interfaces that service the internal UARTs of the i.MX31. UARTA and UARTB are DTE and UARTC is DCE. UARTA and UARTC can have full modem support, but not UART B. All three interfaces have a choice between two sets of UART signals from i.MX31.There is also a FIR (Fast Infra Red) transceiver connected to UART2 of the i.MX31. All four interfaces can be enabled on power up based on SW1 switch settings. Mux and enable controls can be software controlled through the CPLD.

Figure 3-18 shows how the UART and IrDA circuits are connected.

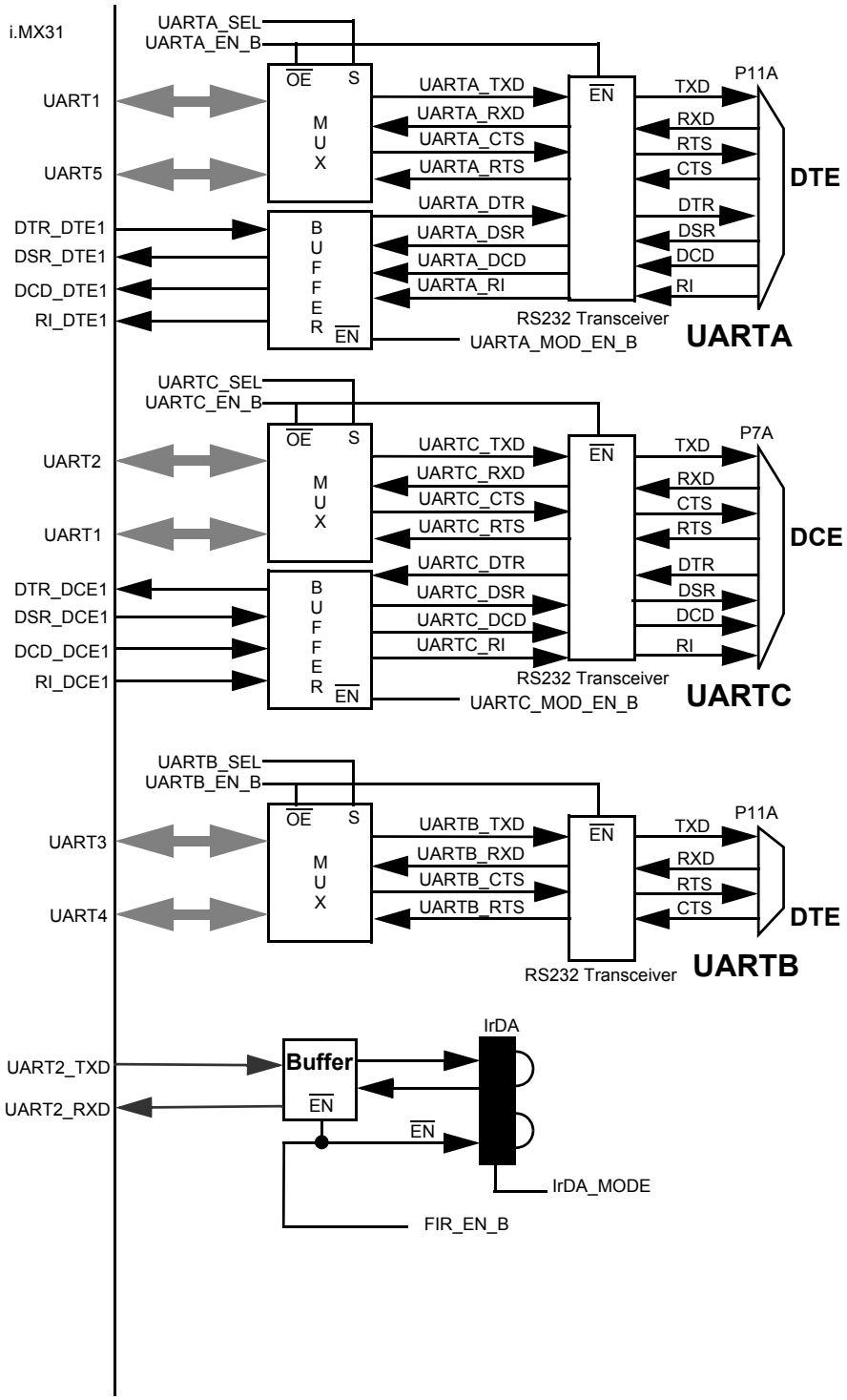


Figure 3-18. UARTs and IrDA Interface

3.12 Ethernet Interface

The ADS is equipped with a Cirrus Logic CS8900A Crystal LAN ISA Ethernet Controller. The CS8900A has 10BaseT transmit and receive filters. The interface can operate in interrupt-driven mode and perform DMA transfers. Chip-select function is controlled by CPLD logic. Figure 3-19 shows the Ethernet interface.

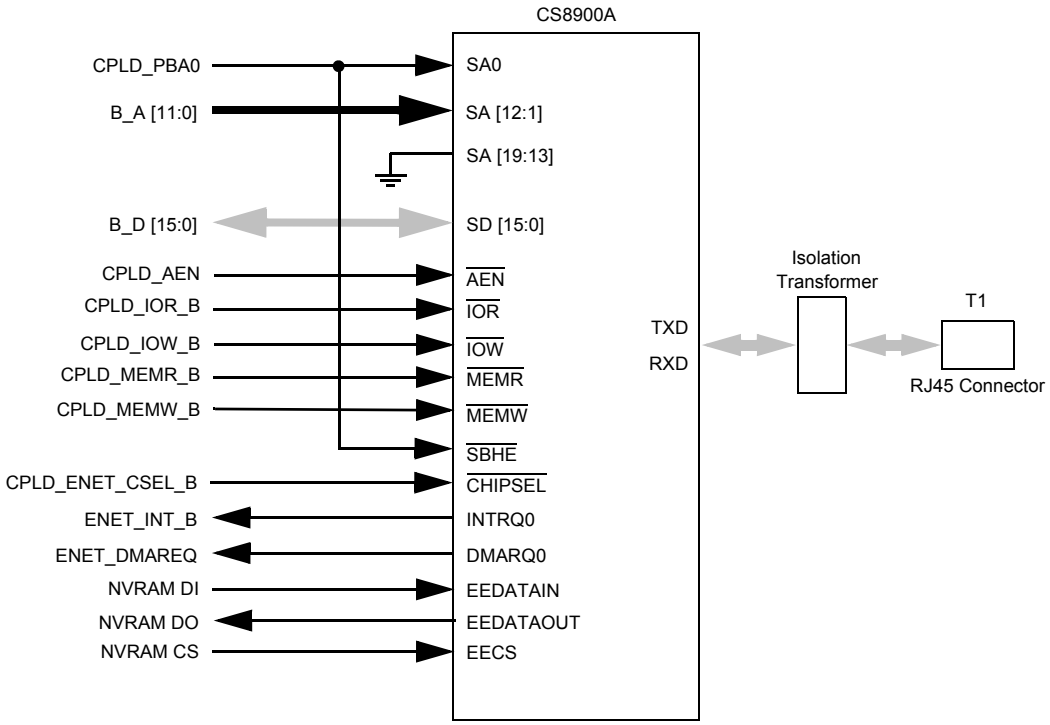


Figure 3-19. Ethernet Interface

3.13 LCD/IPU Interfaces

The ADS support several different types of LCD interfaces. The asynchronous LCD interface (J12) is where scan control is provided by the i.MX31. This is similar to the LCD interface of previous i.MX processors. Additionally there are connectors for “smart” LCD interfaces. These LCD display types can buffer data and provide scan control without the help of the CPU. Two connectors (J8, J9) are parallel and one is serial (J6). There is also a connector with CSPI3 signals available for serial LCD control (J15). Besides control signals these connectors have power, selects, backlight controls, and GPIO signals. J20 connects to the three push button switches and the Fun Light connections on the MC13783 card. To use the Fun Light signals the Fun Light components on the MC13783 card must be disabled by removing R136 through R144.

3.14 Keypad

The ADS includes an external keypad module that connects to the Base board at J21. The keys provide tactile feedback. The keypad interface reads the pad via the KCOL[7:0] and KROW[7:0] signals. The

interface has chording diodes to prevent ghost key presses. The keys are labeled with numeric, cursor control, soft key, and spare key functions, but the actual functionality is determined by user software. A few of the keypad functions must be read through the CPLD. The default keypad can be replaced by a custom design. Table 3-16 shows the key switch matrix to the keypad signals by function name (as labeled on the PCB) and the switch reference designators.

Table 3-16. Keypad Layout and Connections

	KCOL7	KCOL6	KCOL5	KCOL4	KCOL3	KCOL2	KCOL1	KCOL0
KROW7	O SW52	P SW53	BACK SP SW54	L SW55	ENTER SW56	SW57	ON/OFF SW58	SPACE SW59
KROW6	I SW44	U SW45	K SW46	J SW47	M SW48	N SW49	H SW50	B SW51
KROW5	G SW36	V SW37	C SW38	X SW39	Z SW40	CAPS SW41	SYMB SW42	TAB SW43
KROW4	Y SW28	T SW29	R SW30	F SW31	E SW32	D SW33	S SW34	A SW35
KROW3	W SW20	Q SW21	REC SW22	* sw23	0 SW24	8 SW25	# SW26	9 SW27
KROW2	6 SW12	7 SW13	8 SW14	VOL DWN SW15	4 SW16	1 SW17	2 SW18	3 SWSW19
KROW1	APP4 SW4	APP3 SW5	APP2 SW6	VOL UP SW7	APP1 SW8	HOME SW9	SEND SW10	KEY1 SW11
KROW0	BACK SW1	END SW2	KEY 2 SW3	UP*	RIGHT*	DOWN*	LEFT*	SEL*

3.15 Audio Indicator

The ADS includes an audio indicator or buzzer, BZ1. When SW2-2 is ON, the PWMO pin of the ADS controls this function. This buzzer operates from 1 KHz to 10 KHz. The maximum sound level is reached when the frequency is 3 KHz and the duty cycle is 50%.

3.16 LED Indicators

Table 3-17 shows the ADS LED indicators and their associated functions.

Table 3-17. Function of LED Indicators

Reference #	Color	Name	ADS BOARD	Function
D1	Green	+5V	CPU	5 V power is ON
D4	Green	+3.3V	CPU	3.3 V power is ON
D5	Yellow	STAT 0	BASE	User status controlled by CPLD
D6	Yellow	STAT 1	BASE	User status controlled by CPLD
T1	Green	ACTIVE	BASE	Blinking indicates LAN Activity
T1	Yellow	LINK	BASE	Link good or host controlled output
T1	Red	BSTAT	BASE	ISA bus activity
D1	Yellow	LED_SYNTH	BASE	YUM782B output indicator
D4-D10	Yellow	LEDxx_FORCE	MC13783	Backlight LED indicator, not provide
D11,D12,D13	Yellow	FUNLITES	MC13783	Tri-colored LEDs used for color mixing

Table 3-17. Function of LED Indicators

Reference #	Color	Name	ADS BOARD	Function
D21-D40	Yellow	PWR ON X	MC13783	ON indicates the MC13783 voltage active

3.17 Sound Synthesizer

The ADS includes a Yamaha YUM783 mobile audio synthesizer. This device can simultaneously generate up to 64 different voices (32 FM synthesized, 32 wave table). The CPLD decodes a sixteen bit chip select and provides the byte routing for the synthesizer. A speaker connectors and a 3.5mm headphone jack are provided, las well as low and high impedance inputs and outputs (mono). These signals can to connected to the MC13783 board audio interface using standard 3.5mm patch cables. There is also a digital audio interface that may be used with MCU audio port 6. The YUM783 data sheet is provided on the ADS data CD.

3.18 Using the TFT LCD Display Panel

The ADS is equipped with a Sharp LQ035Q7DB02 touch control enabled TFT LCD display assembly. The ADS documentation CD contains specifications for the TFT LCD component.

CAUTION

Make sure that the input power to the main board is disconnected or switched off before connecting the LCD module. Connecting the module with power applied can damage the LCD module and/or the main board.

To use the TFT LCD display, connect the 34 conductor ribbon cable supplied with the ADS from J11 on the LCD module to J12 on the Base board. The Touch Screen Controller is built into the MC13783 chip and therefore the MC13783 board is required for this function to operate.

The potentiometer VR1, which is to the left of the LCD panel just below J11, controls flickering of the display screen. This control is set at the factory and normally does not require adjustment. However, if the TFT LCD display flickers, you may adjust VR1 to stabilize the display. Use a suitable flat head or phillips head screwdriver. Because the adjustment is normally done with power applied, we recommend use of a plastic blade tool.

3.19 Using the Keypad

To use the keypad module, connect the 30 conductor ribbon cable supplied with the ADS from connector P1 of the Keypad module to J21 of the Base board**.**

3.20 Using the Image Sensor Daughter Card

Connectors J10 and J13 are pre-configured to operate directly with the IM8012 image sensor daughter card supplied with the ADS. Communication with this card takes place through the I^2C interface. For details on image sensor operation, refer to the data sheet on the documentation CD.

CAUTION

To avoid circuit damage, do not plug-in the image sensor card with power applied to the board.

To install the image sensor card, plug its 48 position DIN connector into either J10 or J13 of the Base board. When the image sensor card is installed at J10, the two boards are at a right angle to each other, with the image sensor facing away from the Base board.When the image sensor card is installed at J13, the two boards are parallel and the image sensor faces up, away from the Base board.

3.21 Using the TV Encoder

A TV encoder card is supplied with the ADS. The main component is a FS453 (PC to TV Video Scan converter) from FOCUS Enhancements Semiconductor. For details on TV encoder operation, refer to its data sheet, available at http://www.focusinfo.com/

CAUTION

Make sure that input power is disconnected or switched off before the TV encoder card is installed. Connecting the card with power applied can damage the TV encoder card and the Base board.

This TV encoder cannot be used at the same time as any parallel LCD display because they share IPU data connections. To use the TV encoder module, you must disconnect the TFT LCD board from J12 on the Base board and install the TV encoder module in J12 and J11of the Base board.

3.22 Using a Plug in Memory Card

The ADS provides several plug-in memory cards. Two Memory Stick card holders are on the CPU card (J5, J6). The Base board has two SD/MMC card holders (P3, P4) as well as a SIMM card connector (P8). The Memory Stick and SD/MMC connectors share the same control signals from the i.MX31. J5 (MS1) shares with P3 (SD/MMC1) and J6 (MS2) shares with P4 (SD/MMC2). The interface signals to the Memory Stick on the CPU card are multiplexed. They are either routed to the cards or to the Base board where they may be used with the SD/MMC cards or some other designated interface. Each Memory Stick mux has an individual control signal from the CPLD.

Interface signals are provided by the i.MX31 but write protect and card detect inputs are read through the CPLD. Power to the card requires the MC13783 card. The associated NVCC power must also be set to select the same MC13783-provided power source. You must obtain a compatible card for use with these connectors.

3.23 Using a PCMCIA Card

The ADS comes equipped with a PCMCIA card holder, U30 on the Base board. Most of the PCMCIA interface signals are buffered including the data and address that are shared with other system peripherals. The card is powered by a LTC1472CS power switch. Only 3.3V cards are supported and MC13783 power is not required. The CPLD controls the LTC1472CS. It can turn VCC power ON and OFF and VPP power can be set to +5V or left unconnected (Hi-Z). These default to OFF and unconnected at reset. You must supply a compatible PCMCIA card for use with the i.MX31 ADS.

3.24 Using a Mini ATA Hard Drive

The ADS provides an ATA5 compatible interface designed to work with mini hard drives. J3 is a 44 pin header designed to be directly compatible with Hatachi mini drives. The dual row, 2mm spaced connector requires a ribbon cable to connect to the mini drive. Neither the cable nor the drive is provided with the ADS. Most of the ATA signals are multiplexed and then translated to 3.3V levels for the mini hard drive. The CPLD controls the multiplexer enables and selects.

CAUTION

Make sure that input power is disconnected or switched off before the mini hard drive is connected. Connecting it with power applied can damage the mini hard drive and the Base board.

3.25 Using the MC13783 Power Management Board

The MC13783 Power Management Board (APMB) provides many functions beside power regulation. It has audio interface and processing, tri-colored Fun Light LED controls, touch panel controller, backlight LED drivers, programming interfaces to both a primary and secondary processors, a vibratory actuator, a USB OTG transceiver, battery charging controller, battery emulation for both the main and coin cell batteries, and two 32KHz clock outputs. Most regulators have programmable output voltages. The switching regulators feature voltage scaling that can be used to minimize power consumption. Back up power control for part of the ARM core and SDRAM memory is also provided.

Be careful to follow the configuration guide in chapter 2 when installing this board. Plugging in the APMB will disable all power regulators on the CPU board, including the 3.3V one. However if jumpers for NVCC power selections are left installed on the CPU, MC13783 regulator outputs could be shorted. Plugging in the MC13783 enables the 3.3V regulator on the Base board. This regulator features a buck-boost configuration which can maintain the 3.3V output even if the input voltage is below 3.3V. In fact it is designed to operate from 4.5 volts down to 2.5 volts, the useful range of most lithium batteries. This combined with MC13783' capabilities allows the system to operate from an external source in the useful voltage range of most battery applications. Using actual batteries is possible but not really practical because the current consumption of the system has not been optimized.

3.26 Using the ETM Connectors

Two connectors for connecting the ARM based i.MX31 CPU to an ARM supplied ETM (Embedded Trace Macrocell) are provided. Since this capability is normally needed only during development, the ETM functions are pin shared with other modules. Using these pins for ETM will prohibit their use with the other modules. Having Main and Alternate ETM connectors allows the user to choose which signal group will be replaced by ETM signals.

3.27 Using the Samtec Logic Analyzer Connectors

The CPU board has four specialized Samtec connectors designed to be compatible with Logic Analyzer cables from HP that use the mating connector. This style of connector has lower capacitance than Mictor style connections. All CPU connections required for memory interfacing are brought to these connectors.

Chapter 4 ADS Connectors and Signals

4.1 Introduction

This chapter describes connector pin assignments and signals for the M9328MX31ADS Base, CPU, and APM boards. The tables in this section list signal names as they appear in the board schematics. The use of "_B" at the end of a name indicates an active low signal.

4.2 Base Board Connectors

Table 3-1 shows the Base board connectors. Figure 3-1 shows connector layout on the left-hand side of the Base board. Figure 3-2 shows connector layout on the right-hand side of the Base board. Connectors P1 and P2, which mate with connectors J1 and J2 on the CPU board; and P5 and P6, which mate with connectors J5 and J6 on the MC13783 board, are described in this section.

Table 4-1. Base Board Connectors

Connector	Type	Description	Figure
J1	Mini AB	USB OTG high speed	Figure 3-1, top
J2	Mini AB	USB OTG full speed	Figure 3-1, top
J3	44-pin header	Small form-factor ATA	Figure 3-2, top
J4	Standard USB Host	USB host high speed	Figure 3-1, top
J5	Standard USB Host	USB host full speed	Figure 3-1, top
J6	16-pin header	Smart serial LCD	Figure 3-2, right
J7	10-pin header	UART B (ADS) RS-232 DCE	Figure 3-1, top
J8	40-pin header	Smart parallel LCD 2	Figure 3-2, right
J9	40-pin header	Smart parallel LCD 1	Figure 3-2, right
J10	16-pin, 3-row	CSI 1 (horizontal)	Figure 3-1, left
J11	16-pin header	Synchronous LCD option	Figure 3-2, right
J12	34-pin header	Synchronous LCD	Figure 3-2, right
J13	16-pin, 3-row	CSI 2 (vertical)	Figure 3-1, left
J14	10-pin header	CPLD in-circuit programming	Figure 3-1, left
J15	20-pin header	CSPI interface	Figure 3-2, right
J16	10-pin header	TV encoder	Figure 3-2, right
J17	16-pin, 3-row	Expansion 1 (horizontal)	Figure 3-1, left
J18	20-pin header	MC13783 A/D (not populated)	Figure 3-1, bottom
J19	14-pin header	CE bus	Figure3-1, left
J20	16-pin header	Funlight	Figure 3-2, right
J21	30-pin header	Keypad	Figure 3-2, right
J22	16-pin, 3-row	Expansion 1 (horizontal)	Figure 3-1, left

Table 4-1. Base Board Connectors (continued)

Connector	Type	Description	Figure
J23	16-pin, 3-row	Expansion 1 (vertical)	Figure 3-1, left
J24	64-pin	Baseband	Figure 3-1, bottom
J25	Mini-jack	Voice transmission output	Figure 3-2, bottom
J26	Mini-jack	External analog output	Figure 3-2, bottom
J27	Mini-jack	Stereo headphone output	Figure 3-2, bottom
J28	Mini-jack	Voice output	Figure 3-2, bottom
J29	Mini-jack	External analog input	Figure 3-2, bottom
JP13	3-pin jumper	1^2C (source selectable)	Figure 3-1, left
P1	215-pin	Base/CPU 1	Figure 3-2, top
P2	215-pin	Base/CPU 2	Figure 3-1, top
P3	Memory card	SD/MMC 1	Figure 3-1, top
P4	Memory card	SD/MMC 2	Figure 3-1, top
P5	215-pin	Base/MC13783 1	Figure 3-2, bottom
P6	215-pin	Base/MC13783 2	Figure 3-2, bottom
P7A	DB-9	UART C (MCU) RS-232 DCE	Figure 3-1, left
P7B	DB-9	UART A (ADS) RS-232 DCE	Figure 3-1, left
P8	GSM SIM	SIMM	Figure 3-1, left
P9	40-pin	Software analysis	Figure 3-1, left
P10	40-pin	Software analysis	Figure 3-1, left
P11A	DB-9	UART A (MCU) RS-232 DTE	Figure 3-2, left
P11B	DB-9	UART B (MCU) RS-232 DTE	Figure 3-2, left
T1	RJ45	Ethernet	Figure 3-1, left
TB1	Screw terminal	Stereo speaker output	Figure 3-1, bottom
U30	PCMCIA	PCMCIA	Figure 3-1, bottom

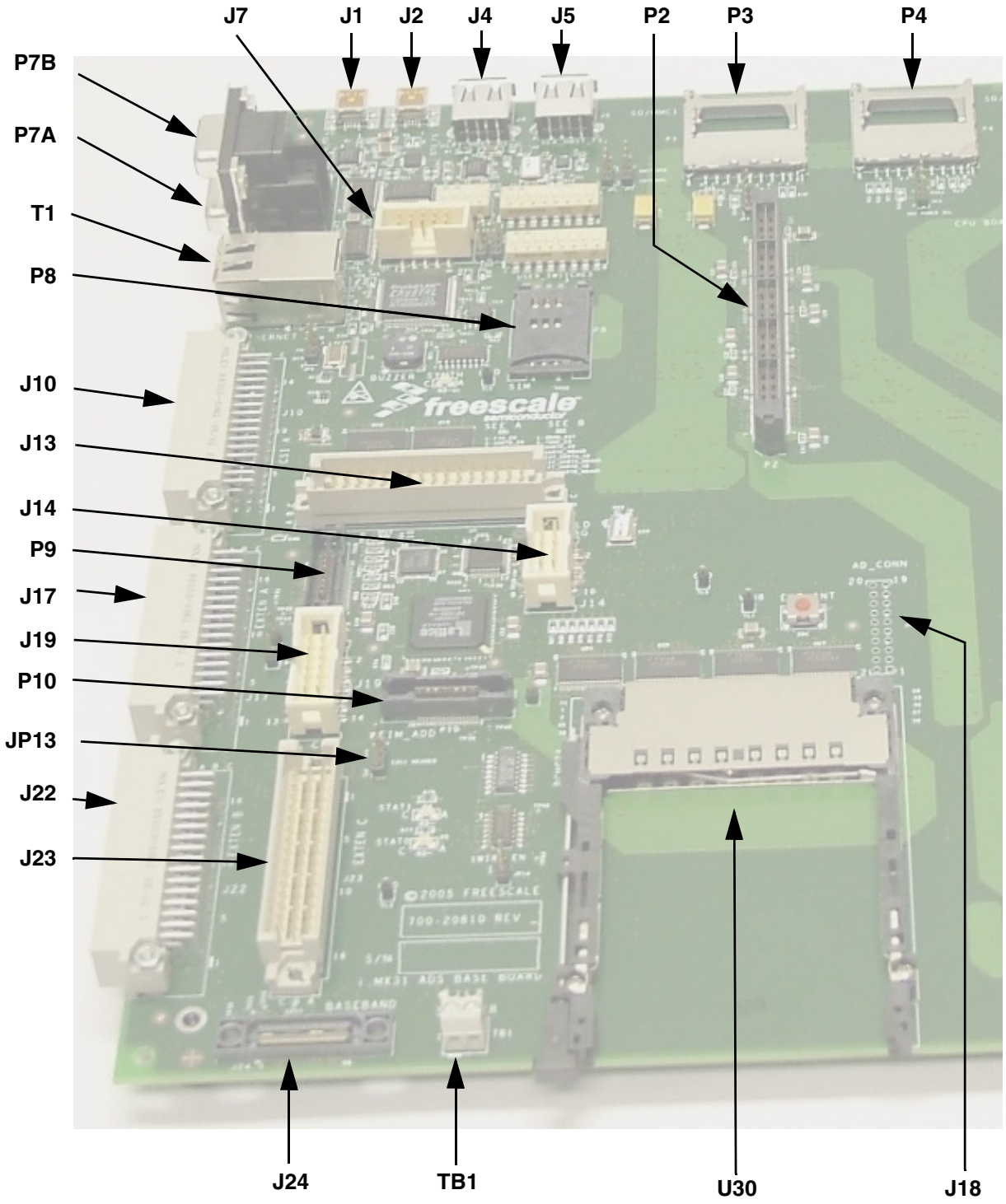


Figure 4-1. Base Board Connectors — Left Side

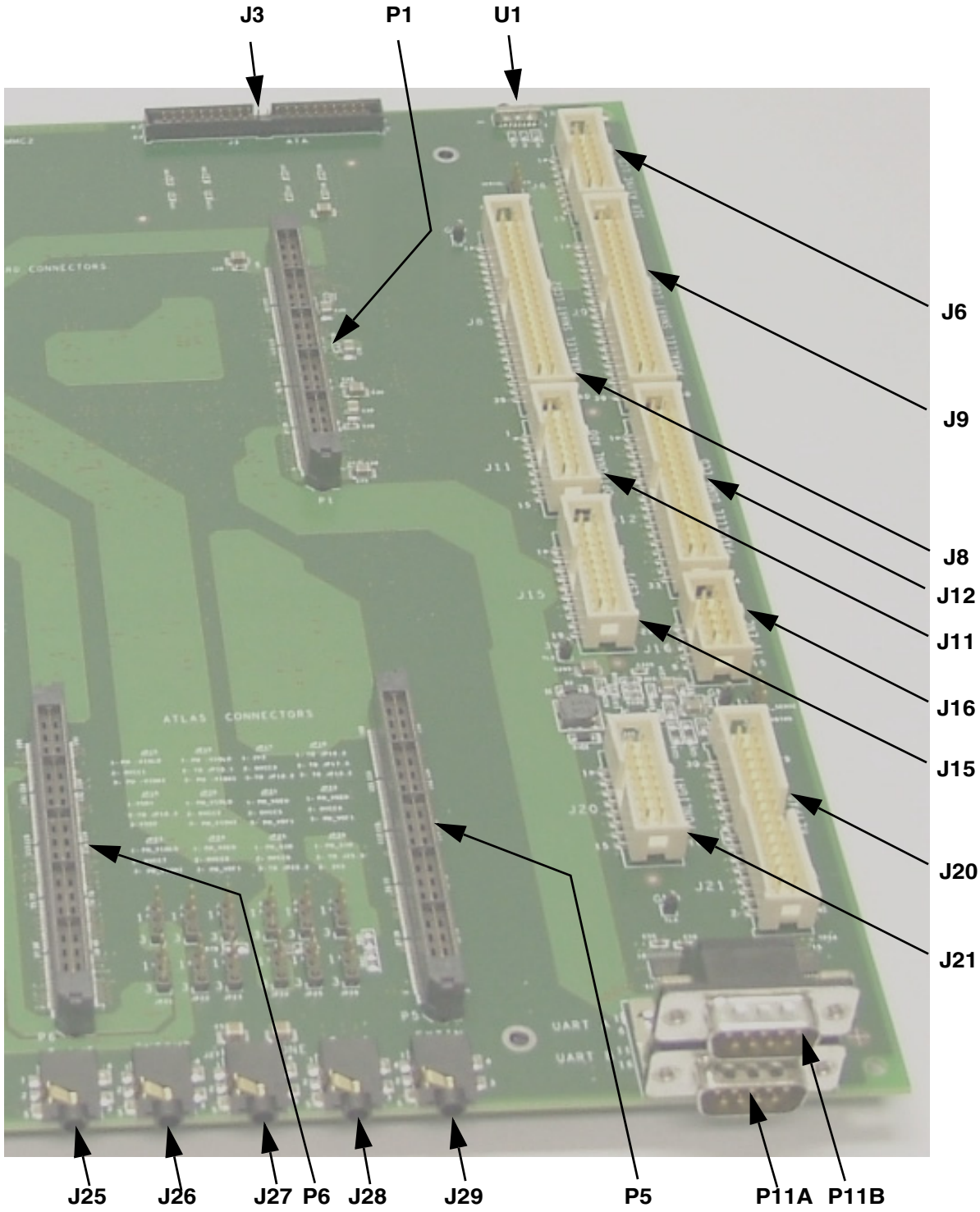


Figure 4-2. Base Board Connectors — Right Side

4.2.1 Base Board to CPU Board Connectors

ADS Base board connectors P1 and P2 mate with CPU board connectors J1 and J2 (bottom side). Figure 4-3 shows connector pin assignments. Table 4-2 and Table 4-3 describe connector signals.

P1

5V	2	1	5V		
5V	4	3	5V		
5V	6	5	PC_RST		
5V	8	7	PC_BVD1		
PC_RW_B	10	9	PC_BVD2		
PC_PWRON	12	11	PWMO		
PV_VS2	14	13	CAPTURE		
GND	16	15	COMPARE		
CSP13_MOSI	18	17	VSD1		
CSP13_MISO	20	19	VSD1		
CSP13_SPI_RDY	22	21	SD1_DATA0		
CSP13_SCLK	24	23	SD1_DATA1		
GND	26	25	SD1_DATA2		
ATA_DMAC	28	27	SD1_DATA3		
ATA_RESET_B	30	29	GND		
ATA_DIOW	32	31	SD1_CLK		
ATA_DIOR	34	33	SD1_CMD		
ATA_CS1	36	35	NVCC3		
ATA_CS0	38	37	NVCC3		
GND	192	191	GND		
GND	194	193	GND		
		195	GND		
VSD2	40	39	NVCC3		
VSD2	42	41	IOIS16		
PC_CD2_B	44	43	PC_WAIT_B		
PC_CD1_B	46	45	PC_READY		
STXD4	48	47	PC_VS1		
SRXD4	50	49	GND		
SFS4	52	51	USBOTG_STP		
SCK4	54	53	USBOTG_DIR		
GND	56	55	USBOTG_NXT		
SCK4	58	57	USBOTG_CLK		
SRXD4	60	59	GND		
SFS4	62	61	USBOTG_DATA0		
STXD4	64	63	USBOTG_DATA1		
GND	66	65	USBOTG_DATA2		
USB_BYP	68	67	USBOTG_DATA3		
USB_OC	70	69	USBOTG_DATA4		
USB_PWR	72	71	USBOTG_DATA5		
NVCC5	74	73	USBOTG_DATA6		
NVCC5	76	75	USBOTG_DATA7		
GND	196				
GND	198	197	GND		
GND	200	199	GND		
NVCC5	78	77	NVCC5		
OWDAT	80	79	CSP12_MOSI		
CSPI2_SPI_RDY	82	81	CSP12_MISO		
CSPI2_SCLK	84	83	CSP12_SS1		
GND	86	85	CSP12_SS0		
IPU_LCS1	88	87	CSP12_SS2		
IPU_LCS0	90	89	GND		
GND	92	91	CLK_26M		
IPU_VSYNCH3	94	93	GND		
GND	96	95	IPU_LD17		

P2

3V3	2	1	NVCC2		
3V3	4	3	NVCC2		
3V3	6	5	STXD6		
B_D0	8	7	SRXD6		
B_D1	10	9	SFS6		
B_D2	12	11	SCK6		
B_D3	14	13	GND		
B_D4	16	15	SCK3		
B_D5	18	17	SRXD3		
B_D6	20	19	SFS3		
B_D7	22	21	STXD3		
B_D8	24	23	GND		
B_D9	26	25	CSPI1_SCLK		
B_D10	28	27	CSPI1_MISO		
B_D11	30	29	CSPI1_MOSI		
B_D12	32	31	CSPI1_SS2		
B_D13	34	33	CSPI1_SS1		
B_D14	36	35	CSPI1_SS0		
B_D15	38	37	CSPI1_SPI_RDY		
GND	192	191	GND		
GND	194	193	GND		
		195	GND		
B_A15	40	39	PM_BKUP_DDR		
B_A14	42	41	PM_BKUP_DDR		
B_A13	44	43	NC		
B_A12	46	45	PWGT2_OUT		
B_A11	48	47	PWGT2_OUT		
B_A10	50	49	NC		
GND	52	51	USBH2_NXT		
B_A9	54	53	USBH2_STP		
B_A8	56	55	USBH2_DIR		
B_A7	58	57	GND		
B_A6	60	59	USBH2_CLK		
B_A5	62	61	GND		
GND	64	63	USBH2_DATA1		
B_A4	66	65	USBH2_DATA0		
B_A3	68	67	PM_SW1A		
B_A2	70	69	PM_SW1A		
B_A1	72	71	PC_POE		
B_A0	74	73	PWGT1_OUT		
B_A16	76	75	PWGT1_OUT		
GND	196				
GND	198	197	GND		
GND	200	199	GND		
B_A17	78	77	DVDD_1.8V		
B_A18	80	79	DVDD_1.8V		
B_A19	82	81	NC		
B_A20	84	83	GND		
B_A21	86	85	BBCLK		
B_A22	88	87	GND		
B_A23	90	89	NC		
B_A24	92	91	CVDD_2.7V		
B_A25	94	93	CVDD_2.7V		
GND	96	95	BLBA_B		

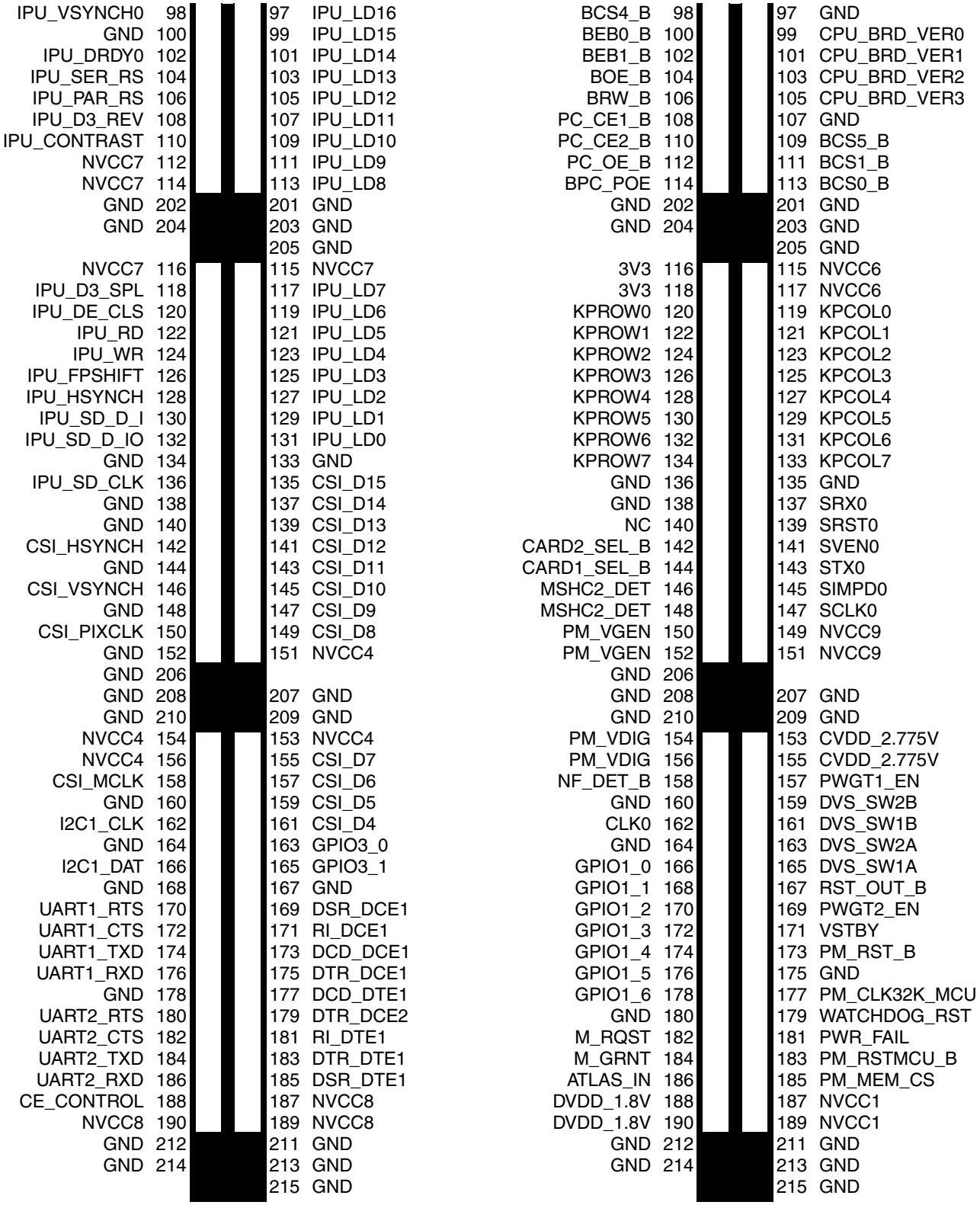


Figure 4-3. Base Board to CPU Board Connectors P1 and P2 Pin Assignment

Table 4-2. Base Board to CPU Board Connector P1 Signal Description

Signal	Pin	Description
5V	1, 2, 3, 4, 6, 8	5VDC Supply Voltage
ATA_CS0	38	CHIP SELECT 0 — ATA controller signal
ATA_CS1	36	CHIP SELECT 1 — ATA controller signal
ATA_DIOR	34	DATA I/O READ — ATA controller signal
ATA_DIOW	32	DATA I/O WRITE — ATA controller signal
ATA_DMAC	28	DIRECT MEMORY ACCESS CONTROL — ATA controller signal
ATA_RESET_B	30	RESET — ATA controller signal
CAPTURE	13	Timer input capture
CE_CONTROL	188	CE bus signal - Signal muxing of the CE bus
CLK_26M	91	26 MHz clock signal
COMPARE	15	LCD BIAS VOLTAGE
CSI_D4	161	CMOS SENSOR INTERFACE DATA 4 — Image Sensor input data
CSI_D5	159	CMOS SENSOR INTERFACE DATA 5 — Image Sensor input data
CSI_D6	157	CMOS SENSOR INTERFACE DATA 6 — Image Sensor input data
CSI_D7	155	CMOS SENSOR INTERFACE DATA 7 — Image Sensor input data
CSI_D8	149	CMOS SENSOR INTERFACE DATA 8 — Image Sensor input data
CSI_D9	147	CMOS SENSOR INTERFACE DATA 9 — Image Sensor input data
CSI_D10	145	CMOS SENSOR INTERFACE DATA 10 — Image Sensor input data
CSI_D11	143	CMOS SENSOR INTERFACE DATA 11 — Image Sensor input data
CSI_D12	141	CMOS SENSOR INTERFACE DATA 12 — Image Sensor input data
CSI_D13	139	CMOS SENSOR INTERFACE DATA 13 — Image Sensor input data
CSI_D14	137	CMOS SENSOR INTERFACE DATA 14 — Image Sensor input data
CSI_D15	135	CMOS SENSOR INTERFACE DATA 15 — Image Sensor input data
CSI_HSYNCH	142	CMOS SENSOR INTERFACE HORIZONTAL SYNC — Control input
CSI_MCLK	158	CMOS SENSOR INTERFACE MASTER CLOCK — Clock output to sensor card
CSI_PIXCLK	150	CMOS SENSOR INTERFACE PIXAL CLOCK — Data latch strobe
CSI_VSYNCH	146	CMOS SENSOR INTERFACE VERTICAL SYNC — Control input
CSP12_MISO	81	MASTER IN / SLAVE OUT — CSPI data signal (bidirectional)
CSP12_MOSI	79	MASTER OUT / SLAVE IN — CSPI data signal (bidirectional)
CSP12_SS0	85	SLAVE SELECT 0 — CSPI signal (bidirectional)
CSP12_SS1	83	SLAVE SELECT 1 — CSPI signal (bidirectional)
CSP12_SS2	87	SLAVE SELECT 2 — CSPI signal (bidirectional)
CSP13_MISO	20	MASTER IN / SLAVE OUT — CSPI data signal (bidirectional)
CSP13_MOSI	18	MASTER OUT / SLAVE IN — CSPI data signal (bidirectional)
CSP13_SCLK	24	SERIAL CLOCK — Bidirectional
CSP13_SPI_RDY	22	READY — CSPI serial burst trigger, active low input
CSPI2_SCLK	84	SERIAL CLOCK — Bidirectional
CSPI2_SPI_RDY	82	READY — CSPI serial burst trigger, active low input
DCD_DCE1	173	UART1 DCE signal - DCD
DCD_DTE1	177	UART1 DTE signal - DCD
DSR_DCE1	169	UART1 DCE signal - DSR
DSR_DTE1	185	UART1 DTE signal - DSR
DTR_DCE1	175	UART1 DCE signal - DTR

Table 4-2. Base Board to CPU Board Connector P1 Signal Description (continued)

Signal	Pin	Description
DTR_DCE2	179	UART2 DCE signal - DTR
DTR_DTE1	183	UART1 DTE signal - DTR
GND	16, 26, 29, 49, 56, 59, 66, 86, 89, 92, 93, 96, 100, 133, 134, 138, 140, 144, 148, 152, 160, 164, 167, 168, 178, 191, 192-215	Signal Ground
GPIO3_0	163	GENERAL PURPOSE I/O
GPIO3_1	165	GENERAL PURPOSE I/O
I2C1_CLK	162	I SQUARED C CLOCK — Serial clock, bidirectional
I2C1_DAT	166	I SQUARED C DATA — Serial data, bidirectional
IOIS16	41	PCMCIA control signal
IPU_CONTRAST	110	CONTRAST — Synchronous LCD control signal
IPU_D3_REV	108	D3_REV — Synchronous LCD control signal
IPU_D3_SPL	118	D3_SPL— Synchronous LCD control signal
IPU_DE_CLS	120	DE_CLS— Synchronous LCD control signal
IPU_DRDY0	102	DRDY— Synchronous LCD control signal
IPU_FPSHIFT	126	FPSHIFT— Synchronous LCD control signal
IPU_HSYNCH	128	HORIZONTAL SYNCH— Synchronous LCD control signal
IPU_LCS0	90	LCS0— Synchronous LCD control signal
IPU_LCS1	88	LCS1— Synchronous LCD control signal
IPU_LD0	131	DISPLAY DATA — Synchronous LCD control signal
IPU_LD1	129	DISPLAY DATA — Synchronous LCD control signal
IPU_LD2	127	DISPLAY DATA — Synchronous LCD control signal
IPU_LD3	125	DISPLAY DATA — Synchronous LCD control signal
IPU_LD4	123	DISPLAY DATA — Synchronous LCD control signal
IPU_LD5	121	DISPLAY DATA — Synchronous LCD control signal
IPU_LD6	119	DISPLAY DATA — Synchronous LCD control signal
IPU_LD7	117	DISPLAY DATA — Synchronous LCD control signal
IPU_LD8	113	DISPLAY DATA — Synchronous LCD control signal
IPU_LD9	111	DISPLAY DATA — Synchronous LCD control signal
IPU_LD10	109	DISPLAY DATA — Synchronous LCD control signal
IPU_LD11	107	DISPLAY DATA — Synchronous LCD control signal
IPU_LD12	105	DISPLAY DATA — Synchronous LCD control signal
IPU_LD13	103	DISPLAY DATA — Synchronous LCD control signal
IPU_LD14	101	DISPLAY DATA — Synchronous LCD control signal
IPU_LD15	99	DISPLAY DATA — Synchronous LCD control signal
IPU_LD16	97	DISPLAY DATA — Synchronous LCD control signal
IPU_LD17	95	DISPLAY DATA — Synchronous LCD control signal
IPU_PAR_RS	106	PARALLEL RS— Synchronous LCD control signal
IPU_RD	122	READ— Synchronous LCD control signal

Table 4-2. Base Board to CPU Board Connector P1 Signal Description (continued)

Signal	Pin	Description
IPU_SD_CLK	136	SERIAL DATA CLOCK — Synchronous LCD control signal
IPU_SD_D_I	130	SERIAL DATA IN — Synchronous LCD control signal
IPU_SD_D_IO	132	SERIAL DATA I/O— Synchronous LCD control signal
IPU_SER_RS	104	SERIAL RESET — Synchronous LCD control signal
IPU_VSYNCH0	98	VERTICAL SYNCH — Synchronous LCD control signal
IPU_VSYNCH3	94	VERTICAL SYNCH — Synchronous LCD control signal
IPU_WR	124	WRITE — Synchronous LCD control signal
NVCC3	35, 37, 39	CONDITIONED POWER SUPPLY
NVCC4	151, 153, 154, 156	CONDITIONED POWER SUPPLY
NVCC5	74, 76, 77, 78	CONDITIONED POWER SUPPLY
NVCC7	112, 114, 115, 116	CONDITIONED POWER SUPPLY
NVCC8	187, 189, 190	CONDITIONED POWER SUPPLY
OWDAT	80	One Wire Data signal
PC_BVD1	7	PCMCIA Battery Voltage Detect 1
PC_BVD2	9	PCMCIA Battery Voltage Detect 2
PC_CD1_B	46	PCMCIA Card Detect 1
PC_CD2_B	44	PCMCIA Card Detect 2
PC_PWRON	12	PCMCIA Power ON
PC_READY	45	PCMCIA READY
PC_RST	5	PCMCIA RESET signal
PC_RW_B	10	PCMCIA READ/WRITE signal
PC_VS1	47	PCMCIA Voltage Sense 1 signal
PC_WAIT_B	43	PCMCIA WAIT signal
PC_VS2	14	PCMCIA Voltage Sense 1 signal
PWMO	11	PULSE-WIDTH MODULATOR OUTPUT
RI_DCE1	171	UART1 DCE signal - Ring Indicator
RI_DTE1	181	UART1 DTE signal - Ring Indicator
SCK4	54	Audio Port 4 - Serial clock
SCK5	58	Audio Port 5 - Serial clock
SD1_CLK	31	SD/MMC CLOCK — Clock output to SD/MMC card
SD1_CMD	33	SD/MMC COMMAND — Serial command bit to SD/MMC card, bidirectional
SD1_DATA0	21	SD/MMC DATA BIT 0 — Serial data bit to SD/MMC card, bidirectional
SD1_DATA1	23	SD/MMC DATA BIT 1 — Serial data to SD/MMC card, bidirectional
SD1_DATA2	25	SD/MMC DATA BIT 2 — Serial data to SD/MMC card, bidirectional
SD1_DATA3	27	SD/MMC DATA BIT 3 — Serial data to SD/MMC card, bidirectional
SFS4	52	Audio Port 4 - Frame Sync
SFS5	62	Audio Port 5 - Frame Sync
SRXD4	50	Audio Port 4 - Receive Data
SRXD5	60	Audio Port 5 - Receive Data
STXD4	48	Audio Port 4 - Transmit Data
STXD5	64	Audio Port 5 - Transmit Data
UART1_CTS	172	UART1 CLEAR TO SEND

Table 4-2. Base Board to CPU Board Connector P1 Signal Description (continued)

Signal	Pin	Description
UART1_RTS	170	UART1 REQUEST TO SEND
UART1_RXD	176	UART1 RECEIVED DATA
UART1_TXD	174	UART1 TRANSMITTED DATA
UART2_CTS	182	UART2 CLEAR TO SEND
UART2_RTS	180	UART2 REQUEST TO SEND
UART2_RXD	186	UART2 RECEIVED DATA
UART2_TXD	184	UART2 TRANSMITTED DATA
USB_BYP	68	USB BYPASS
USB_OC	70	USB OUTPUT CONTROL
USB_PWR	72	USB POWER
USBOTG_CLK	57	USB OTG CLOCK
USBOTG_DATA0	61	USB OTG DATA
USBOTG_DATA1	63	USB OTG DATA
USBOTG_DATA2	65	USB OTG DATA
USBOTG_DATA3	67	USB OTG DATA
USBOTG_DATA4	69	USB OTG DATA
USBOTG_DATA5	71	USB OTG DATA
USBOTG_DATA6	73	USB OTG DATA
USBOTG_DATA7	75	USB OTG DATA
USBOTG_DIR	53	USB OTG DIRECTION
USBOTG_NXT	55	USB OTG NEXT
USBOTG_STP	51	USB OTG STOP
VSD1	17, 19	CONDITIONED POWER SUPPLY FROM PM
VSD2	40, 42	CONDITIONED POWER SUPPLY FROM PM

Table 4-3. Base Board to CPU Board Connector P2 Signal Description

Signal	Pin	Description
3V3	2, 4, 6, 116, 118	3 VDC POWER
ATLAS_IN	186	ATLAS PM INPUT
B_A0	74	BUFFERED ADDRESS — MCU address bus
B_A1	72	BUFFERED ADDRESS — MCU address bus
B_A2	70	BUFFERED ADDRESS — MCU address bus
B_A3	68	BUFFERED ADDRESS — MCU address bus
B_A4	66	BUFFERED ADDRESS — MCU address bus
B_A5	62	BUFFERED ADDRESS — MCU address bus
B_A6	60	BUFFERED ADDRESS — MCU address bus
B_A7	58	BUFFERED ADDRESS — MCU address bus
B_A8	56	BUFFERED ADDRESS — MCU address bus
B_A9	54	BUFFERED ADDRESS — MCU address bus
B_A10	50	BUFFERED ADDRESS — MCU address bus
B_A11	48	BUFFERED ADDRESS — MCU address bus
B_A12	46	BUFFERED ADDRESS — MCU address bus
B_A13	44	BUFFERED ADDRESS — MCU address bus
B_A14	42	BUFFERED ADDRESS — MCU address bus
B_A15	40	BUFFERED ADDRESS — MCU address bus
B_A16	76	BUFFERED ADDRESS — MCU address bus
B_A17	78	BUFFERED ADDRESS — MCU address bus
B_A18	80	BUFFERED ADDRESS — MCU address bus
B_A19	82	BUFFERED ADDRESS — MCU address bus
B_A20	84	BUFFERED ADDRESS — MCU address bus
B_A21	86	BUFFERED ADDRESS — MCU address bus
B_A22	88	BUFFERED ADDRESS — MCU address bus
B_A23	90	BUFFERED ADDRESS — MCU address bus
B_A24	92	BUFFERED ADDRESS — MCU address bus
B_A25	94	BUFFERED ADDRESS — MCU address bus
B_D0	8	BUFFERED DATA — MCU data bus
B_D1	10	BUFFERED DATA — MCU data bus
B_D2	12	BUFFERED DATA — MCU data bus
B_D3	14	BUFFERED DATA — MCU data bus
B_D4	16	BUFFERED DATA — MCU data bus
B_D5	18	BUFFERED DATA — MCU data bus
B_D6	20	BUFFERED DATA — MCU data bus
B_D7	22	BUFFERED DATA — MCU data bus
B_D8	24	BUFFERED DATA — MCU data bus
B_D9	26	BUFFERED DATA — MCU data bus
B_D10	28	BUFFERED DATA — MCU data bus
B_D11	30	BUFFERED DATA — MCU data bus
B_D12	32	BUFFERED DATA — MCU data bus
B_D13	34	BUFFERED DATA — MCU data bus
B_D14	36	BUFFERED DATA — MCU data bus

Table 4-3. Base Board to CPU Board Connector P2 Signal Description (continued)

Signal	Pin	Description
B_D15	38	BUFFERED DATA — MCU data bus
BBCLK	85	BASE BOARD CLOCK
BCS0_B	113	BUFFERED CHIP SELECT
BCS1_B	111	BUFFERED CHIP SELECT
BCS4_B	98	BUFFERED CHIP SELECT
BCS5_B	109	BUFFERED CHIP SELECT
BEB0_B	100	BUFFERED BITE ENABLE
BEB1_B	102	BUFFERED BITE ENABLE
BLBA_B	95	BUFFERED LOAD BASE ADDRESS
BOE_B	104	BUFFERED OUTPUT ENABLE
BPC_POE	114	PCMCIA OUTPUT ENABLE
BRW_B	106	BUFFERED READ/WRITE
CARD1_SEL_B	144	MEMORY STICK1 CARD SELECT
CARD2_SEL_B	142	MEMORY STICK2 CARD SELECT
CLKO	162	CLOCK OUT
CPU_BRD_VER0	99	CPU BOARD VERSION
CPU_BRD_VER1	101	CPU BOARD VERSION
CPU_BRD_VER2	103	CPU BOARD VERSION
CPU_BRD_VER3	105	CPU BOARD VERSION
CSPI1_MISO	27	MASTER IN / SLAVE OUT — CSPI data signal (bidirectional)
CSPI1_MOSI	29	MASTER OUT / SLAVE IN — CSPI data signal (bidirectional)
CSPI1_SCLK	25	SERIAL CLOCK — Bidirectional
CSPI1_SPI_RDY	37	READY — CSPI serial burst trigger, active low input
CSPI1_SS0	35	SLAVE SELECT 0 — CSPI signal (bidirectional)
CSPI1_SS1	33	SLAVE SELECT 1 — CSPI signal (bidirectional)
CSPI1_SS2	31	SLAVE SELECT 2 — CSPI signal (bidirectional)
CVDD_2.775V	153, 155	2.775 VDC SUPPLY
CVDD_2.7V	91, 93	2.7 VDC SUPPLY
DVDD_1.8V	77, 79, 188, 190	1.8 VDC SUPPLY
DVS_SW1A	165	CONDITIONED POWER SUPPLY FROM PM
DVS_SW1B	161	CONDITIONED POWER SUPPLY FROM PM
DVS_SW2A	163	CONDITIONED POWER SUPPLY FROM PM
DVS_SW2B	159	CONDITIONED POWER SUPPLY FROM PM
GND	13, 23, 52, 64, 57, 61, 83, 87, 96, 97, 107, 135, 136, 138, 160, 164, 175, 180, 191- 215	SIGNAL GROUND
GPIO1_0	166	GENERAL PURPOSE I/O
GPIO1_1	168	GENERAL PURPOSE I/O
GPIO1_2	170	GENERAL PURPOSE I/O
GPIO1_3	172	GENERAL PURPOSE I/O
GPIO1_4	174	GENERAL PURPOSE I/O

Table 4-3. Base Board to CPU Board Connector P2 Signal Description (continued)

Signal	Pin	Description
GPIO1_5	176	GENERAL PURPOSE I/O
GPIO1_6	178	GENERAL PURPOSE I/O
KPCOL0	119	KEYPAD COLUMN SELECT
KPCOL1	121	KEYPAD COLUMN SELECT
KPCOL2	123	KEYPAD COLUMN SELECT
KPCOL3	125	KEYPAD COLUMN SELECT
KPCOL4	127	KEYPAD COLUMN SELECT
KPCOL5	129	KEYPAD COLUMN SELECT
KPCOL6	131	KEYPAD COLUMN SELECT
KPCOL7	133	KEYPAD COLUMN SELECT
KPROW0	120	KEYPAD ROW SELECT
KPROW1	122	KEYPAD ROW SELECT
KPROW2	124	KEYPAD ROW SELECT
KPROW3	126	KEYPAD ROW SELECT
KPROW4	128	KEYPAD ROW SELECT
KPROW5	130	KEYPAD ROW SELECT
KPROW6	132	KEYPAD ROW SELECT
KPROW7	134	KEYPAD ROW SELECT
M_GRNT	184	EMI CONTROL SIGNAL - MASTER GRANT
M_RQST	182	EMI CONTROL SIGNAL - MASTER REQUEST
MSHC2_DET	146	MEMORY STICK 2 DETECT
MSHC1_DET	148	MEMORY STICK 1 DETECT
NC	43, 49, 81, 89, 140	NOT CONNECTED
NF_DET_B	158	NAND FLASH DETECT
NVCC1	187, 189	CONDITIONED POWER SUPPLY
NVCC2	1, 3, 5	CONDITIONED POWER SUPPLY
NVCC6	115, 117	CONDITIONED POWER SUPPLY
NVCC9	149, 151	CONDITIONED POWER SUPPLY
PC_CE1_B	108	PCMCIA CARD ENABLE1
PC_CE2_B	110	PCMCIA CARD ENABLE2
PC_OE_B	112	PCMCIA OUTPUT ENABLE
PC_POE	71	PCMCIA OUTPUT ENABLE
PM_BKUP_DDR	39	POWER MANAGEMENT DDR BACKUP
PM_BKUP_DDR	41	POWER MANAGEMENT DDR BACKUP
PM_CLK32K_MCU	177	POWER MANAGEMENT BOARD 32 KHz MCU CLOCK
PM_MEM_CS	185	POWER MANAGEMENT MEMORY CHIP SELECT
PM_RST_B	173	POWER MANAGEMENT RESET
PM_RSTMCU_B	183	POWER MANAGEMENT MCU RESET
PM_SW1A	67	POWER MANAGEMENT
PM_SW1A	69	POWER MANAGEMENT
PM_VDIG	154	POWER MANAGEMENT
PM_VDIG	156	POWER MANAGEMENT
PM_VGEN	150	POWER MANAGEMENT
PM_VGEN	152	POWER MANAGEMENT
PWGT1_EN	157	POWER GATE 1 ENABLE

Table 4-3. Base Board to CPU Board Connector P2 Signal Description (continued)

Signal	Pin	Description
PWGT1_OUT	73	POWER MANAGEMENT
PWGT1_OUT	75	POWER MANAGEMENT
PWGT2_EN	169	POWER GATE 2 ENABLE
PWGT2_OUT	45	POWER MANAGEMENT
PWGT2_OUT	47	POWER MANAGEMENT
PWR_FAIL	181	POWER FAILURE
RST_OUT_B	167	RESET OUT — Active low reset signal from the MCU
SCK3	15	Audio Port 3 - Serial clock
SCK6	11	Audio Port 6 - Serial clock
SCLK0	147	Audio Port 0 - Serial clock
SFS3	19	Audio Port 3 - Frame Sync
SFS6	9	Audio Port 6 - Frame Sync
SIMPD0	145	SIM CARD - PRESENCE DETECT
SRST0	139	Audio Port 0 - RESET
SRXD0	137	Audio Port 0 - RECEIVE DATA
SRXD3	17	Audio Port 3 - RECEIVE DATA
SRXD6	7	Audio Port 6 - RECEIVE DATA
STXD0	143	Audio Port 0 - TRANSMIT DATA
STXD3	21	Audio Port 3 - TRANSMIT DATA
STXD6	5	Audio Port 6 - TRANSMIT DATA
SVEN0	141	SIM CARD VCC Enable Port 0
USBH2_CLK	59	USB HOST CLOCK
USBH2_DATA0	65	USB HOST DATA
USBH2_DATA1	63	USB HOST DATA
USBH2_DIR	55	USB HOST DIRECTION
USBH2_NXT	51	USB HOST NEXT
USBH2_STP	53	USB HOST STOP
VSTBY	171	STANDBY VOLTAGE
WATCHDOG_RST	179	WATCHDOG RESET

4.2.2 Base Board to MC13783 Board Connectors

ADS Base board connectors P5 and P6 mate with MC13783 board connectors J5 and J6 (bottom side). Figure 4-4 shows connector pin assignments. Table 4-5 describe connector signals.

P5

NC	2		1	NC
GND	4		3	GND
NC	6		5	NC
NC	8		7	NC
NC	10		9	NC
NC	12		11	NC
NC	14		13	GND
NC	16		15	NC
NC	18		17	GND
NC	20		19	NC
GND	22		21	NC
NC	24		23	NC
GND	26		25	NC
NC	28		27	NC
NC	30		29	NC
NC	32		31	NC
GND	34		33	PM_VUSB_3V
NC	36		35	PM_VUSB_3V
NC	38		37	PM_VUSB_3V
GND	192		191	GND
GND	194		193	GND
			195	GND
GND	40		39	NC
NC	42		41	NC
NC	44		43	NC
GND	46		45	NC
NC	48		47	NC
NC	50		49	NC
NC	52		51	NC
NC	54		53	PM_VIOLO
NC	56		55	PM_VIOLO
NC	58		57	PM_VIOLO
NC	60		59	NC
NC	62		61	PM_VIOHI
NC	64		63	PM_VIOHI
NC	66		65	PM_VIOHI
NC	68		67	NC
NC	70		69	5V
NC	72		71	5V
NC	74		73	5V
NC	76		75	5V
GND	196			
GND	198		197	GND
GND	200		199	GND
NC	78		77	NC
NC	80		79	GND
NC	82		81	NC
NC	84		83	NC
NC	86		85	NC
NC	88		87	NC
NC	90		89	NC
NC	92		91	NC
NC	94		93	NC
NC	96		95	NC

P6

VIB_EN	2		1	LEDR1
DVS_SW1_B	4		3	LEDR2
LED_MD1	6		5	LEDR3
LED_MD2	8		7	LEDG1
LED_MD3	10		9	LEDG2
LED_MD4	12		11	LEDG3
LED_AD1	14		13	LEDB1
LED_AD2	16		15	LEDB2
LED_KP	18		17	LEDB3
ATLAS_UTX_ENB	20		19	GND
GND	22		21	TSX1
ATLAS_UDATVP	24		23	GND
ATLAS_USE_0VM	26		25	TSX2
GND	28		27	GND
ATLAS_URCVD	30		29	TSY1
GND	32		31	GND
ATLAS_URXVP	34		33	TSY2
ATLAS_URXVM	36		35	GND
ATLAS_IN	38		37	ADIN4
GND	192		191	GND
GND	194		193	GND
			195	GND
PM_VUSB_3V	40		39	ADIN5
PM_VUSB_3V	42		41	GND
PM_RST_B	44		43	ADIN6
VSTBY	46		45	GND
DVS_SW1A	48		47	ADIN7
BB_STBY	50		49	GND
DVS_SW2A	52		51	ADIN8
PM_RSTMCU_B	54		53	GND
PM_VIOLO	56		55	ADIN9
PM_VIOLO	58		57	GND
ADTRIG	60		59	ADIN10
BB_SEC_INT	62		61	GND
PM_VIOHI	64		63	CPU_PRI_VCC
PM_VIOHI	66		65	GND
BB_VCC	68		67	PM_CLK32K_MCU
REGEN	70		69	GND
5V	72		71	PM_INT
5V	74		73	GND
5V	76		75	PM_CLIA
GND	196			
GND	198		197	GND
GND	200		199	GND
DVS_SW2B	78		77	CSPI2_SCLK
GND	80		79	CSPI2_SS0
PM_VDIG	82		81	CSPI2_MOSI
PM_VDIG	84		83	CSPI2_MISO
PM_PWRRDY/GPIO1_1	86		85	NC
GND	88		87	GND
PM_GP01_BUFF	90		89	BB_CSPI_CLK
PWR_FAIL	92		91	BB_CSPI_SS0
USER_OFF/GPIO1_0	94		93	BB_CSPI_MOSI
PM_GP02_BUFF	96		95	BB_CSPI_MISO

NC	98	97	PM_VDIG	PM_VRFDIG	98	97	NC
NC	100	99	PM_VDIG	PM_VRFDIG	100	99	ADOUT
NC	102	101	NC	PM_GP03_BUFF	102	101	LOWBAT
NC	104	103	NC	PM_VESIM	104	103	NC
NC	106	105	NC	PM_VESIM	106	105	PM_VCAM
NC	108	107	NC	CLK0	108	107	PM_VCAM
NC	110	109	NC	PC_CE2_B	110	109	NC
PM_VRF_REF	112	111	OPM_SW1A	PC_OE_B	112	111	PWGT2_OUT
PM_VRF_REF	114	113	OPM_SW1A	BPC_POE	114	113	PWGT2_OUT
GND	202	201	NC	GND	202	201	GND
GND	204	203	GND	GND	204	203	GND
		205	GND			205	GND
NC	116	115	PM_SW1A	PM_SW1A	116	115	PM_VGEN
NC	118	117	PM_SW1A	PM_SW1A	118	117	PM_VGEN
NC	120	119	PM_SW1A	NC	120	119	NC
NC	122	121	PM_SW1A	NC	122	121	NC
NC	124	123	NC	NC	124	123	NC
NC	126	125	NC	NC	126	125	NC
NC	128	127	NC	NC	128	127	NC
NC	130	129	NC	NC	130	129	NC
NC	132	131	NC	CVDD_2.775V	132	131	NC
NC	134	133	NC	CVDD_2.775V	134	133	NC
NC	136	135	NC	NC	136	135	NC
NC	138	137	NC	STXD4	138	137	NC
NC	140	139	NC	SRXD4	140	139	NC
NC	142	141	NC	SFS4	142	141	PM_WDOG_RST
NC	144	143	NC	SCK4	144	143	VSIM_EN
NC	146	145	NC	NC	146	145	GND
NC	148	147	PM_SW1B	NC	148	147	NC
GND	150	149	PM_SW1B	PM_SW1B	150	149	GND
NC	152	151	PM_SW1B	PM_SW1B	152	151	NC
GND	206			GND	206		
GND	208	207	GND	GND	208	207	GND
GND	210	209	GND	GND	210	209	GND
GND	154	153	NC	PM_CLK32K	154	153	STXD5
NC	156	155	GND	GND	156	155	SRXD5
GND	158	157	NC	NVCC2	158	157	SFS5
NC	160	159	NC	PM_SW2A	160	159	SCK5
NC	162	161	GND	PM_SW2A	162	161	NC
NC	164	163	NC	NC	164	163	NC
NC	166	165	NC	PM_SW2B	166	165	PM_VRF1
PM_VRF_CP	168	167	GND	PM_SW2B	168	167	PM_VRF1
NC	170	169	NC	NC	170	169	PWGT1_EN
NC	172	171	GND	PWGT1_OUT	172	171	PM_BP
NC	174	173	NC	PWGT1_OUT	174	173	PM_BP
NC	176	175	NC	NC	176	175	PWGT2_EN
NC	178	177	GND	PM_BKUP_DDR	178	177	VESIM_EN
NC	180	179	NC	PM_BKUP_DDR	180	179	PM_MEM_CS
NC	182	181	NC	ON1_B	182	181	PM_VBLITE
NC	184	183	NC	ON2_B	184	183	PM_VBLITE
NC	186	185	3V3	ON3_B	186	185	NC
NC	188	187	3V3	VSD2	188	187	VSD1
NC	190	189	3V3	VSD2	190	189	VSD1
GND	212	211	GND	GND	212	211	GND
GND	214	213	GND	GND	214	213	GND
		215	GND			215	GND

Figure 4-4. Base Board to MC13783 Board Connectors P5 and P6 Pin Assignment

Table 4-4. Base Board to MC13783 Board Connector P5 Signal Description

Signal	Pin	Description
3V3	185, 187, 189	3 VDC POWER
5V	69, 71, 73, 75	5 VDCPOWER
GND	3, 4, 13, 17, 22, 26, 34, 40, 48, 79, 150, 154, 155, 158, 161, 167, 171, 177, 191 - 215	SIGNAL GROUND
NC	1, 2, 5-12, 14-16, 18-21, 23-25, 27-32, 36, 38, 39, 41-45, 47-52, 54, 56, 58-60, 62, 64, 66-68, 70, 72, 74, 76-78, 80-96, 98, 100-110, 116, 118, 120, 122-146, 148, 152, 153, 156, 157, 159, 160, 162-166, 169, 170, 172-176, 178-184, 186, 188, 190, 201	NOT CONNECTED
PM_SW1A	111, 113, 115, 117, 119, 121	SWITCHER OUTPUT
PM_SW1B	147, 149, 151	SWITCHER OUTPUT
PM_VDIG	97, 99	VOLTAGE REGULATOR OUTPUT
PM_VIOHI	61, 63, 65	VOLTAGE REGULATOR OUTPUT
PM_VIOLO	53, 55, 57	VOLTAGE REGULATOR OUTPUT
PM_VRF_CP	168	VOLTAGE REGULATOR OUTPUT
PM_VRF_REF	112, 114	REGULATOR REFERENCE VOLTAGE
PM_VUSB_3V	33, 36, 37	VOLTAGE REGULATOR OUTPUT

Table 4-5. Base Board to MC13783 Board Connector P6 Signal Description

Signal	Pin	Description
5V	72, 74, 76	5V INPUT
ADIN4	37	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN5	39	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN6	43	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN7	47	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN8	51	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN9	55	GENERAL PURPOSE ANALOG TO DIGITAL INPUT
ADIN10	59	GENERAL PURPOSE ANALOG TO DIGITAL INPUT

Table 4-5. Base Board to MC13783 Board Connector P6 Signal Description (continued)

Signal	Pin	Description
ADOUT	99	GENERAL PURPOSE ANALOG TO DIGITAL OUTPUT
ADTRIG	60	ANALOG TO DIGITAL TRIGGER
ATLAS_IN	38	MC13783 IN INDICATOR
ATLAS_UDATVP	24	USB DATA V PLUS
ATLAS_URCVD	30	USB RECEIVE DATA
ATLAS_URXVM	36	USB RECEIVE MINUS
ATLAS_URXVP	34	USB RECEIVE MINUS
ATLAS_USE_0VM	26	USB SINGLE ENDED ZERO
ATLAS_UTX_ENB	20	USB TRANSMIT ENABLE
BB_CSPI_CLK	89	BASEBAND CONFIGURABLE SERIAL PERIPHERAL INTERFACE CLOCK
BB_CSPI_MISO	95	BASEBAND CONFIGURABLE SERIAL PERIPHERAL INTERFACE MISO
BB_CSPI_MOSI	93	BASEBAND CONFIGURABLE SERIAL PERIPHERAL INTERFACE MOSI
BB_CSPI_SS0	91	BASEBAND CONFIGURABLE SERIAL PERIPHERAL INTERFACE SS0
BB_SEC_INT	62	BASEBAND SECONDERY INTERRUPT
BB_STBY	50	BASEBAND STANDBY
BB_VCC	68	BASEBAND VCC
BPC_POE	114	PCMCIA OUTPUT ENABLE
CLKO	108	CLKOUT
CPU_PRI_VCC	63	CPU PRIMARY VCC
CSPI2_MISO	83	CONFIGURABLE SERIAL PERIPHERAL INTERFACE MISO
CSPI2_MOSI	81	CONFIGURABLE SERIAL PERIPHERAL INTERFACE MOSI
CSPI2_SCLK	77	CONFIGURABLE SERIAL PERIPHERAL INTERFACE CLOCK
CSPI2_SS0	79	CONFIGURABLE SERIAL PERIPHERAL INTERFACE SS0
CVDD_2.775V	132,134	2.775V VDCPOWER
DVS_SW1B	4	DYNAMIC VOLTAGE SCALING INPUT FOR SWITCHER
DVS_SW1A	48	DYNAMIC VOLTAGE SCALING INPUT FOR SWITCHER
DVS_SW2A	52	DYNAMIC VOLTAGE SCALING INPUT FOR SWITCHER
DVS_SW2B	78	DYNAMIC VOLTAGE SCALING INPUT FOR SWITCHER
GND	19, 22, 23, 27, 28, 31, 32, 35, 41, 45, 49, 53, 57, 61, 65, 69, 73, 80, 87, 88, 145, 149, 156, 191-215	SIGNAL GROUND
LED_AD1	14	AUXILARY DISPLAY LIGHT EMMITING DIODE
LED_AD2	16	AUXILARY DISPLAY LIGHT EMMITING DIODE
LED_KP	18	KEYPAD LIGHT EMMITING DIODE
LED_MD1	6	MAIN DISPLAY LIGHT EMMITING DIODE
LED_MD2	8	MAIN DISPLAY LIGHT EMMITING DIODE
LED_MD3	10	MAIN DISPLAY LIGHT EMMITING DIODE
LED_MD4	12	MAIN DISPLAY LIGHT EMMITING DIODE
LEDB1	13	FUNLIGHT LED 1 BLUE SEGMENT
LEDB2	15	FUNLIGHT LED 2 BLUE SEGMENT
LEDB3	17	FUNLIGHT LED 3 BLUE SEGMENT
LEDG1	7	FUNLIGHT LED 1 GREEN SEGMENT
LEDG2	9	FUNLIGHT LED 2 GREEN SEGMENT

Table 4-5. Base Board to MC13783 Board Connector P6 Signal Description (continued)

Signal	Pin	Description
LEDG3	11	FUNLIGHT LED 3 GREEN SEGMENT
LEDR1	1	FUNLIGHT LED 1 RED SEGMENT
LEDR2	3	FUNLIGHT LED 2 RED SEGMENT
LEDR3	5	FUNLIGHT LED 3 RED SEGMENT
LOWBAT	101	LOW BATTERY
NC	85, 97, 103, 109, 119-131, 133, 135-137, 139, 146-148, 151, 161, 163, 164, 170, 176, 185	NOT CONNECTED
NVCC2	158	VOLTAGE REGULATOR OUTPUT
ON1_B	182	MC13783 POWER ON/OFF BUTTON
ON2_B	184	MC13783 POWER ON/OFF BUTTON
ON3_B	186	MC13783 POWER ON/OFF BUTTON
PC_CE2_B	110	PCMCIA CARD ENABLE
PC_OE_B	112	PCMCIA OUTPUT ENABLE
PM_BKUP_DDR	178, 180	VOLTAGE REGULATOR OUTPUT
PM_BP	171, 173	BATTERY POWER
PM_CLIA	75	CLOCK INPUT
PM_CLK32K	154	32KHZ CLOCK OUTPUT
PM_CLK32K_MCU	67	32KHZ CLOCK OUTPUT TO THE PROCESSOR
PM_GPO1_BUFF	90	GENERAL PURPOSE OUTPUT
PM_GPO2_BUFF	96	GENERAL PURPOSE OUTPUT
PM_GPO3_BUFF	102	GENERAL PURPOSE OUTPUT
PM_INT	71	INTERRUPT
PM_MEM_CS	179	MEMORY CHIP SELECT
PM_PWRRDY	86	POWER READY
PM_RST_B	44	RESET SIGNAL
PM_RSTMCU_B	54	RESET SIGNAL to MCU
PM_SW1A	116, 118	SWITCHER OUTPUT
PM_SW1B	150, 152	SWITCHER OUTPUT
PM_SW2A	160, 162	SWITCHER OUTPUT
PM_SW2B	166, 168	SWITCHER OUTPUT
PM_VBLITE	181, 183	VOLTAGE REGULATOR OUTPUT
PM_VCAM	105, 107	VOLTAGE REGULATOR OUTPUT
PM_VDIG	82, 84	VOLTAGE REGULATOR OUTPUT
PM_VESIM	104, 106	VOLTAGE REGULATOR OUTPUT
PM_VGEN	115, 117	VOLTAGE REGULATOR OUTPUT
PM_VIOHI	64, 66	VOLTAGE REGULATOR OUTPUT
PM_VIOLO	56, 58	VOLTAGE REGULATOR OUTPUT
PM_VRF1	165, 167	VOLTAGE REGULATOR OUTPUT
PM_VRFDIG	98,100	VOLTAGE REGULATOR OUTPUT
PM_VUSB_3V	40, 42	VOLTAGE REGULATOR OUTPUT
PM_WDOG_RST	141	WADTCHDOG RESET
PWGT1_EN	169	POWER GATE 1 ENABLE

Table 4-5. Base Board to MC13783 Board Connector P6 Signal Description (continued)

Signal	Pin	Description
PWGT1_OUT	172, 174	POWER GATE 1 OUTPUT
PWGT2_EN	175	POWER GATE 2 ENABLE
PWGT2_OUT	111, 113	POWER GATE 2 OUTPUT
PWR_FAIL	92	POWER FAIL INDICATOR
REGEN	70	REGULATOR ENABLE
SCK4	144	AUDIO PORT 4 - SERIAL CLOCK
SCK5	159	AUDIO PORT 5 - SERIAL CLOCK
SFS4	142	AUDIO PORT 4 - FRAME SYNC
SFS5	157	AUDIO PORT 5 - FRAME SYNC
SRXD4	140	AUDIO PORT 4 - RECEIVE DATA
SRXD5	155	AUDIO PORT 5 - RECEIVE DATA
STXD4	138	AUDIO PORT 4 - TRANSMIT DATA
STXD5	153	AUDIO PORT 5 - TRANSMIT DATA
TSX1	21	TOUCHSCREEN X-PLATE
TSX2	25	TOUCHSCREEN X-PLATE
TSY1	29	TOUCHSCREEN Y-PLATE
TSY2	33	TOUCHSCREEN Y-PLATE
USER_OFF	94	USER OFF MODE INPUT
VESIM_EN	177	ESIM REGULATOR ENABLE
VIB_EN	2	VIBRATOR REGULATOR ENABLE
VSD1	187, 189	VOLTAGE REGULATOR OUTPUT
VSD2	188, 190	VOLTAGE REGULATOR OUTPUT
VSIM_EN	143	SIM REGULATOR ENABLE
VSTBY	46	STAND BY INPUT

4.2.3 Image Sensor and Extension Connectors

Connectors J10, J13, J17, J22, and J23 are three-row, 16-pin DIN connectors.

J10 and J13 are connectors for the image sensor module included with the ADS. They are identical except for connector orientation on the Base board. J10 is horizontal, while J13 is vertical.

Extension connectors J17, J22, and J23 provide ADS signals for use with expansion cards and accessories. The connector pin assignments are not identical. J17 and J22 are horizontal, while J23 is vertical.

Figure 4-5 shows pin numbering for these connectors. Table 4-6 describes image sensor connector signals. Table 4-7, Table 4-8, and Table 4-9 describe expansion connector signals.

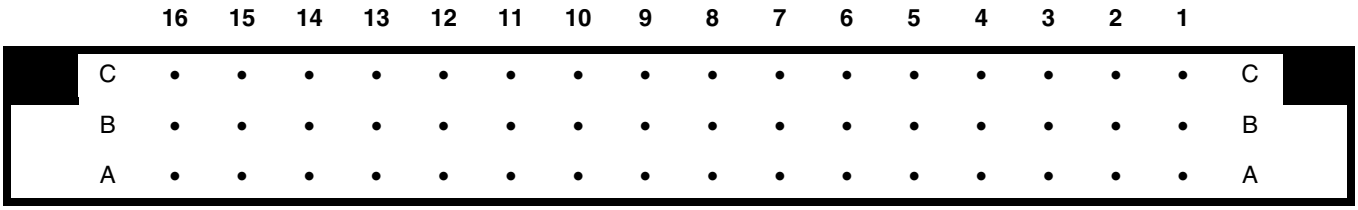


Figure 4-5. Image Sensor and Extension Connector Pin Numbering

Table 4-6. Image Sensor Connectors J10 and J13 Signal Description

Pin	Signal	Description
A1	GND	SIGNAL GROUND
A2	EXT_CSI_D8	CMOS SENSOR INTERFACE DATA 8— Image Sensor input data
A3	EXT_CSI_D10	CMOS SENSOR INTERFACE DATA 10— Image Sensor input data
A4	EXT_CSI_D12	CMOS SENSOR INTERFACE DATA 12— Image Sensor input data
A5	EXT_CSI_D14	CMOS SENSOR INTERFACE DATA 14— Image Sensor input data
A6	EXT_CSI_PIXCLK	CMOS SENSOR INTERFACE PIXEL CLOCK — Data latch strobe
A7	EXT_CSI_VSYNC	CMOS SENSOR INTERFACE VERTICAL SYNC — Control input
A8	CSI_SCL	CMOS SENSOR INTERFACE SERIAL CLOCK — Serial clock, bidirectional
A9	CSI_CS1	CMOS SENSOR INTERFACE CHIP SELECT 1 — Control signal (bidirectional)
A10	CSI_CS2	CMOS SENSOR INTERFACE CHIP SELECT 2 — Control signal (bidirectional)
A11	NC	NO CONNECTION
A12	NC	NO CONNECTION
A13	NC	NO CONNECTION
A14	B14	Wired connection
A15	NC	NO CONNECTION
A16	3V3	+3 VDC power
B1	GND	SIGNAL GROUND
B2	NC	NO CONNECTION
B3	NC	NO CONNECTION
B4	EXT_CSI_D2	CMOS SENSOR INTERFACE DATA 2— Image Sensor input data
B5	EXT_CSI_D3	CMOS SENSOR INTERFACE DATA 3— Image Sensor input data
B6	EXT_CSI_D4	CMOS SENSOR INTERFACE DATA 4— Image Sensor input data
B7	EXT_CSI_D5	CMOS SENSOR INTERFACE DATA 5— Image Sensor input data
B8	EXT_CSI_D6	CMOS SENSOR INTERFACE DATA 6— Image Sensor input data
B9	PM_VCAM	POWER MANAGER VIDEO CAMERA
B10	PM_VCAM	POWER MANAGER VIDEO CAMERA
B11	EXT_CSI_D7	CMOS SENSOR INTERFACE DATA 7— Image Sensor input data
B12	DVDD_1.8V	POWER SUPPLY
B13	EXT_CSI_D1	CMOS SENSOR INTERFACE DATA 1— Image Sensor input data
B14	A14	Wired connection
B15	EXT_CSI_D0	CMOS SENSOR INTERFACE DATA0 — Image Sensor input data
B16	3V3	+3 VDC POWER
C1	GND	SIGNAL GROUND
C2	EXT_CSI_D9	CMOS SENSOR INTERFACE DATA 9— Image Sensor input data
C3	EXT_CSI_D11	CMOS SENSOR INTERFACE DATA 11— Image Sensor input data
C4	EXT_CSI_D13	CMOS SENSOR INTERFACE DATA 13 — Image Sensor input data

Table 4-6. Image Sensor Connectors J10 and J13 Signal Description (continued)

Pin	Signal	Description
C5	EXT_CSI_D15	CMOS SENSOR INTERFACE DATA 15— Image Sensor input data
C6	EXT_CSI_HSYNC	CMOS SENSOR INTERFACE HORIZONTAL SYNC— Control input
C7	EXT_CSI_MCLK	CMOS SENSOR INTERFACE MASTER CLOCK — Clock output to the sensor card
C8	CSI_SDA	CMOS SENSOR INTERFACE SERIAL DATA — Serial data, bidirectional
C9	CSI_EN	CMOS SENSOR INTERFACE ENABLE
C10	CSI_CTL0	CMOS SENSOR CONTROL 0 — Control output from MM I/O
C11	CSI_CTL1	CMOS SENSOR CONTROL 1 — Control output from MM I/O
C12	CSI_CTL2	CMOS SENSOR CONTROL 2 — Control output from MM I/O
C13	NC	NO CONNECTION
C14	CVDD_2.775V	CONDITIONED POWER SUPPLY
C15	NC	NO CONNECTION
C16	3V3	+3 VDC POWER

Table 4-7. Extension Connector J17 Signal Description

Pin	Signal	Description
A1	R_SD1_CLK	SD/MMC CLOCK — Clock output to SD/MMC card
A2	R_SD1_CMD	SD/MMC COMMAND — Serial command bit to SD/MMC card, bidirectional
A3	R_SD1_DATA3	SD/MMC DATA BIT 3 — Serial data bit to SD/MMC card, bidirectional
A4	R_SD1_DATA2	SD/MMC DATA BIT 2 — Serial data bit to SD/MMC card, bidirectional
A5	R_SD1_DATA1	SD/MMC DATA BIT 1 — Serial data bit to SD/MMC card, bidirectional
A6	R_SD1_DATA0	SD/MMC DATA BIT 0 — Serial data bit to SD/MMC card, bidirectional
A7	UART1_RTS	UART1 REQUEST TO SEND — Active low input signal
A8	UART1_CTS	UART1 CLEAR TO SEND — Active low output signal
A9	UART1_RXD	UART1 RECEIVED DATA — Serial input signal
A10	UART1_TXD	UART1 TRANSMITTED DATA — Serial output signal
A11	UART2_RTS	UART2 REQUEST TO SEND — Active low input signal
A12	UART2_CTS	UART2 CLEAR TO SEND — Active low output signal
A13	UART2_RXD	UART2 RECEIVED DATA — Serial input signal
A14	UART2_TXD	UART2 TRANSMITTED DATA — Serial output signal
A15	KPROW7	KEYPAD ROW 7 — Bidirectional signal used to scan a keypad
A16	KPROW6	KEYPAD ROW 6 — Bidirectional signal used to scan a keypad
B1	KPROW5	KEYPAD ROW 5 — Bidirectional signal used to scan a keypad
B2	KPROW4	KEYPAD ROW 4 — Bidirectional signal used to scan a keypad
B3	KPROW3	KEYPAD ROW 3 — Bidirectional signal used to scan a keypad
B4	KPROW2	KEYPAD ROW 2 — Bidirectional signal used to scan a keypad
B5	KPROW1	KEYPAD ROW 1 — Bidirectional signal used to scan a keypad
B6	KPROW0	KEYPAD ROW 0 — Bidirectional signal used to scan a keypad
B7	KPCOL5	KEYPAD COLUMN 5 — Bidirectional signal used to scan a keypad
B8	KPCOL4	KEYPAD COLUMN 4 — Bidirectional signal used to scan a keypad
B9	KCOL3	KEYPAD COLUMN 3 — Bidirectional signal used to scan a keypad

Table 4-7. Extension Connector J17 Signal Description (continued)

Pin	Signal	Description
B10	KPCOL2	KEYPAD COLUMN 2 — Bidirectional signal used to scan a keypad
B11	KPCOL1	KEYPAD COLUMN 1 — Bidirectional signal used to scan a keypad
B12	KPCOL0	KEYPAD COLUMN 0 — Bidirectional signal used to scan a keypad
B13	SRXD4	SYCHRONOUS AUDIO PORT RECEIVED DATA — serial data input
B14	SFS4	SYCHRONOUS AUDIO PORT FRAME SYNC — Bidirectional, output in master mode, input in slave mode
B15	KPCOL7	KEYPAD COLUMN 7 — Bidirectional signal used to scan a keypad
B16	KPCOL6	KEYPAD COLUMN 6 — Bidirectional signal used to scan a keypad
C1	GND	GROUND
C2	R_CSPI1_MOSI	MASTER OUT / SLAVE IN — CSPI data signal (bidirectional)
C3	R_CSPI1_MISO	MASTER IN / SLAVE OUT — CSPI data signal (bidirectional)
C4	R_CSPI1_SCLK	SERIAL CLOCK — Bidirectional
C5	R_CSPI1_SS0	SLAVE SELECT 0 — CSPI signal (bidirectional)
C6	R_CSPI1_SS1	SLAVE SELECT 1 — CSPI signal (bidirectional)
C7	R_CSPI1_SS2	SLAVE SELECT 2 — CSPI signal (bidirectional)
C8	R_CSPI1_RDY	READY — CSPI serial burst trigger, active low input
C9	R_SCK3	SYCHRONOUS SERIAL INTERFACE TRANSMITTER CLOCK — Bidirectional, output in master mode and input in slave mode
C10	R_STXD3	SYCHRONOUS SERIAL INTERFACE TRANSMITTED DATA — Serial output signal
C11	R_SRXD3	SYCHRONOUS SERIAL INTERFACE RECEIVED DATA — Serial input signal
C12	R_SFS3	SYCHRONOUS SERIAL INTERFACE FRAME SYNC
C13	SCK4	SYCHRONOUS AUDIO PORT CLOCK — Serial transmit clock, bidirectional, output in master mode, input in slave mode
C14	R_STXD4	SYCHRONOUS AUDIO PORT TRANMITTED DATA — Serial data output
C15	NC	NOT CONNETED
C16	3V3	+ 3 VDC power

Table 4-8. Extension Connector J22 Signal Description

Pin	Signal	Description
A1	CSPI2_MOSI	MASTER OUT / SLAVE IN — CSPI data signal (bidirectional)
A2	CSPI2_MISO	MASTER IN / SLAVE OUT — CSPI data signal (bidirectional)
A3	CSPI2_SCLK	SERIAL CLOCK — Bidirectional
A4	CSPI2_SS0	SLAVE SELECT 0 — CSPI signal (bidirectional)
A5	CSPI2_SS1	SLAVE SELECT 1 — CSPI signal (bidirectional)
A6	CSPI2_SS2	SLAVE SELECT 2 — CSPI signal (bidirectional)
A7	I2C1_CLK	I SQUARED C CLOCK — Serial clock, bidirectional
A8	I2C1_DAT	I SQUARED C DATA — Serial data, bidirectional
A9	SCK5	SYCHRONOUS SERIAL INTERFACE TRANSMITTER CLOCK — Bidirectional, output in master mode and input in slave mode
A10	STXD5	SYCHRONOUS SERIAL INTERFACE TRANSMITTED DATA — Serial output signal
A11	SRXD5	SYCHRONOUS SERIAL INTERFACE RECEIVED DATA — Serial input signal
A12	SFS5	SYCHRONOUS SERIAL INTERFACE FRAME SYNC
A13	SCK6	SYCHRONOUS SERIAL INTERFACE TRANSMITTER CLOCK — Bidirectional, output in master mode and input in slave mode
A14	R_STXD6	SYCHRONOUS SERIAL INTERFACE TRANSMITTED DATA — Serial output signal
A15	R_SRXD6	SYCHRONOUS SERIAL INTERFACE RECEIVED DATA — Serial input signal
A16	R_SFS6	SYCHRONOUS SERIAL INTERFACE FRAME SYNC
B1	USBGOTG_DATA3	USB OTG DATA 3
B2	USBGOTG_DATA4	USB OTG DATA 4
B3	USBGOTG_DATA1	USB OTG DATA 1
B4	USBGOTG_DATA2	USB OTG DATA 2
B5	USBGOTG_DATA0	USB OTG DATA 0
B6	USBGOTG_DATA6	USB OTG DATA 6
B7	USBGOTG_DATA7	USB OTG DATA 7
B8	USBGOTG_DATA5	USB OTG DATA 5
B9	R_PC_RST	PCMCIA RESET signal
B10	R_PC_BVD2	PCMCIA Battery Voltage Detect 2
B11	R_PC_BVD1	PCMCIA Battery Voltage Detect 1
B12	R_PC_VS2	PCMCIA Voltage Sense 2 signal
B13	R_USBH2_DATA1	USB HOST DATA 1
B14	R_IOIS16	PCMCIA control signal
B15	R_USBH2_DATA0	USB HOST DATA 0
B16	R_PC_RW_B	PCMCIA READ/WRITE signal
C1	GND	GROUND
C2	CAPTURE	TIMER INPUT CAPTURE — Timer input
C3	COMPARE	TIMER OUTPUT COMPARE — Timer output
C4	R_PC_CD2_B	PCMCIA Card Detect 2
C5	R_PC_CD1_B	PCMCIA Card Detect 1

Table 4-8. Extension Connector J22 Signal Description (continued)

Pin	Signal	Description
C6	R_PC_PWRON	PCMCIA POWER ON SIGNAL
C7	R_PC_VS1	PCMCIA Voltage Sense 1 signal
C8	R_PC_RDY	PCMCIA READY signal
C9	R_PC_WAIT_B	PCMCIA WAIT signal
C10	PWMO	PULSE WIDTH MODULATOR OUTPUT
C11	RST_OUT_B	RESET OUT — Active low reset signal from the processor
C12	NC	NO CONNECTION
C13	USB_OC	USB OVER CURRENT input active low
C14	USB_PWR	USB POWER
C15	USB_BYP	USB BY PASS
C16	VCC	+3 VDC power

Table 4-9. Extension Connector J23 Signal Description

Pin	Signal	Description
A1	GND	SIGNAL GROUND
A2	NC	NO CONNECTION
A3	NC	NO CONNECTION
A4	NC	NO CONNECTION
A5	CPLD_SP4	CUSTOM PROGRAMMED LOGIC DEVICE SP 4
A6	CPLD_SP3	CUSTOM PROGRAMMED LOGIC DEVICE SP 3
A7	CPLD_SP2	CUSTOM PROGRAMMED LOGIC DEVICE SP 2
A8	CPLD_SP1	CUSTOM PROGRAMMED LOGIC DEVICE SP 1
A9	DSR_DTE1	UART1 DTE signal - DSR
A10	RI_DTE1	UART1 DTE signal - Ring Indicator
A11	DCD_DTE1	UART1 DTE signal - DCD
A12	DTR_DCE2	UART2 DCE signal - DTR
A13	NC	NO CONNECTION
A14	CSP12_SPI_RDY	SERIAL PERIPHERAL INTERFACE READY
A15	NC	NO CONNECTION
A16	NC	NO CONNECTION
B1	NC	NO CONNECTION
B2	SCLK0	SERIAL CLOCK 0
B3	SRST0	SERIAL RESET 0
B4	SVEN0	SERIAL ENABLE 0
B5	STX0	SERIAL TRANSMIT 0
B6	CPLD_SP0	CUSTOM PROGRAMMED LOGIC DEVICE SP 0
B7	SIMPD0	SIM CARD PRESENCE DETECT
B8	GPIO1_0	GENERAL PURPOSE I/O PORT 1 LINE 0

Table 4-9. Extension Connector J23 Signal Description (continued)

Pin	Signal	Description
B9	GPIO1_1	GENERAL PURPOSE I/O PORT 1 LINE 1
B10	GPIO1_2	GENERAL PURPOSE I/O PORT 1 LINE 2
B11	GPIO1_3	GENERAL PURPOSE I/O PORT 1 LINE 3
B12	GPIO1_4	GENERAL PURPOSE I/O PORT 1 LINE 4
B13	GPIO1_5	GENERAL PURPOSE I/O PORT 1 LINE 5
B14	GPIO1_6	GENERAL PURPOSE I/O PORT 1 LINE 6
B15	GPIO3_0	GENERAL PURPOSE I/O PORT 3 LINE 0
B16	GPIO3_1	GENERAL PURPOSE I/O PORT 3 LINE 1
C1	GND	GROUND
C2	NC	NO CONNECTION
C3	NC	NO CONNECTION
C4	NC	NO CONNECTION
C5	NC	NO CONNECTION
C6	NC	NO CONNECTION
C7	NC	NO CONNECTION
C8	NC	NO CONNECTION
C9	NC	NO CONNECTION
C10	OWDAT	One Wire Data signal
C11	RST_OUT_B	RESET OUT — Active low reset signal from the processor
C12	DTR_DCE1	UART1 DCE signal - DTR
C13	DSR_DCE1	UART1 DCE signal - DSR
C14	RI_DCE1	UART1 DCE signal - Ring Indicator
C15	DCD_DCE1	UART1 DCE signal - DCD
C16	3V3	+3 VDC power

4.2.4 External Keypad Connector

P5 is a connector for the ADS external keypad. Figure 4-6 shows pin assignments and Table 4-10 describes connector signals.

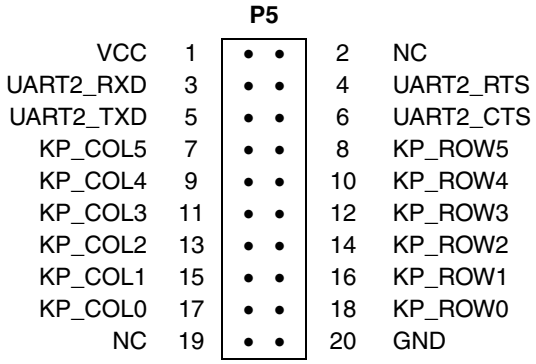


Figure 4-6. External Keypad Connector P5 Pin Assignment

Table 4-10. External Keypad Connector P5 Signal Description

Pin	Signal	Description
1	VCC	+3 volt power
2	NC	NO CONNECTION
3	UART2_RXD *KEY_COL7*	KEYPAD COLUMN 7 — Bidirectional signal used to scan a keypad
4	UART2_RTS *KEY_ROW6*	KEYPAD ROW 6 — Bidirectional signal used to scan a keypad
5	UART2_TXD *KEY_COL6*	KEYPAD COLUMN 6 — Bidirectional signal used to scan a keypad
6	UART2_CTS *KEY_ROW7*	KEYPAD ROW 7 — Bidirectional signal used to scan a keypad
7	KP_COL5	KEYPAD COLUMN 5 — Bidirectional signal used to scan a keypad
8	KP_ROW5	KEYPAD ROW 5 — Bidirectional signal used to scan a keypad
9	KP_COL4	KEYPAD COLUMN 4 — Bidirectional signal used to scan a keypad
10	KP_ROW4	KEYPAD ROW 4 — Bidirectional signal used to scan a keypad
11	KP_COL3	KEYPAD COLUMN 3 — Bidirectional signal used to scan a keypad
12	KP_ROW3	KEYPAD ROW 3 — Bidirectional signal used to scan a keypad
13	KP_COL2	KEYPAD COLUMN 2 — Bidirectional signal used to scan a keypad
14	KP_ROW2	KEYPAD ROW 2 — Bidirectional signal used to scan a keypad
15	KP_COL1	KEYPAD COLUMN 1 — Bidirectional signal used to scan a keypad
16	KP_ROW1	KEYPAD ROW 1 — Bidirectional signal used to scan a keypad
17	KP_COL0	KEYPAD COLUMN 0 — Bidirectional signal used to scan a keypad
18	KP_ROW0	KEYPAD ROW 0 — Bidirectional signal used to scan a keypad
19	NC	NO CONNECTION
20	GND	GROUND

* The signal name in italics is the function intended for operation with this connector. It is multiplexed in the i.MX31 processor with the listed signal.

4.2.5 Display Connectors

4.2.5.1 Synchronous LCD Connector

J12 is a connector for a synchronous serial LCD panel interface. Figure 4-7 shows pin assignments and Table 4-11 describes connector signals.

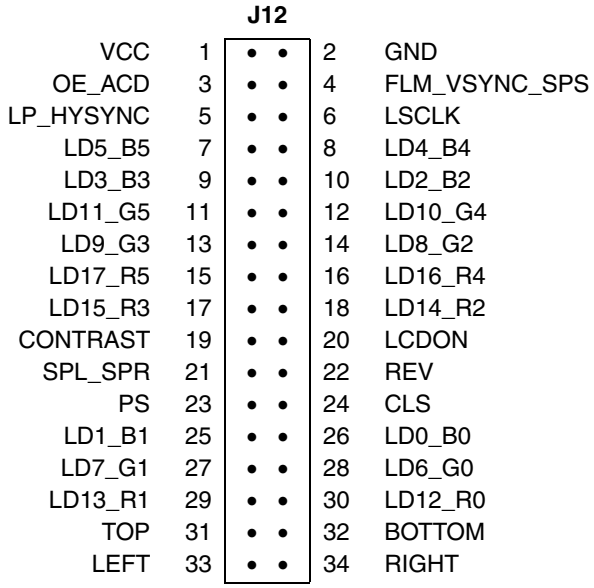


Figure 4-7. Synchronous LCD Connector J12 Pin Assignment

Table 4-11. Synchronous LCD Connector J12 Signal Description

Pin	Signal	Description
1	VCC	3 VDC POWER
2	GND	SIGNAL GROUND
3	OE_ACD	OUTPUT ENABLE / ALTERNATE CRYSTAL DIRECTION
4	FLM_VSYNC_SPS	FIRST LINE MARKER / VERTICAL SYNCHRONIZATION
5	LP_HSYNC	LINE PULSE / HORIZONTAL SYNCHRONIZATION
6	LSCLK	LCD SHIFT CLOCK — Output to LCD
7	LD5_B5	LCD DATA 5 / BLUE BIT 5 — Output data to LCD
8	LD4_B4	LCD DATA 4 / BLUE BIT 4 — Output data to LCD
9	LD3_B3	LCD DATA 3 / BLUE BIT 3 — Output data to LCD
10	LD2_B2	LCD DATA 2 / BLUE BIT 2 — Output data to LCD
11	LD11_G5	LCD DATA 11 / GREEN BIT 5 — Output data to LCD
12	LD10_G4	LCD DATA 10 / GREEN BIT 4 — Output data to LCD
13	LD9_G3	LCD DATA 9 / GREEN BIT 3 — Output data to LCD
14	LD8_G2	LCD DATA 8 / GREEN BIT 2 — Output data to LCD
15	LD17_R5	LCD DATA 17 / RED BIT 5 — Output data to LCD
16	LD16_R4	LCD DATA 16 / RED BIT 4 — Output data to LCD
17	LD15_R3	LCD DATA 15 / RED BIT 3 — Output data to LCD
18	LD14_R2	LCD DATA 14 / RED BIT 2 — Output data to LCD

Table 4-11. Synchronous LCD Connector J12 Signal Description (continued)

Pin	Signal	Description
19	CONTRAST	LCD bias voltage used as contrast control
20	LCDON	LCD enable — Active High, Enables the Sharp LCD
21	SPL_SPR	SAMPLING LEFT to RIGHT— Horizontal scan direction
22	REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal)
23	PS	Control signal output for source driver (Sharp panel dedicated signal)
24	CLS	Start signal output for gate driver. This signal is inverted version of PS (Sharp panel dedicated signal)
25	LD1_B1	LCD DATA 1 / BLUE BIT 1 — Output data to LCD
26	LD0_B0	LCD DATA 0 / BLUE BIT 0 — Output data to LCD
27	LD7_G1	LCD DATA 7 / GREEN BIT 1 — Output data to LCD
28	LD6_G0	LCD DATA 6 / GREEN BIT 0 — Output data to LCD
29	LD13_R1	LCD DATA 13 / RED BIT 1 — Output data to LCD
30	LD12_R0	LCD DATA 12 / RED BIT 0 — Output data to LCD
31	TOP	Negative pen-Y analog input
32	BOTTOM	Positive pen-Y analog input
33	LEFT	Negative pen-X analog input
34	RIGHT	Positive pen-X analog input

4.2.5.2 Option Connector

Connector J11 provides optional LCD panel control signals. Figure 4-8 shows connector pin assignments and Table 4-12 describes connector signals.

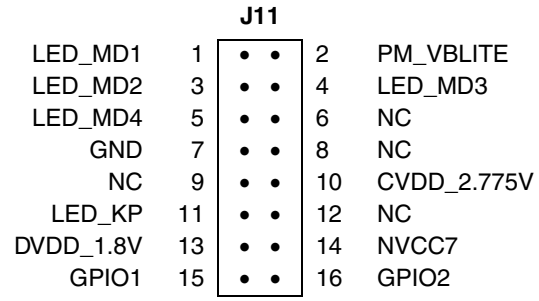


Figure 4-8. Option Connector J11 Pin Assignment

Table 4-12. Option Connector J11 Signal Description

Pin	Signal	Description
1	LED_MD1	MAIN DISPLAY LIGHT EMMITING DIODE
2	PM_VBLITE	LCD PANEL BACKLIGHT VOLTAGE
3	LED_MD2	MAIN DISPLAY LIGHT EMMITING DIODE
4	LED_MD3	MAIN DISPLAY LIGHT EMMITING DIODE
5	LED_MD4	MAIN DISPLAY LIGHT EMMITING DIODE
6	NC	NOT CONNECTED
7	GND	SIGNAL GROUND
8	NC	NOT CONNECTED
9	NC	NOT CONNECTED
10	CVDD_2.775V	2.775 VDC SUPPLY
11	LED_KP	KEYPAD LIGHT EMMITING DIODE
12	NC	NOT CONNECTED
13	DVDD_1.8V	1.8 VDC SUPPLY
14	NVCC7	5 VDC SUPPLY
15	GPIO1	GENERAL PURPOSE I/O LINE 1
16	GPIO2	GENERAL PURPOSE I/O LINE 2

4.2.5.3 Parallel LCD Connectors

Connectors J8 and J9 provide parallel interface signals for LCD panels. J9 is Parallel Connector I and J8 is Parallel connector II. Figure 4-9 shows J9 pin assignments and Table 4-13 describes J9 signals. Figure 4-10 shows J8 pin assignments and Table 4-14 describes J8 signals.

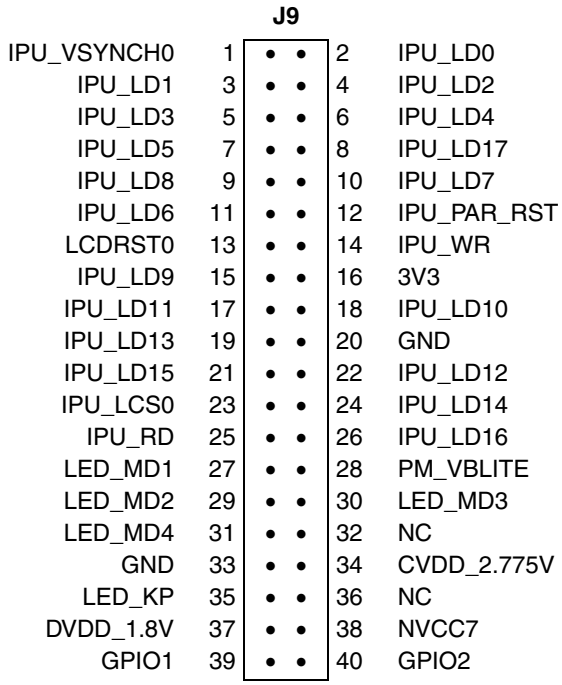


Figure 4-9. Parallel LCD Connector I J9 Pin Assignment

Table 4-13. Parallel LCD Connector I J9 Signal Description

Pin	Signal	Description
1	IPU_VSYNCH0	VERTICAL SYNCH 0
2	IPU_LD0	LCD DATA 0
3	IPU_LD1	LCD DATA 1
4	IPU_LD2	LCD DATA 2
5	IPU_LD3	LCD DATA 3
6	IPU_LD4	LCD DATA 4
7	IPU_LD5	LCD DATA 5
8	IPU_LD17	LCD DATA 17
9	IPU_LD8	LCD DATA 8
10	IPU_LD7	LCD DATA 7
11	IPU_LD6	LCD DATA 6
12	IPU_PAR_RESET	PARALLEL INTERFACE RESET
13	LCDRST0	LCD RESET 0
14	IPU_WR	PARALLEL INTERFACE WRITE
15	IPU_LD9	LCD DATA 9
16	3V3	3 VDC SUPPLY
17	IPU_LD11	LCD DATA 11
18	IPU_LD10	LCD DATA 10
19	IPU_LD13	LCD DATA 13
20	GND	SIGNAL GROUND
21	IPU_LD15	LCD DATA 15
22	IPU_LD12	LCD DATA 12
23	IPU_LCS0	LCD CHIP SELECT
24	IPU_LD14	LCD DATA 14
25	IPU_RD	PARALLEL INTERFACE READ
26	IPU_LD16	LCD DATA 16
27	LED_MD1	MAIN DISPLAY LIGHT EMMITING DIODE
28	PM_VBLITE	LCD PANEL BACKLIGHT VOLTAGE
29	LED_MD2	MAIN DISPLAY LIGHT EMMITING DIODE
30	LED_MD3	MAIN DISPLAY LIGHT EMMITING DIODE
31	LED_MD4	MAIN DISPLAY LIGHT EMMITING DIODE
32	NC	NOT CONNECTED
33	GND	SIGNAL GROUND
34	CVDD_2.775V	2.775 VDC SUPPLY
35	LED_KP	KEYPAD LIGHT EMMITING DIODE
36	NC	NOT CONNECTED
37	DVDD_1.8V	1.8 VDC SUPPLY
38	NVCC7	5 VDC SUPPLY
39	GPIO1	GENERAL PURPOSE I/O LINE 1
40	GPIO2	GENERAL PURPOSE I/O LINE 2

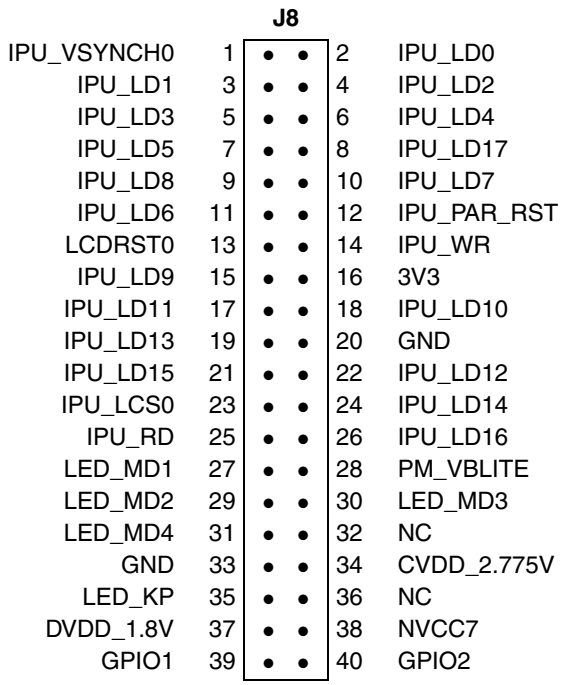


Figure 4-10. Parallel LCD Connector II J8 Pin Assignment

Table 4-14. Parallel LCD Connector II J8 Signal Description

Pin	Signal	Description
1	IPU_VSYNCH0	VERTICAL SYNCH 0
2	IPU_LD0	LCD DATA 0
3	IPU_LD1	LCD DATA 1
4	IPU_LD2	LCD DATA 2
5	IPU_LD3	LCD DATA 3
6	IPU_LD4	LCD DATA 4
7	IPU_LD5	LCD DATA 5
8	IPU_LD17	LCD DATA 17
9	IPU_LD8	LCD DATA 8
10	IPU_LD7	LCD DATA 7
11	IPU_LD6	LCD DATA 6
12	IPU_PAR_RESET	PARALLEL INTERFACE RESET
13	LCDRST0	LCD RESET 0
14	IPU_WR	PARALLEL INTERFACE WRITE
15	IPU_LD9	LCD DATA 9
16	3V3	3 VDC SUPPLY
17	IPU_LD11	LCD DATA 11
18	IPU_LD10	LCD DATA 10
19	IPU_LD13	LCD DATA 13
20	GND	SIGNAL GROUND
21	IPU_LD15	LCD DATA 15

Table 4-14. Parallel LCD Connector II J8 Signal Description (continued)

Pin	Signal	Description
22	IPU_LD12	LCD DATA 12
23	IPU_LCS0	LCD CHIP SELECT
24	IPU_LD14	LCD DATA 14
25	IPU_RD	PARALLEL INTERFACE READ
26	IPU_LD16	LCD DATA 16
27	LED_MD1	MAIN DISPLAY LIGHT EMMITING DIODE
28	PM_VBLITE	LCD PANEL BACKLIGHT VOLTAGE
29	LED_MD2	MAIN DISPLAY LIGHT EMMITING DIODE
30	LED_MD3	MAIN DISPLAY LIGHT EMMITING DIODE
31	LED_MD4	MAIN DISPLAY LIGHT EMMITING DIODE
32	NC	NOT CONNECTED
33	GND	SIGNAL GROUND
34	CVDD_2.775V	2.775 VDC SUPPLY
35	LED_KP	KEYPAD LIGHT EMMITING DIODE
36	NC	NOT CONNECTED
37	DVDD_1.8V	1.8 VDC SUPPLY
38	NVCC7	5 VDC SUPPLY
39	GPIO1	GENERAL PURPOSE I/O LINE 1
40	GPIO2	GENERAL PURPOSE I/O LINE 2

4.2.5.4 Serial Asynchronous LCD Connector

Connector J6 provides serial asynchronous control signals for an LCD panel. Figure 4-11 shows connector pin assignments and Table 4-15 describes the signals.

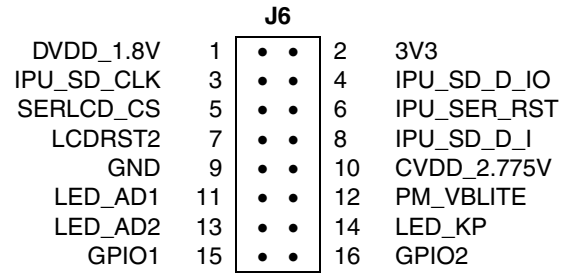


Figure 4-11. Serial Asynchronous LCD Connector J6 Pin Assignment

Table 4-15. Serial Asynchronous LCD Connector J6 Signal Description

Pin	Signal	Description
1	DVDD_1.8V	1.8 VDC SUPPLY
2	3V3	3 VDC SUPPLY
3	IPU_SD_CLK	SERIAL DATA CLOCK
4	IPU_SD_D_IO	SERIAL DATA INPUT/OUTPUT
5	SERLCD_CS	SERIAL LCD CHIP SELECT
6	IPU_SER_RST	SERIAL INTERFACE RESET
7	LCDRST2	LCD DISPLAY RESET 2
8	IPU_SD_D_I	SERIAL DATA INPUT
9	GND	SIGNAL GROUND
10	CVDD_2.775V	2.775 VDC SUPPLY
11	LED_AD1	AUXILARY DISPLAY LIGHT EMMITING DIODE
12	PM_VBLITE	LCD PANEL BACKLIGHT VOLTAGE
13	LED_AD2	AUXILARY DISPLAY LIGHT EMMITING DIODE
14	LED_KP	KEYPAD LIGHT EMMITING DIODE
15	GPIO1	GENERAL PURPOSE I/O LINE 1
16	GPIO2	GENERAL PURPOSE I/O LINE 2

4.2.6 Funlight Connector

Connector J20 provides control signals for three, three-segment RGB LCD funlights. Figure 4-12 shows connector pin assignments and Table 4-16 describes the signals.

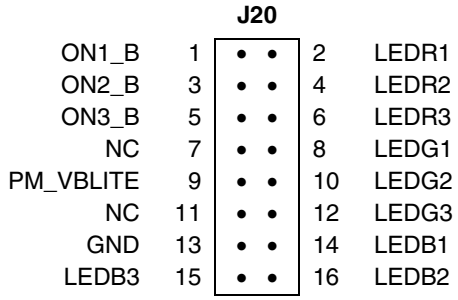


Figure 4-12. Funlight Connector J20 Pin Assignment

Table 4-16. Funlight Connector J20 Signal Description

Pin	Signal	Description
1	ON1_B	ON FUNLIGHT 1
2	LEDR1	LED 1 RED SEGMENT ON
3	ON2_B	ON FUNLIGHT 2
4	LEDR2	LED 2 RED SEGMENT ON
5	ON3_B	ON FUNLIGHT 3
6	LEDR3	LED 3 RED SEGMENT ON
7	NC	NO CONNECTION
8	LEDG1	LED 1 GREEN SEGMENT ON
9	PM_VBLITE	LCD PANEL BACKLIGHT VOLTAGE
10	LEDG2	LED 2 GREEN SEGMENT ON
11	NC	NO CONNECTION
12	LEDG3	LED 3 GREEN SEGMENT ON
13	GND	SIGNAL GROUND
14	LEDB1	LED 1 BLUE SEGMENT ON
15	LEDB3	LED 3 BLUE SEGMENT ON
16	LEDB2	LED 2 BLUE SEGMENT ON

4.2.7 Audio Connectors

All the audio connectors on the Base board provide connections to the Yamaha YMU782B music synthesizer chip. See the manufacturer's specification sheet (on the ADS CD) for detailed signal and drive specifications.

4.2.7.1 Miniature Audio Jacks

Audio connectors J25 through J29 are all standard stereo mini-jacks. Figure 4-13 shows jack terminals. Table 4-17 describes the signals and termination.

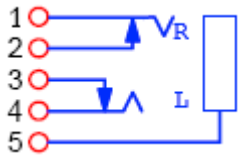


Figure 4-13. Audio Jack Diagram

4.2.7.2 Speaker Terminals

TB1 provides two screw terminals for left and right channel analog stereo speaker output signals SPOUT 1 and SPOUT2.

Table 4-17. Audio Jack Signal Description

Jack	Termination				
	1	2	3	4	5
25	NC	NC	NC	TXOUT	GND
26	NC	NC	NC	EXTOUT	GND
27	HPOUTL	NC	NC	HPOUTR	GND
28	NC	NC	NC	RXIN	GND
29	NC	NC	NC	EXTIN	GND
Signal Description					
TXOUT	TX OUT				
EXTOUT	ANALOG LINE OUT				
HPOUTL	HEADPHONE ANALOG OUTPUT LEFT				
HPOUTR	HEADPHONE ANALOG OUTPUT RIGHT				
RXIN	RX IN				
EXTIN	ANALOG LINE IN				

4.2.8 Television Encoder Connector

P13 is the TV encoder connector. Figure 4-14 shows pin assignments and Table 4-18 describes the signals.

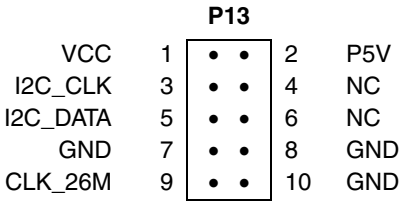


Figure 4-14. TV Encoder Connector P13 Pin Assignment

Table 4-18. TV Encoder Connector P13 Signal Description

Pin	Signal	Description
1	VCC	3 VDC POWER
2	P5V	5 VDC POWER
3	I2C_CLK	I 2C CLOCK — Serial clock, bidirectional
4	NC	NO CONNECTION
5	I2C_DATA	I2 C DATA — Serial data, bidirectional
6	NC	NO CONNECTION
7	GND	SIGNAL GROUND
8	GND	SIGNAL GROUND
9	CLK_26M	26 MHz CLOCK
8	GND	SIGNAL GROUND

4.2.9 ATA Drive Controller Connector

J3 is a 44-pin, 2-row keyed header with 2-mm pin spacing. It supports connection of small form-factor ATA HDDs. Figure 4-15 shows pin assignments and Table 4-19 describes the signals.

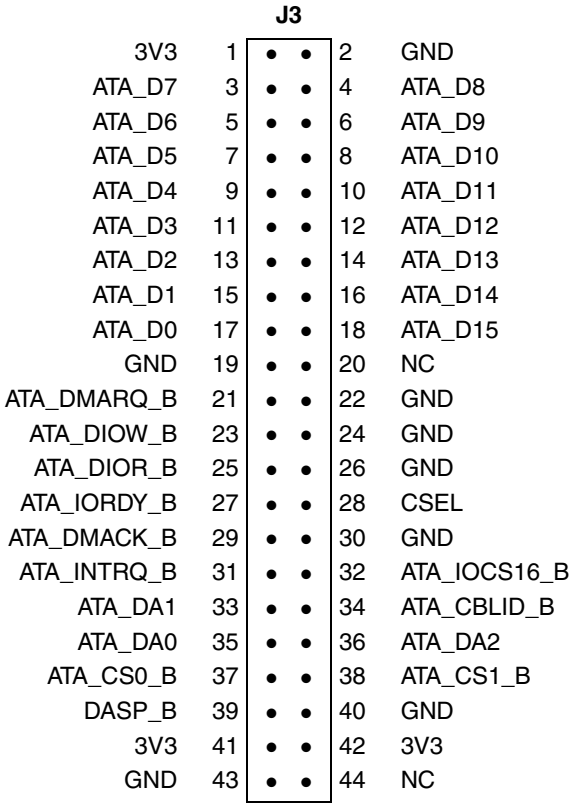


Figure 4-15. ATA Connector J3 Pin Assignment

Table 4-19. ATA Connector J3 Signal Description

Pin	Signal	Description
1	3V3	3 VDC POWER
2	GND	SIGNAL GROUND
3	ATA_D7	ATA DATA 7
4	ATA_D8	ATA DATA 8
5	ATA_D6	ATA DATA 6
6	ATA_D9	ATA DATA 9
7	ATA_D5	ATA DATA 5
8	ATA_D10	ATA DATA 10
9	ATA_D4	ATA DATA 4
10	ATA_D11	ATA DATA 11
11	ATA_D3	ATA DATA 3
12	ATA_D12	ATA DATA 12
13	ATA_D2	ATA DATA 2
14	ATA_D13	ATA DATA 13

Table 4-19. ATA Connector J3 Signal Description (continued)

Pin	Signal	Description
15	ATA_D1	ATA DATA 1
16	ATA_D14	ATA DATA 14
17	ATA_D0	ATA DATA 0
18	ATA_D15	ATA DATA 15
19	GND	SIGNAL GROUND
20	NC	NO CONNECTION
21	ATA_DMARQ_B	ATA DMA REQUEST
22	GND	SIGNAL GROUND
23	ATA_DIOW_B	ATA DATA INPUT/OUTPUT READ
24	GND	SIGNAL GROUND
25	ATA_DIOR_B	ATA DATA INPUT/OUTPUT WRITE
26	GND	SIGNAL GROUND
27	ATA_IORDY_B	ATA INPUT/OUTPUT READY
28	CSEL	CHIP SELECT (TIED HIGH)
29	ATA_DMACK_B	ATA DMA ACKNOWLEDGE
30	GND	SIGNAL GROUND
31	ATA_INTREQ_B	ATA INTERRUPT REQUEST
32	ATAIOIS16_B	ATA - IO PORT IS 16 BIT
33	ATA_DA1	ATA REGISTER ADDRESS SIGNAL
34	ATA_CBLID_B	ATA CABLE ID
35	ATA_DA0	ATA REGISTER ADDRESS SIGNAL
36	ATA_DA2	ATA REGISTER ADDRESS SIGNAL
37	ATA_CS0_B	ATA CHIP SELECT
38	ATA_CS1_B	ATA CHIP SELECT
39	ATA_DASP_B	ATA DRIVE 1 IS PRESENT
40	GND	SIGNAL GROUND
41	3V3	3 VDC POWER
42	3V3	3 VDC POWER
43	GND	SIGNAL GROUND
44	NC	NO CONNECTION

4.2.10 RS-232 Connectors

ADS RS-232 interfaces are controlled either by MCU UARTs or by a DUART on the Base board. Transceivers on the Base board drive the MCU signals to RS-232 levels. MCU UARTs are switch-selectable on the Base board. There are three DCE ports and two DTE ports.

4.2.10.1 DCE Connectors

DB9 connector P7A connects to UART transceiver C, which can be driven by MCU UART1 or UART2. DB9 connector P7B connects to DUART channel A. Header J7 connects to DUART channel B. Figure 4-16 shows DB9 pin assignments and Table 4-20 describes connector signals. Figure Figure 4-17 shows J7 pin assignments and Table 4-21 describes J7 signals.

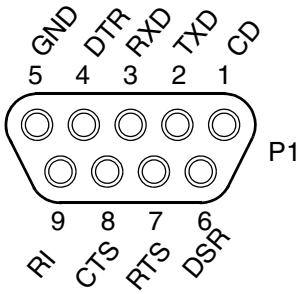


Figure 4-16. RS-232 DCE Connectors P7A and P7B Pin Assignment

Table 4-20. RS-232 DCE Connectors P7A and P7B Signal Description

Pin	Signal	Description
1	CD	CARRIER DETECT — RS-232 output signal, pulled active positive
2	TXD	TRANSMITTED DATA — RS-232 serial data output signal
3	RXD	RECEIVED DATA — RS-232 serial data input signal
4	DTR	DATA TERMINAL READY — RS-232 input signal, the logic level signal is available at TP8
5	GND	GROUND
6	DSR	DATA SET READY — RS-232 output signal, pulled active positive
7	$\overline{\text{RTS}}$	READY TO SEND — RS-232 input signal, active positive
8	CTS	CLEAR TO SEND — RS-232 output signal, active positive
9	RI	RING INDICATOR — RS-232 output signal, forced inactive negative

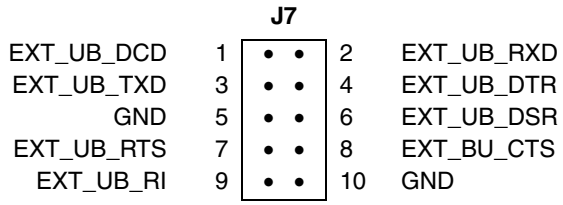


Figure 4-17. RS-232 DCE Connector J7 Pin Assignment

Table 4-21. RS-232 DCE Connector J7 Pin Signal Description

Pin	Signal	Description
1	EXT_UB_DCD	DUART CHANNEL B CARRIER DETECT
2	EXT_UB_RXD	DUART CHANNEL B TRANSMITTED DATA
3	EXT_UB_TXD	DUART CHANNEL B RECEIVED DATA
4	EXT_UB_DTR	DUART CHANNEL B DATA TERMINAL READY
5	GND	SIGNAL GROUND
6	EXT_UB_DSR	DUART CHANNEL B DATA SET READ
7	EXT_UB_RTS	DUART CHANNEL B READY TO SEND
8	EXT_BU_CTS	DUART CHANNEL B CLEAR TO SEND
9	EXT_UB_RI	DUART CHANNEL B RING INDICATOR
10	GND	SIGNAL GROUND

4.2.10.2 DTE Connectors

DB9 connector P11A connects to UART transceiver A, which can be driven by MCU UART1 or UART5. DB9 connector P11B connects to UART transceiver B, which can be driven by MCU UART3 or UART4. Figure 4-18 shows DB9 pin assignments and Table 4-22 describes connector signals.

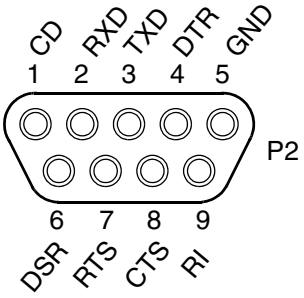


Figure 4-18. RS-232 DTE Connectors P11A and P11B Pin Assignment

Table 4-22. RS-232 DTE Connectors P11A and P11B Signal Description

Pin	Signal	Description
1	CD	CARRIER DETECT — RS-232 input signal
2	RXD	RECEIVED DATA — RS-232 serial data input signal
3	TXD	TRANSMITTED DATA — RS-232 serial data output signal
4	DTR	DATA TERMINAL READY — RS-232 output signal
5	GND	GROUND
6	DSR	DATA SET READY — RS-232 input signal
7	RTS	READY TO SEND — RS-232 output signal
8	CTS	CLEAR TO SEND — RS-232 input signal
9	RI	RING INDICATOR — RS-232 input signal

4.2.11 I2C Connector

JP13 is the I2C interface connector for the ADS. The jumper block is used to connect directly to MCU I2C transceiver 1. Table 4-23 describes JP13 signals.

Table 4-23. I2C Connector JP13 Signal Description

Pin	Signal	Description
1	12C1_CLK	I2C INTERFACE 1 CLOCK
2	I2C1_DAT	I2C INTERFACE 1 DATA
3	GND	SIGNAL GROUND

4.2.12 CSPI Connector

J15 is the ADS CSPI connector. Figure 4-19 shows pin assignments and Table 4-24 describes J15 signals.

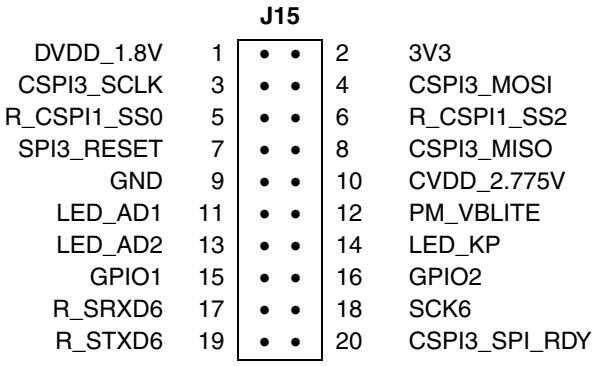


Figure 4-19. CSPI Connector J15 Pin Assignment

Table 4-24. CSPI Connector J15 Signal Description

Pin	Signal	Description
1	DVDD_1.8V	1.8 VDC POWER
2	3V3	3 VDC POWER
3	CSPI3_SCLK	CSPI3 SERIAL CLOCK
4	CSPI3_MOSI	CSPI3 MASTER OUT SLAVE IN
5	R_CSPI1_SS0	CSPI1 SLAVE SELECT 0
6	R_CSPI1_SS2	CSPI1 SLAVE SELECT 2
7	SPI3_RESET	SPI3 RESET FROM CPLD
8	CSPI3_MISO	CSPI3 MASTER IN SLAVE OUT
9	GND	SIGNAL GROUND
10	CVDD_2.775V	2.775 VDC POWER
11	LED_AD1	AUXILARY DISPLAY LIGHT EMMITING DIODE
12	PM_VBLITE	POWER MANAGER BACKGROUND LIGHT
13	LED_AD2	AUXILARY DISPLAY LIGHT EMMITING DIODE
14	LED_KP	KEYPAD LIGHT EMMITING DIODE
15	GPIO1	GENERAL PURPOSE INPUT/OUTPUT 1
16	GPIO2	GENERAL PURPOSE INPUT/OUTPUT 2
17	R_SRXD6	Audio Port 6 - RECEIVE DATA
18	SCK6	SERIAL CLOCK 6
19	R_STXD6	Audio Port 6 - TRANSMIT DATA
20	CSPI3_SPI_RDY	CSPI3 INTERFACE READY

4.2.13 Ethernet Connector

T1 is the RJ-45 Ethernet connector for the ADS. Figure 4-20 shows pin numbering and Table 4-25 provides signal descriptions for the connector.

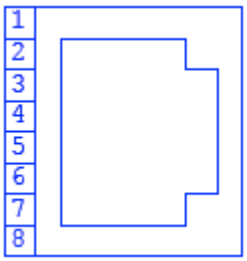


Figure 4-20. Ethernet Connector T1 Pin Numbers

Table 4-25. Ethernet Connector T1 Signal Description

Pin	Signal	Description
1	TPO+	DIFFERENTIAL OUTPUT PLUS
2	TPO-	DIFFERENTIAL OUTPUT MINUS
3	TPI+	DIFFERENTIAL INPUT PLUS
4	NC	NO CONNECTION
5	NC	NO CONNECTION
6	TPI-	DIFFERENTIAL INPUT MINUS
7	NC	NO CONNECTION
8	NC	NO CONNECTION

4.2.14 USB OTG Connectors

J1 and J2 are USB OTG connectors. J1 is a high-speed connector, while J2 is a full-speed connector. Figure 4-21 shows pin assignments and Table 4-26 describes signals.

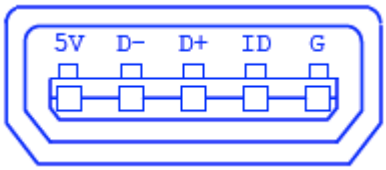


Figure 4-21. USB OTG Connectors J1 and J2 Pin Assignment

Table 4-26. USB OTG Connectors J1 andJ2 Signal Description

Pin	Signal	Description
1	5V	5 VDC BUS VOLTAGE
2	D-	USB DATA MINUS
3	D+	USB DATA PLUS
4	ID	BUS ID
5	GND	GROUND

4.2.15 USB Host Connectors

J4 and J5 are USB host connectors. J4 is a high-speed connector, while J5 is a full-speed connector. Figure 4-22 shows pin assignments and Table 4-27 describes signals.

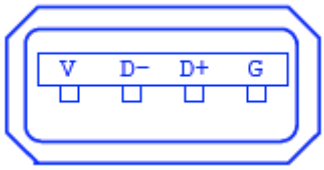


Figure 4-22. USB Host Connectors J4 and J5 Pin Assignment

Table 4-27. USB Host Connectors J4 and J5 Signal Description

Pin	Signal	Description
1	VBUS	VBUS
2	D-	USB DATA MINUS
3	D+	USB DATA PLUS
4	GND	GROUND

4.2.16 CE Bus Connector

Connector J19 is the CE bus header. Figure 4-23 shows pin assignments and Table 4-28 describes signals.

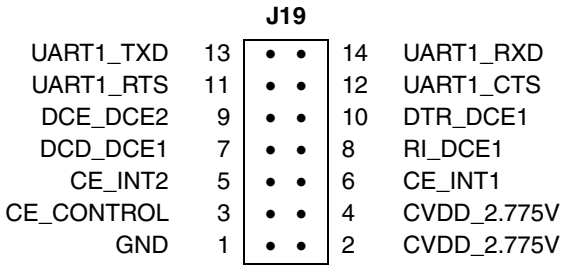


Figure 4-23. CE Bus Connector J19 Pin Assignment

Table 4-28. CE Bus Connector J19 Signal Description

Pin	Signal	Description
1	GND	SIGNAL GROUND
2	CVDD_2.775V	2.775 VDC POWER
3	CE_CONTROL	CE BUS CONTROL
4	CVDD_2.775V	2.775 VDC POWER
5	CE_INT2	CE BUS INTERRUPT 2
6	CE_INT1	CE BUS INTERRUPT 1
7	DCD_DCE1	UART1 DCE signal - DCD
8	RI_DCE1	UART1 DCE signal - Ring Indicator
9	DCD_DCE2	UART1 DCE signal - DCD
10	DTR_DCE1	UART1 DCE signal - DTR
11	UART1_RTS	UART 1 READY TO SEND
12	UART1_CTS	UART1 CLEAR TO SEND
13	UART1_TXD	UART1 TRANSMIT DATA
14	UART1_RXD	UART1 RECEIVE DATA

4.2.17 SD/MMC Connectors

P3 and P4 are SD/MMC connectors. Figure 4-24 shows pin assignments. Table 4-29 describes P3 signals. Table 4-30 describes P4 signals.

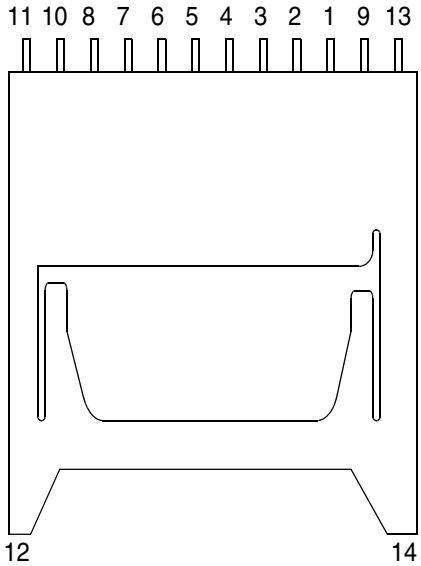


Figure 4-24. SD/MMC Connector Pin Assignments

Table 4-29. SD/MMC Connector P3 Signal Description

Pin(s)	Signal	Description		
		MMC Card	SD Card	
			1-Bit Mode	4-Bit Mode
1	SD1_DATA3	DATA LINE 3	Not Used	DATA LINE 3
2	SD1_CMD	COMMAND/RESPONSE		
3	GND	SIGNAL GROUND		
4	VDD	3 VDC POWER (selectable VSD2 or 3V3)		
5	SD1_CLK	CLOCK INPUT		
6	GND	SIGNAL GROUND		
7	SD1_DATA0	DATA LINE 0		
8	SD1_DAT1	DATA LINE 1	INTERRUPT (IRQ)	DATA LINE 1 or IRQ
9	SD1_DAT2	DATA LINE 2	READWAIT(RW)	DATA LINE 2 or RW
10	SD1_DET	CARD DETECT		
11	GND	GROUND		
12	NC	NO CONNECTION		
13	NC	NO CONNECTION		
14	NC	NO CONNECTION		
15	NC	NO CONNECTION		
16	SD_WP	WRITE PROTECT DETECT		

Table 4-30. SD/MMC Connector P4 Signal Description

Pin(s)	Signal	Description		
		MMC Card	SD Card	
			1-Bit Mode	4-Bit Mode
1	PC_PWRON	DATA LINE 3	Not Used	DATA LINE 3
2	PC_CD1_B	COMMAND/RESPONSE		
3	GND	SIGNAL GROUND		
4	VDD	3 VDC POWER (selectable VSD2 or 3V3)		
5	PC_CD2_B	CLOCK INPUT		
6	GND	SIGNAL GROUND		
7	PC_WAIT_B	DATA LINE 0		
8	PC_READY	DATA LINE 1	INTERRUPT (IRQ)	DATA LINE 1 or IRQ
9	PC_VS1	DATA LINE 2	READWAIT(RW)	DATA LINE 2 or RW
10	SD2_DET	CARD DETECT		
11	GND	GROUND		
12	NC	NO CONNECTION		
13	NC	NO CONNECTION		
14	NC	NO CONNECTION		
15	NC	NO CONNECTION		
16	SD2_WP	WRITE PROTECT DETECT		

4.2.18 PCMCIA Connector

U30 is a standard 88-pin PCMCIA socket. Table 4-31 describes U30 signals.

Table 4-31. PCMCIA Connector U30 Signal Description

Pin	Signal	Description
1	GND	SIGNAL GROUND
2	PC_D3	DATA 3
3	PC_D4	DATA 4
4	PC_D5	DATA 5
5	PC_D6	DATA 6
6	PC_D7	DATA 7
7	PC_CE1_B	DATA 8
8	PC_A10	ADDRESS 10
9	OE_B	OUTPUT ENABLE
10	PC_A11	ADDRESS 11
11	PC_A9	ADDRESS 9
12	PC_A8	ADDRESS 8
13	PC_A13	ADDRESS 13
14	PC_A14	ADDRESS 14
15	WE_B	WRITE ENABLE
16	READY	READY
17	VCC	SWITCHED POWER
18	VPP	SWITCHED POWER
19	PC_A16	ADDRESS 16
20	PC_A15	ADDRESS 15
21	PC_A12	ADDRESS 12
22	PC_A7	ADDRESS 7
23	PC_A6	ADDRESS 6
24	PC_A5	ADDRESS 5
25	PC_A4	ADDRESS 4
26	PC_A3	ADDRESS 3
27	PC_A2	ADDRESS 2
28	PC_A1	ADDRESS 1
29	PC_A0	ADDRESS 0
30	PC_D0	DATA 0
31	PC_D1	DATA 1
32	PC_D2	DATA 2
33	IOIS16/WP	PCMCIA control signal
34	GND	SIGNAL GROUND
35	GND	SIGNAL GROUND
36	R_PC_CD1_B	PCMCIA Card Detect 1
37	PC_D11	DATA 11
38	PC_D12	DATA 12
39	PC_D13	DATA 13
40	PC_D14	DATA 14
41	PC_D15	DATA 15
42	PC_CE2_B	PCMCIA CARD ENABLE2

Table 4-31. PCMCIA Connector U30 Signal Description (continued)

Pin	Signal	Description
43	VS1	PCMCIA Voltage Sense 1 signal
44	IORD_B	INPUT/OUTPUT READ
45	IOWR_B	INPUT/OUTPUT WRITE
46	PC_A17	ADDRESS 17
47	PC_A18	ADDRESS 18
48	PC_A19	ADDRESS 19
49	PC_A20	ADDRESS 20
50	PC_A21	ADDRESS 21
51	VCC	SWITCHED POWER
52	VPP	SWITCHED POWER
53	PC_A22	ADDRESS 22
54	PC_A23	ADDRESS 23
55	PC_A24	ADDRESS 24
56	PC_A25	ADDRESS 25
57	VS2	PCMCIA Voltage Sense 2signal
58	RST_PC	PCMCIA RESET
59	WAIT	PCMCIA WAIT
60	NC	NO CONNECTION
61	REG_B	PCMCIA REGISTER ACCESS OUTPUT
62	BVD2	PCMCIA Battery Voltage Detect 2
63	BVD1	PCMCIA Battery Voltage Detect 1
64	PC_D8	DATA 8
65	PC_D9	DATA 9
66	PC_D10	DATA 10
67	R_PC_CD2_B	PCMCIA Card Detect 2
68	GND	SIGNAL GROUND
69-88	NC	NO CONNECTION

4.2.19 SIMM Socket

P8 is a standard six-contact SIMM socket. Table 4-32 describes socket signals.

Table 4-32. SIMM Socket P8 Signal Description

Pin	Signal	Description
1	NVCC9	POWER
2	SRST0	RESET 0
3	SCLK0	SERIAL CLOCK 0
4	GND	GROUND SIGNAL
5	VPP	PROGRAMING POWER
6	STX0	BIDIRECTIONAL DATA

4.2.20 Baseband Board Connector

J24 is a 64-pin socket for an optional baseband board. Figure 4-25 shows pin assignments. Table 4-33 describes P3 signals.

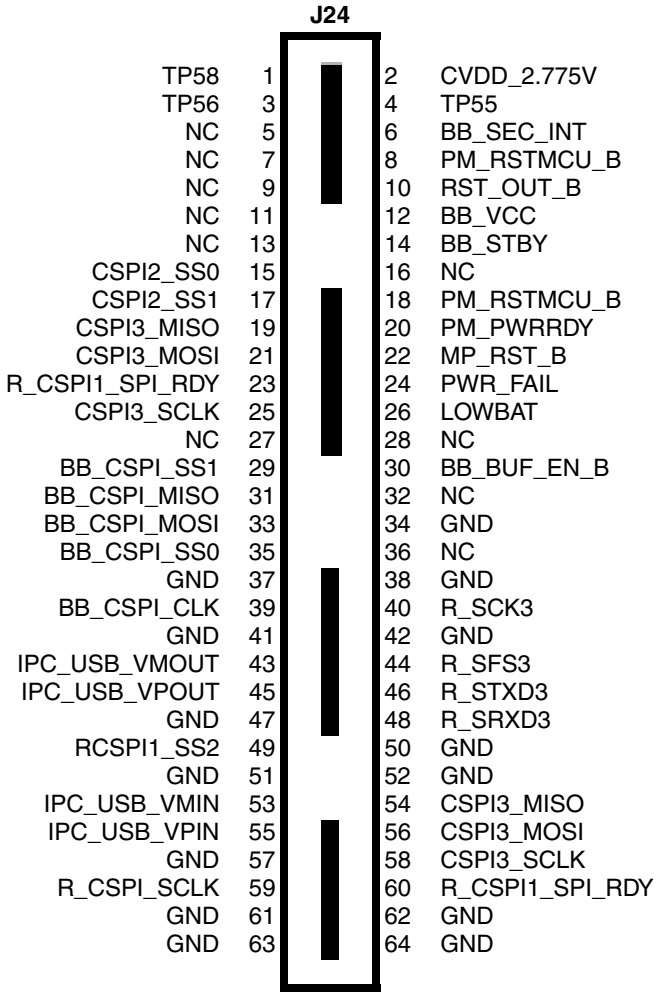


Figure 4-25. Baseband Board Connector J24 Pin Assignment

Table 4-33. Baseband Board Connector J24 Signal Description

Pin	Signal	Description
1	TP58	TEST POINT 58
2	CVDD_2.775V	2.775 VDC POWER
3	TP56	TEST POINT 56
4	TP55	TEST POINT 55
5	NC	NO CONNECTION
6	BB_SEC_INT	BASEBOARD SEC INTERRUPT
7	NC	NO CONNECTION
8	PM_RSTMCU_B	POWER MANAGEMENT RESET MCU
9	NC	NO CONNECTION
10	RST_OUT_B	RESET OUT — Active low reset signal from the MCU
11	NC	NO CONNECTION
12	BB_VCC	BASE BOARD VCC
13	NC	NO CONNECTION
14	BB_STBY	BASE BOARD STANDBY
15	CSPI2_SS0	CSPI 2 SLAVE SELECT 0
16	NC	NO CONNECTION
17	CSPI2_SS1	CSPI 2 SLAVE SELECT 1
18	PM_RSTMCU_B	POWER MANAGEMENT RESET MCU
19	CSPI3_MISO	CSPI3 MASTER IN SLAVE OUT
20	PM_PWRRDY	POWER MANAGEMENT POWER READY
21	CSPI3_MOSI	CSPI3 MASTER OUT SLAVE IN
22	PM_RST_B	POWER MANAGEMENT RESET
23	R_CSPI1_SPI_RDY	CSPI1 SPI READY
24	PWR_FAIL	POWER FAILURE
25	CSPI3_SCLK	CSPI3_SERIAL CLOCK
26	LOWBAT	LOW BATTERY
27	NC	NO CONNECTION
28	NC	NO CONNECTION
29	BB_CSPI_SS1	BASE BOARD CSPI SLACE SELECT 1
30	BB_BUF_EN_B	BASE BOARD BUFFER ENABLE
31	BB_CSPI_MISO	BASE BOARD CSPI MASTER IN SLAVE OUT
32	NC	NO CONNECTION
33	BB_CSPI_MOSI	BASE BOARD MASTER OUT SLAVE IN
34	GND	SIGNAL GROUND
35	BB_CSPI_SS0	BASE BOARD CSPI SALVE SELECT 0
36	NC	NO CONNECTION
37	GND	SIGNAL GROUND
38	GND	SIGNAL GROUND
39	BB_CSPI_CLK	BASE BOARD CSPI CLOCK
40	R_SCK3	SERIAL CLOCK
41	GND	SIGNAL GROUND
42	GND	SIGNAL GROUND
43	IPC_USB_VMOUT	USB VOLTAGE MINUS OUT
44	R_SFS3	FRAME SYNC
45	IPC_USB_VPOUT	USB VOLTAGE POSITIVE OUT

Table 4-33. Baseband Board Connector J24 Signal Description (continued)

Pin	Signal	Description
46	R_STXD3	SEIAL TRANSMIT DATA
47	GND	SIGNAL GROUND
48	R_SRXD3	Audio Port 3- RECEIVE DATA
49	R_CSPI1_SS2	CSPI1 SLAVE SELECT 2
50	GND	SIGNAL GROUND
51	GND	SIGNAL GROUND
52	GND	SIGNAL GROUND
53	IPC_USB_VMIN	USB VOLTAGE MINUS IN
54	CSPI3_MISO	CSPI3 MASTER IN SLAVE OUT
55	IPC_USB_VPIN	USB VOLTAGE POSITIVE IN
56	CSPI3_MOSI	CSPI3 MASTER OUT SLAVE IN
57	GND	SIGNAL GROUND
58	CSPI3_SCLK	CSPI3 SERIAL CLOCK
59	R_CSPI_SCLK	CSPI SERIAL CLOCK
60	R_CSPI1_SPI_RDY	CSPI1SPI READY
61	GND	SIGNAL GROUND
62	GND	SIGNAL GROUND
63	GND	SIGNAL GROUND
64	GND	SIGNAL GROUND

4.2.21 Debugging and Programming Connectors

The Base board has two connectors that provide buffered MCU address, data, and control signals for debugging, and two connectors that can be used to program the CPLD and the single-wire EEPROM.

4.2.21.1 Software Analysis Connector

P9 is the software analysis connector. Figure 4-26 shows pin assignments and Table 4-34 describes the signals.

4.2.21.2 Address Connector

P10 is the software analysis connector. Figure 4-27 shows pin assignments and Table 4-35 describes the signals.

4.2.21.3 CPLD Programming Connector

J14 is the CPLD programming connector. Figure 4-28 shows pin assignments and Table 4-36 describes the signals.

4.2.21.4 One-wire EEPROM Programming

One-wire EEPROM programming is enabled by Jumper 14. See Chapter 2 for more information.

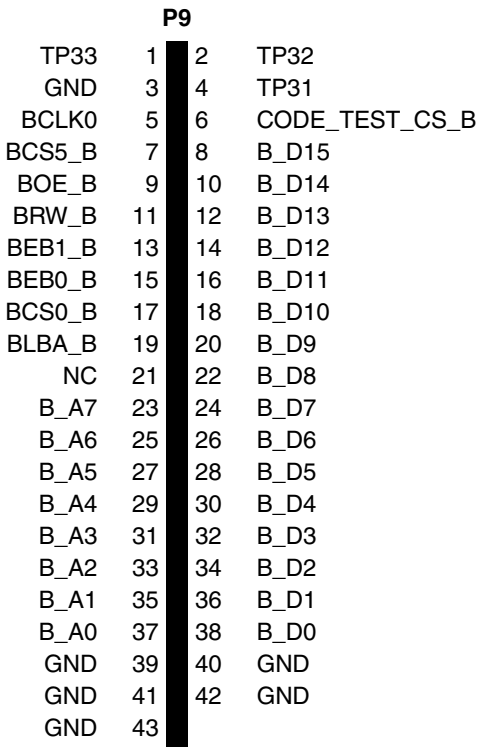


Figure 4-26. Software Analysis Connector P9 Pin Assignment

Table 4-34. Software Analysis Connector P9 Signal Description

Pin	Signal	Description
1	TP33	TEST POINT 33
2	TP32	TEST POINT 32
3	GND	SIGNAL GROUND
4	TP31	TEST POINT 31
5	BCLK0	BUFFERED CLOCK 0
6	CODE_TEST_CS_B	CODE TEST CHIP SELECT
7	BCS5_B	BUFFERED CHIP SELECT 5
8	B_D15	BUFFERED DATA 15
9	BOE_B	BUFFERED OUTPUT ENABLE
10	B_D14	BUFFERED DATA 14
11	BRW_B	BUFFERED READ/WRITE
12	B_D13	BUFFERED DATA 13
13	BEB1_B	BUFFERED EB 1
14	B_D12	BUFFERED DATA 12
15	BEB0_B	BUFFERED EB 0
16	B_D11	BUFFERED DATA 11
17	BCS0_B	BUFFERED CHIP SELECT 0
18	B_D10	BUFFERED DATA 10
19	BLBA_B	BUFFERED LBA

Table 4-34. Software Analysis Connector P9 Signal Description (continued)

Pin	Signal	Description
20	B_D9	BUFFERED DATA 9
21	NC	NO CONNECTION
22	B_D8	BUFFERED DATA 8
23	B_A7	BUFFERED ADDRESS 7
24	B_D7	BUFFERED DATA 7
25	B_A6	BUFFERED ADDRESS 6
26	B_D6	BUFFERED DATA 6
27	B_A5	BUFFERED ADDRESS 5
28	B_D5	BUFFERED DATA 5
29	B_A4	BUFFERED ADDRESS 4
30	B_D4	BUFFERED DATA 4
31	B_A3	BUFFERED ADDRESS 3
32	B_D3	BUFFERED DATA 3
33	B_A2	BUFFERED ADDRESS 2
34	B_D2	BUFFERED DATA 2
35	B_A1	BUFFERED ADDRESS 1
36	B_D1	BUFFERED DATA 1
37	B_A0	BUFFERED ADDRESS 0
38	B_D0	BUFFERED DATA 0
39-43	GND	SIGNAL GROUND

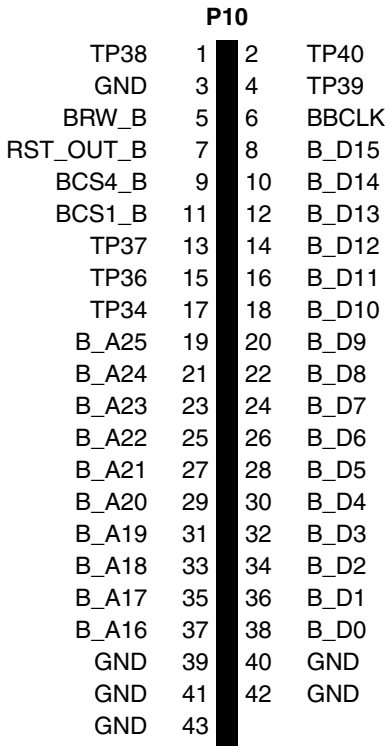


Figure 4-27. Address Connector P10 Pin Assignment

Table 4-35. Address Connector P10 Signal Description

Pin	Signal	Description
1	TP38	TEST POINT 38
2	TP40	TEST POINT 40
3	GND	SIGNAL GROUND
4	TP39	TEST POINT 39
5	BRW_B	BUFFERED READ/WRITE
6	BBCLK	BASE BOARD CLOCK
7	RST_OUT_B	RESET OUT — Active low reset signal from the MCU
8	B_A15	BUFFERED ADDRESS 15
9	BCS4_B	BUFFERED CHIP SELECT 4
10	B_A14	BUFFERED ADDRESS 14
11	BCS1_B	BUFFERED CHIP SELECT 1
12	B_A13	BUFFERED ADDRESS 13
13	TP37	TEST POINT 37
14	B_A12	BUFFERED ADDRESS 12
15	TP36	TEST POINT 36
16	B_A11	BUFFERED ADDRESS 11
17	TP34	TEST POINT 34
18	B_A10	BUFFERED ADDRESS 10
19	B_A25	BUFFERED ADDRESS 25
20	B_A9	BUFFERED ADDRESS 9
21	B_A24	BUFFERED ADDRESS 24
22	B_A8	BUFFERED ADDRESS 8
23	B_A23	BUFFERED ADDRESS 23
24	B_A7	BUFFERED ADDRESS 7
25	B_A22	BUFFERED ADDRESS 22
26	B_A6	BUFFERED ADDRESS 6
27	B_A21	BUFFERED ADDRESS 21
28	B_A5	BUFFERED ADDRESS 5
29	B_A20	BUFFERED ADDRESS 20
30	B_A4	BUFFERED ADDRESS 4
31	B_A19	BUFFERED ADDRESS 19
32	B_A3	BUFFERED ADDRESS 3
33	B_A18	BUFFERED ADDRESS 18
34	B_A2	BUFFERED ADDRESS 2
35	B_A17	BUFFERED ADDRESS 17
36	B_A1	BUFFERED ADDRESS 1
37	B_A16	BUFFERED ADDRESS 16
38	B_A0	BUFFERED ADDRESS 0
39-43	GND	SIGNAL GROUND

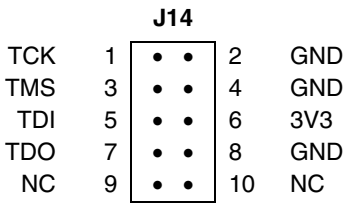


Figure 4-28. CPLD Programming Connector J14 Pin Assignment

Table 4-36. CPLD Programming Connector J14 Signal Description

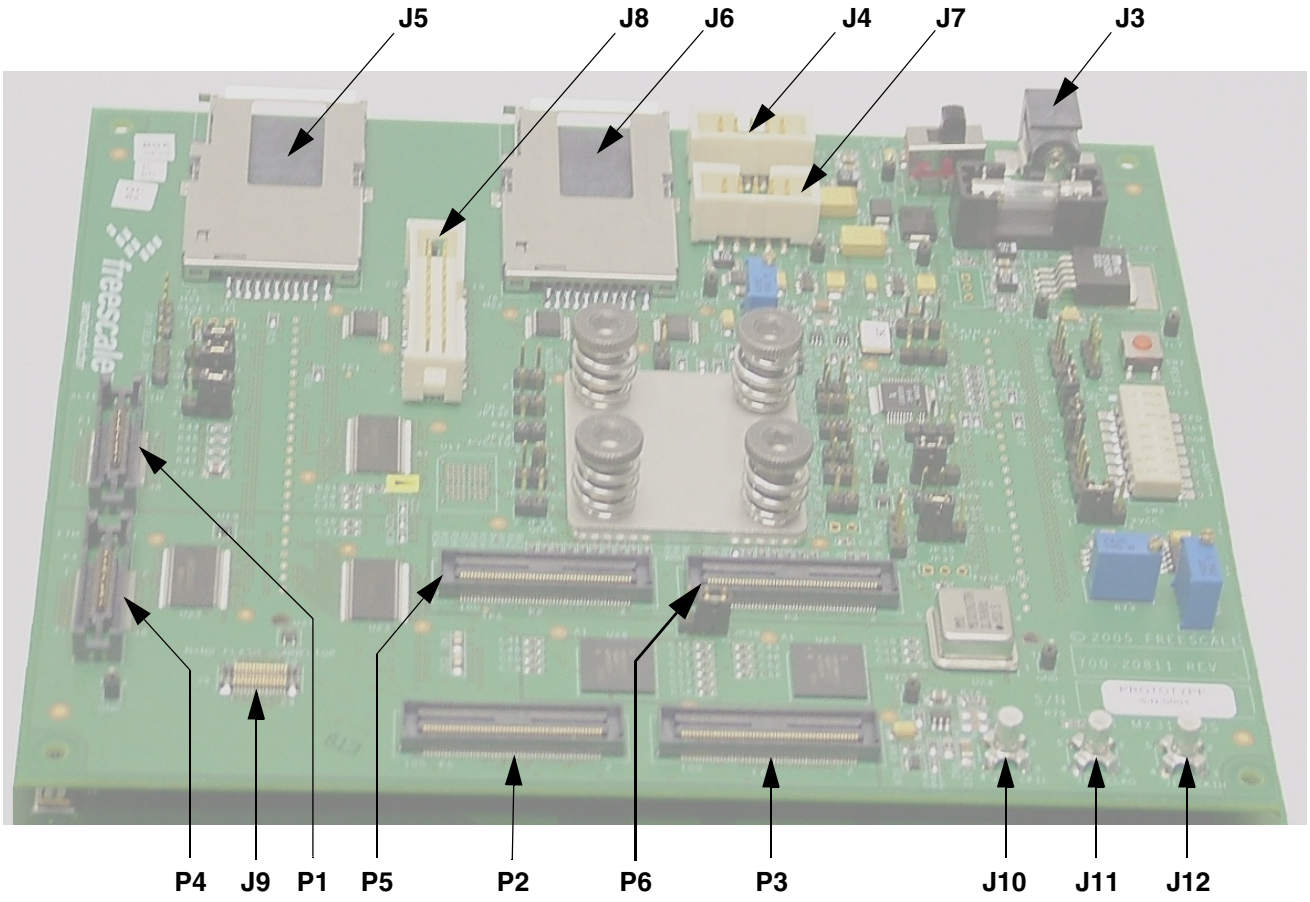
Pin	Signal	Description
1	TCK	JTAG CLOCK
2	GND	SIGNAL GROUND
3	TMS	JTAG MODE
4	GND	SIGNAL GROUND
5	TDI	JTAG DATA IN
6	3V3	3 VDC POWER
7	TDO	JTAG DATA OUT
8	GND	SIGNAL GROUND
9	NC	NO CONNECTION
10	NC	NO CONNECTION

4.3 CPU Board Connectors

Table 4-37 shows the CPU board connectors. Table 4-29 shows connector layout on the board. See paragraph 4.2 for information about CPU board connectors J1 and J2, which mate with connectors P1 and P2 of the Base board.

Table 4-37. CPU Board Connectors

Connector	Type	Description
J1	215-pin	Base/CPU 1 (see Base board for connector description)
J2	215-pin	Base/CPU 2 (see Base board for connector description)
J3	DIN	ADS Power Input
J4	10-pin header	PC Test
J5	Memory Card	Memory Stick
J6	Memory Card	Memory Stick
J7	10-pin header	In-circuit Serial Programming
J8	20-pin header	JTAG Interface
J9	Edge Connector	NAND Flash Connector
J10	Subminiature Jack	External 32 kHz Clock Input (CKIL)
J11	Subminiature Jack	MCU CLK0 Output
J12	Subminiature Jack	External 26 MHz Clock Input (CKIH)
P1	60-pin	Alternate ETM
P2	100-pin	SAMTEC
P3	100-pin	SAMTEC
P4	60-pin	Primary ETM
P5	100-pin	SAMTEC
P6	100-pin	SAMTEC



NOTE: J1 AND J2 ARE LOCATED ON THE UNDERSIDE OF THE BOARD.

Figure 4-29. CPU Board Connectors

4.3.1 Logic Analyzer Connectors

P2, P3, P5, and P6 are the CPU board logic analyzer connectors. All are 100-pin SAMTEC connectors.

Figure 4-30 shows P2 pin assignments and Table 4-38 describes P2 signals.

Figure 4-31 shows P3 pin assignments and Table 4-39 describes P3 signals.

Figure 4-32 shows P5 pin assignments and Table 4-40 describes P5 signals.

Figure 4-33 shows P6 pin assignments and Table 4-40 describes P6 signals.

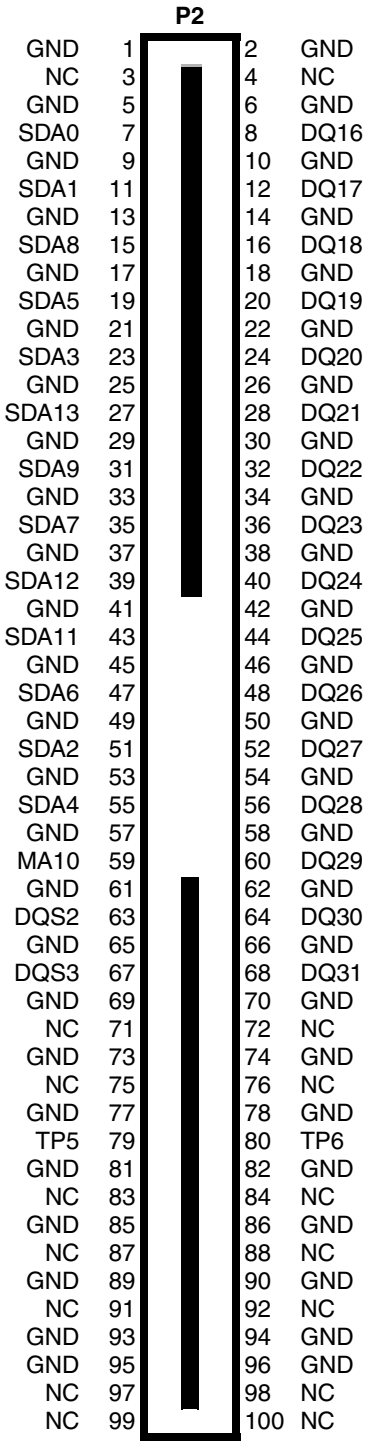


Figure 4-30. Logic Analyzer Connector P2 Pin Assignment

Table 4-38. Logic Analyzer Connector P2 Signal Description

Signal	Pin	Description
DQ16	8	DDR DATA
DQ17	12	DDR DATA
DQ18	16	DDR DATA
DQ19	20	DDR DATA
DQ20	24	DDR DATA
DQ21	28	DDR DATA
DQ22	32	DDR DATA
DQ23	36	DDR DATA
DQ24	40	DDR DATA
DQ25	44	DDR DATA
DQ26	48	DDR DATA
DQ27	52	DDR DATA
DQ28	56	DDR DATA
DQ29	60	DDR DATA
DQ30	64	DDR DATA
DQ31	68	DDR DATA
DQS2	63	DDR CONTROL
DQS3	67	DDR CONTROL
GND	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 73, 74, 77, 78, 81, 82, 85, 86, 89, 90, 93, 94, 95, 96	GROUND SIGNAL
MA10	59	DDR ADDRESS
NC	3, 4, 71, 72, 75, 76, 83, 84, 87, 88, 91, 92, 97, 98, 99, 100	NOT CONNECT
SDA0	7	DDR ADDRESS
SDA1	11	DDR ADDRESS
SDA2	51	DDR ADDRESS
SDA3	23	DDR ADDRESS
SDA4	55	DDR ADDRESS
SDA5	19	DDR ADDRESS
SDA6	47	DDR ADDRESS
SDA7	35	DDR ADDRESS
SDA8	15	DDR ADDRESS
SDA9	31	DDR ADDRESS
SDA11	43	DDR ADDRESS
SDA12	39	DDR ADDRESS
SDA13	27	DDR ADDRESS
TP5	79	NOT CONNECT
TP6	80	NOT CONNECT

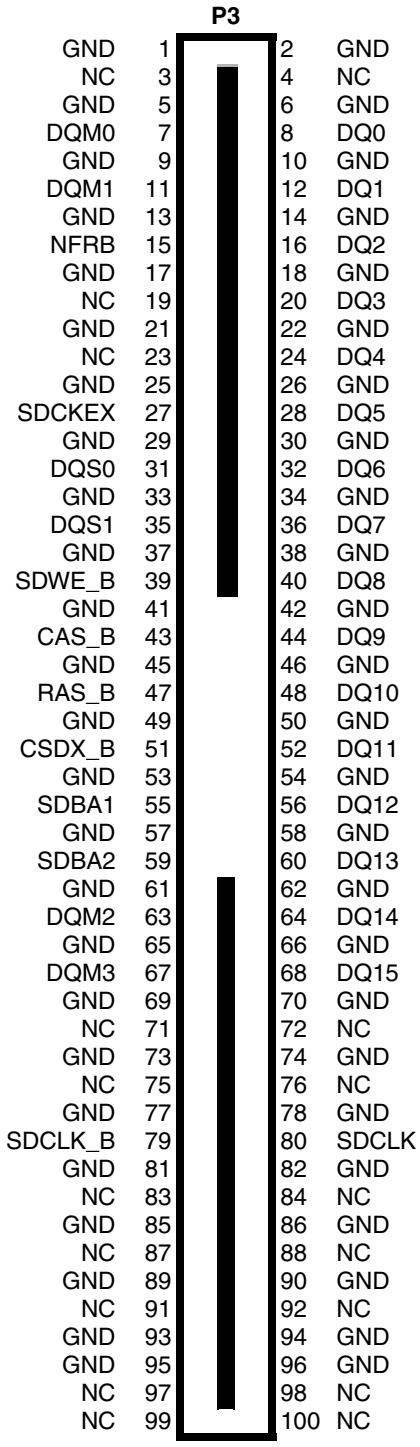


Figure 4-31. Logic Analyzer Connector P3 Pin Assignment

Table 4-39. Logic Analyzer Connector P3 Signal Description

Signal	Pin	Description
CAS_B	43	DDR CONTROL
CSDX_B	51	DDR CONTROL
DQ0	8	DDR DATA
DQ1	12	DDR DATA
DQ2	16	DDR DATA
DQ3	20	DDR DATA
DQ4	24	DDR DATA
DQ5	28	DDR DATA
DQ6	32	DDR DATA
DQ7	36	DDR DATA
DQ8	40	DDR DATA
DQ9	44	DDR DATA
DQ10	48	DDR DATA
DQ11	52	DDR DATA
DQ12	56	DDR DATA
DQ13	60	DDR DATA
DQ14	64	DDR DATA
DQ15	68	DDR DATA
DQM0	7	DDR CONTROL
DQM1	11	DDR CONTROL
DQM2	63	DDR CONTROL
DQM3	67	DDR CONTROL
DQS0	31	DDR CONTROL
DQS1	35	DDR CONTROL
GND	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 73, 74, 77, 78, 81, 82, 85, 86, 89, 90, 93, 94, 95, 96	GROUND SIGNAL
NC	3, 4, 19, 23, 71, 72, 75, 76, 83, 84, 87, 88, 91, 92, 97, 98, 99, 100	NOT CONNECT
NFRB	15	NAND FLASH READ
RAS_B	47	DDR CONTROL
SDBA1	55	DDR CONTROL
SDBA2	59	DDR CONTROL
SDCKEX	27	DDR CONTROL
SDCLK	80	DDR CLOCK
SDCLK_B	79	DDR CLOCK
SDWE_B	39	DDR CONTROL

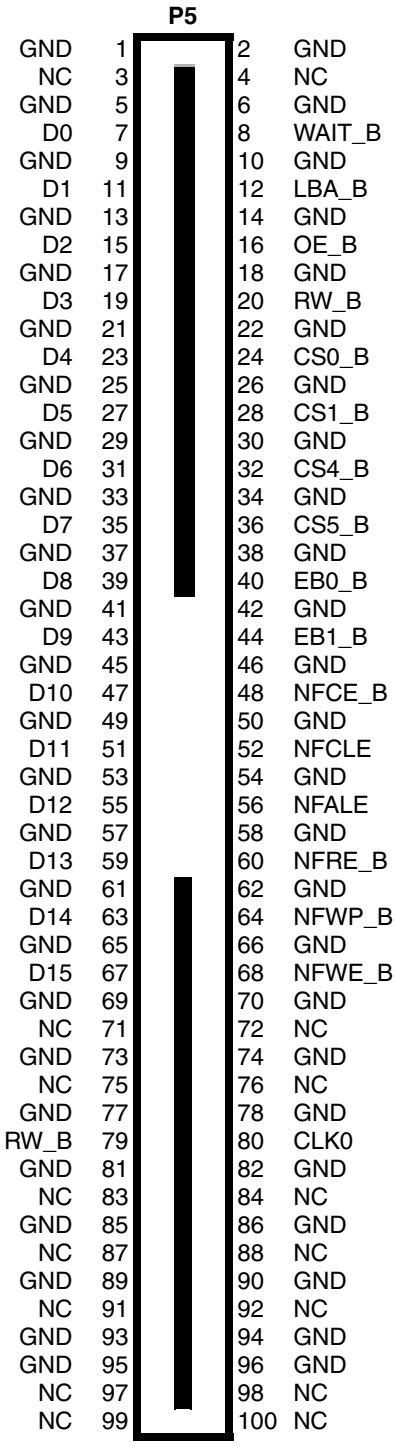


Figure 4-32. Logic Analyzer Connector P5 Pin Assignment

Table 4-40. Logic Analyzer Connector P5 Signal Description

Signal	Pin	Description
CLKO	80	CLOCK OUT
CS0_B	24	BUFFERED CHIP SELECT
CS1_B	28	BUFFERED CHIP SELECT
CS4_B	32	BUFFERED CHIP SELECT
CS5_B	36	BUFFERED CHIP SELECT
D0	7	EMI DATA
D1	11	EMI DATA
D2	15	EMI DATA
D3	19	EMI DATA
D4	23	EMI DATA
D5	27	EMI DATA
D6	31	EMI DATA
D7	35	EMI DATA
D8	39	EMI DATA
D9	43	EMI DATA
D10	47	EMI DATA
D11	51	EMI DATA
D12	55	EMI DATA
D13	59	EMI DATA
D14	63	EMI DATA
D15	67	EMI DATA
EB0_B	40	EMI CONTROL
EB1_B	44	EMI CONTROL
GND	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 73, 74, 77, 78, 81, 82, 85, 86, 89, 90, 93, 94, 95, 96	SIGNAL GROUND
LBA_B	12	EMI CONTROL
MA10	59	DDR ADDRESS
NC	3, 4, 71, 72, 75, 76, 83, 84, 87, 88, 91, 92, 97, 98, 99, 100	NOT CONNECTED
NFALE	56	NAND FLASH CONTROL
NFCE_B	48	NAND FLASH CONTROL
NFCLE	52	NAND FLASH CONTROL
NFRE_B	60	NAND FLASH CONTROL
NFWE_B	68	NAND FLASH CONTROL
NFWP_B	64	NAND FLASH CONTROL
OE_B	16	EMI CONTROL
PW_B	79	EMI CONTROL
RW_B	20	EMI CONTROL
WAIT_B	8	EMI CONTROL

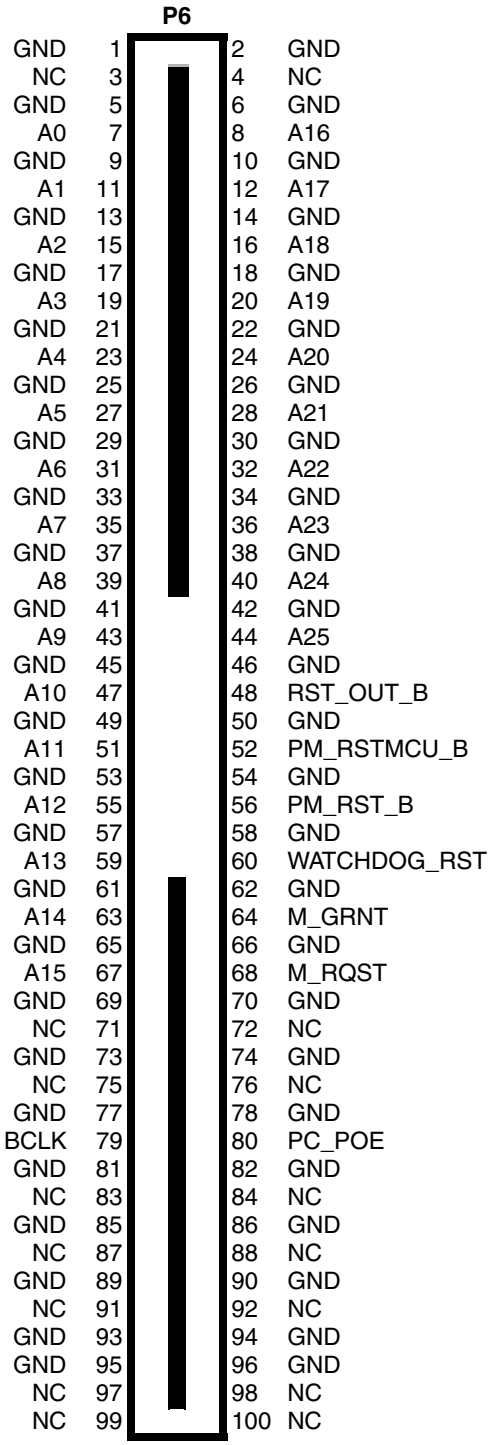


Figure 4-33. Logic Analyzer Connector P6 Pin Assignment

Table 4-41. Logic Analyzer Connector P6 Signal Description

Signal	Pin	Description
A0	7	EMI ADDRESS
A1	11	EMI ADDRESS
A2	15	EMI ADDRESS
A3	19	EMI ADDRESS
A4	23	EMI ADDRESS
A5	27	EMI ADDRESS
A6	31	EMI ADDRESS
A7	35	EMI ADDRESS
A8	39	EMI ADDRESS
A9	43	EMI ADDRESS
A10	47	EMI ADDRESS
A11	51	EMI ADDRESS
A12	55	EMI ADDRESS
A13	59	EMI ADDRESS
A14	63	EMI ADDRESS
A15	67	EMI ADDRESS
A16	8	EMI ADDRESS
A17	12	EMI ADDRESS
A18	16	EMI ADDRESS
A19	20	EMI ADDRESS
A20	24	EMI ADDRESS
A21	28	EMI ADDRESS
A22	32	EMI ADDRESS
A23	36	EMI ADDRESS
A24	40	EMI ADDRESS
A25	44	EMI ADDRESS
BCLK	79	BUFFERED CLOCK
GND	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62, 65, 66, 69, 70, 73, 74, 77, 78, 81, 82, 85, 86, 89, 90, 93, 94, 95, 96	SIGNAL GROUND
M_GRNT	64	EMI CONTROL
M_RQST	68	EMI CONTROL
MA10	59	DDR ADDRESS
NC	3, 4, 71, 72, 75, 76, 83, 84, 87, 88, 91, 92, 97, 98, 99, 100	NOT CONNECTED
PC_POE	80	PCMCIA CONTROL
PM_RST_B	56	PCMCIA CONTROL
PM_RSTMCU_B	52	POWER MANAGEMENT MCU RESET
RST_OUT_B	48	RESET OUT — Active low reset signal from the MCU
WATCHDOG_RST	60	WATCHDOG RESET

4.3.2 ETM Connectors

P4 and P1 are the CPU board ETM connectors. P4 is the primary connector and P1 is the alternate connector.

Figure 4-34 shows P4 pin assignments and Table 4-42 describes P4 signals.

Figure 4-35 shows P1 pin assignments and Table 4-43 describes P1 signals.

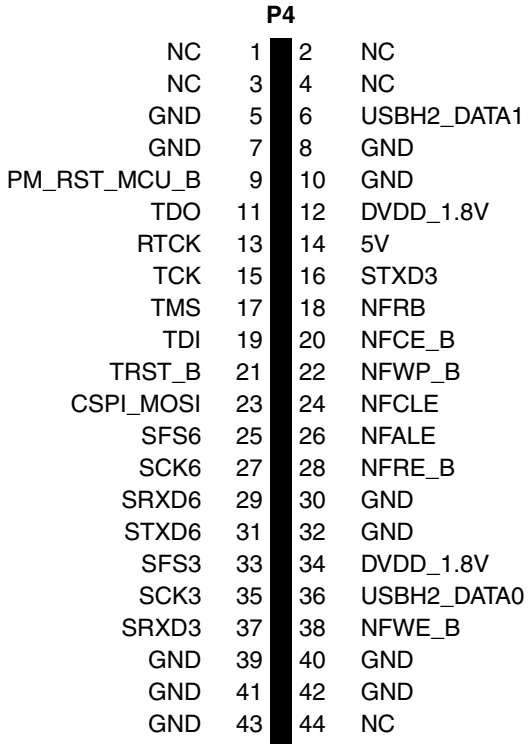


Figure 4-34. Primary ETM Connector P4 Pin Assignment

Table 4-42. Primary ETM Connector P4 Signal Description

Pin	Signal	Description
1-4	NC	NOT CONNECTED
5	GND	SIGNAL GROUND
6	USBH2_DATA1	TRACE CLOCK
7, 8	GND	SIGNAL GROUND
9	PM_RST_MCU_B	POWER MANAGEMENT MCU RESET
10	GND	SIGNAL GROUND
11	TDO	JTAG DATA OUT
12	DVDD_1.8V	1.8V VCC POWER
13	RTCK	JTAG RETURN CLOCK
14	5V	5V VCC POWER
15	TCK	JTAG CLOCK
16	STXD3	TRACE DATA
17	TMS	JTAG MODE
18	NFRB	TRACE DATA
19	TDI	JTAG DATA IN
20	NFCE_B	TRACE DATA
21	TRST_B	JTAG RESET
22	NFWP_B	TRACE DATA
23	CSPI_MOSI	TRACE DATA
24	NFCLE	TRACE DATA
25	SFS6	TRACE DATA
26	NFALE	TRACE DATA
27	SCK6	TRACE DATA
28	NFRE_B	TRACE DATA
29	SRXD6	TRACE DATA
30	GND	SIGNAL GROUND
31	STXD6	TRACE DATA
32	GND	SIGNAL GROUND
33	SFS3	TRACE DATA
34	DVDD_1.8V	1.8V VCC POWER
35	SCK3	TRACE DATA
36	USBH2_DATA0	TRACE CONTROL
37	SRXD3	TRACE DATA
38	NFWE_B	TRACE DATA
39-44	GND	SIGNAL GROUND

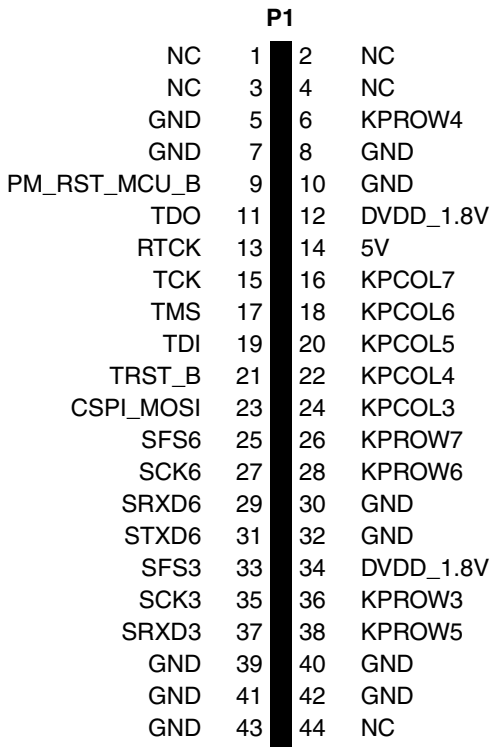


Figure 4-35. Alternate ETM Connector P1 Pin Assignment

Table 4-43. Alternate ETM Connector P1 Signal Description

Pin	Signal	Description
1-4	NC	NOT CONNECTED
5	GND	SIGNAL GROUND
6	KPROW4	TRACE CLOCK
7, 8	GND	SIGNAL GROUND
9	PM_RST_MCU_B	POWER MANAGEMENT MCU RESET
10	GND	SIGNAL GROUND
11	TDO	JTAG DATA OUT
12	DVDD_1.8V	1.8V VCC POWER
13	RTCK	JTAG RETURN CLOCK
14	5V	5V VCC POWER
15	TCK	JTAG CLOCK
16	KPCOL7	TRACE DATA
17	TMS	JTAG MODE
18	KPCOL6	TRACE DATA
19	TDI	JTAG DATA IN
20	KPCOL5	TRACE DATA
21	TRST_B	JTAG RESET
22	KPCOL4	TRACE DATA
23	CSPI_MOSI	TRACE DATA
24	KPCOL3	TRACE DATA
25	SFS6	TRACE DATA
26	KPROW7	TRACE DATA
27	SCK6	TRACE DATA
28	KPROW6	TRACE DATA
29	SRXD6	TRACE DATA
30	GND	SIGNAL GROUND
31	STXD6	TRACE DATA
32	GND	SIGNAL GROUND
33	SFS3	TRACE DATA
34	DVDD_1.8V	1.8V VCC POWER
35	SCK3	TRACE DATA
36	KPROW3	TRACE CONTROL
37	SRXD3	TRACE DATA
38	KPROW5	TRACE DATA
39-44	GND	SIGNAL GROUND

4.3.3 RV ICE/JTAG Connector

J8 is the CPU board RV ICE/JTAG connector. Figure 4-36 shows pin assignments and Table 4-44 describes signals.

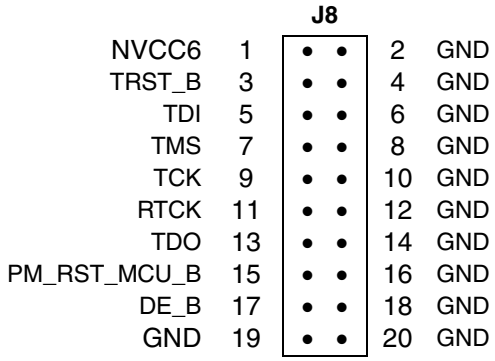


Figure 4-36. RV ICE/JTAG Connector J8 Pin Assignment

Table 4-44. RV ICE/JTAG Connector J8 Signal Description

Pin	Signal	Description
1	NVCC6	VDC POWER
2	GND	SIGNAL GROUND
3	TRST_B	TARGET RESET
4	GND	TEST MODE SELECT
5	TDI	TEST DATA INPUT
6	GND	RETURN CLOCK
7	TMS	TEST MODE SELECT
8	GND	RESET IN
9	TCK	TEST CLOCK
10	GND	SIGNAL GROUND
11	RTCK	RETURN CLOCK
12	GND	SIGNAL GROUND
13	TDO	JTAG TEST DATA OUTPUT
14	GND	SIGNAL GROUND
15	PM_RST_MCU_B	POWER MANAGEMENT MCU RESET
16	GND	SIGNAL GROUND
17	DE_B	DEBUG ENABLE
18	GND	SIGNAL GROUND
19	GND	SIGNAL GROUND
20	GND	SIGNAL GROUND

4.3.4 PC Test Connector

J4 is the CPU board PC Test connector. Figure 4-37 shows pin assignments and Table 4-45 describes signals.

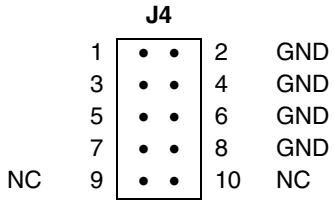


Figure 4-37. PC Test Connector J4 Pin Assignment

Table 4-45. PC Test Connector J4 Signal Description

Pin	Signal	Description
1		DEBUG INTERNAL USE
2	GND	SIGNAL GROUND
3		DEBUG INTERNAL USE
4	GND	SIGNAL GROUND
5		DEBUG INTERNAL USE
6	GND	SIGNAL GROUND
7		DEBUG INTERNAL USE
8	GND	SIGNAL GROUND
9	NC	NO CONNECTION
10	NC	NO CONNECTION

4.3.5 In-circuit Serial Programming Connector

J7 is the CPU board ISP connector. Figure 4-38 shows pin assignments and Table 4-46 describes signals.

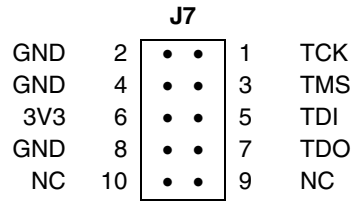


Figure 4-38. ISP Connector J7 Pin Assignment

Table 4-46. ISP Connector J7 Signal Description

Pin	Signal	Description
1	TCK	JTAG CLOCK
2	GND	SIGNAL GROUND
3	TMS	JTAG MODE
4	GND	SIGNAL GROUND
5	TDI	JTAG DATA IN
6	3V3	3 VDC POWER
7	TDO	JTAG DATA OUT
8	GND	SIGNAL GROUND
9	NC	NO CONNECTION
10	NC	NO CONNECTION

4.3.6 NAND Flash Connector

J9 on the CPU board allows the ADS to interface with a NAND Flash module. Figure 4-39 shows pin assignments and Table 4-47 describes connector signals.

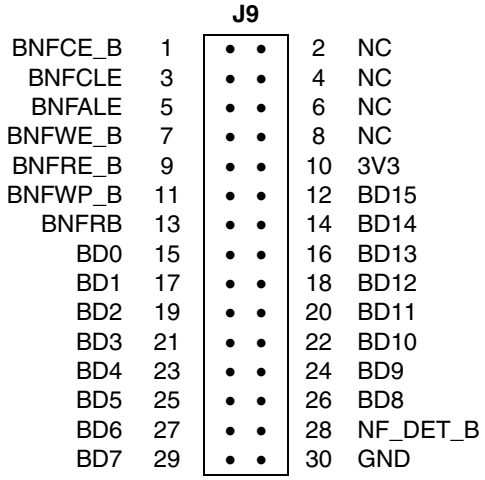


Figure 4-39. NAND Flash Connector J9 Pin Assignment

Table 4-47. NAND Flash Connector J9 Signal Description

Pin(s)	Signal	Description
1	BNFCE_B	NAND FLASH CHIP ENABLE
2	NC	NOT CONNECTED
3	BNFCLE	NAND FLASH COMMAND LATCH ENABLE
4	NC	NOT CONNECTED
5	BNFALE	NAND FLASH ADDRESS LATCH ENABLE
6	NC	NOT CONNECTED
7	BNFWE_B	NAND FLASH WRITE ENABLE
8	NC	NOT CONNECTED
9	BNFRE_B	NAND FLASH READ ENABLE
10	3V3	3 VDC POWER
11	BNFWP_B	NAND FLASH WRITE PROTECT
12	BD15	BIDIRECTIONAL DATA 15
13	BNFRB	NAND FLASH READY/BUSY
14	BD14	BIDIRECTIONAL DATA 14
15	BD0	BIDIRECTIONAL DATA 0
16	BD13	BIDIRECTIONAL DATA 13
17	BD1	BIDIRECTIONAL DATA 1
18	BD12	BIDIRECTIONAL DATA 12
19	BD2	BIDIRECTIONAL DATA 2
20	BD11	BIDIRECTIONAL DATA 11
21	BD3	BIDIRECTIONAL DATA 3
22	BD10	BIDIRECTIONAL DATA 10
23	BD4	BIDIRECTIONAL DATA 4
24	BD9	BIDIRECTIONAL DATA 9
25	BD5	BIDIRECTIONAL DATA 5
26	BD8	BIDIRECTIONAL DATA 8
27	BD6	BIDIRECTIONAL DATA 6
28, 30	GND	GROUND
29	BD7	BIDIRECTIONAL DATA 7

4.3.7 Memory Stick Connectors

J5 and J6 on the CPU board allows the ADS to interface Memory Stick modules. Table 4-48 describes J5 signals. Table 4-49 describes J6 signals.

Table 4-48. Memory Stick Connector J5 Signal Description

Pin	Signal	Description
1	GND	SIGNAL GROUND
2	MSHC1_BS	MS 1
3	MSHC1_DATA 1	MS 1 DATA 1
4	MSHC1_DATA 0	MS 1 DATA 0
5	MSHC1_DATA 2	MS 1 DATA 2
6	MSHC1_DET	MS 1 DETECT
7	MSHC1_DATA 3	MS 1 DATA 3
8	MSHC1_SCLK	MS 1 SERIAL CLOCK
9	VSD1	MS 1 POWER
10	GND	SIGNAL GROUND

Table 4-49. Memory Stick Connector J6 Signal Description

Pin	Signal	Description
1	GND	SIGNAL GROUND
2	MSHC2_BS	MS 2
3	MSHC2_DATA 1	MS 2 DATA 1
4	MSHC2_DATA 0	MS 2 DATA 0
5	MSHC2_DATA 2	MS 2 DATA 2
6	MSHC2_DET	MS 2 DETECT
7	MSHC2_DATA 3	MS 2 DATA 3
8	MSHC2_SCLK	MS 2 SERIAL CLOCK
9	VSD2	MS 2 POWER
10	GND	SIGNAL GROUND

4.3.8 Subminiature Clock Connectors

Subminiature jacks J10, J11, and J12 provide external clock signal connections. J10 provides an input for the 32 KHz low-speed clock signal CKIL, J11 provides the MCU CLK0 output signal, and J12 provides an input for the 26 MHz high-speed clock signal CKIH.

4.3.9 Power Connector

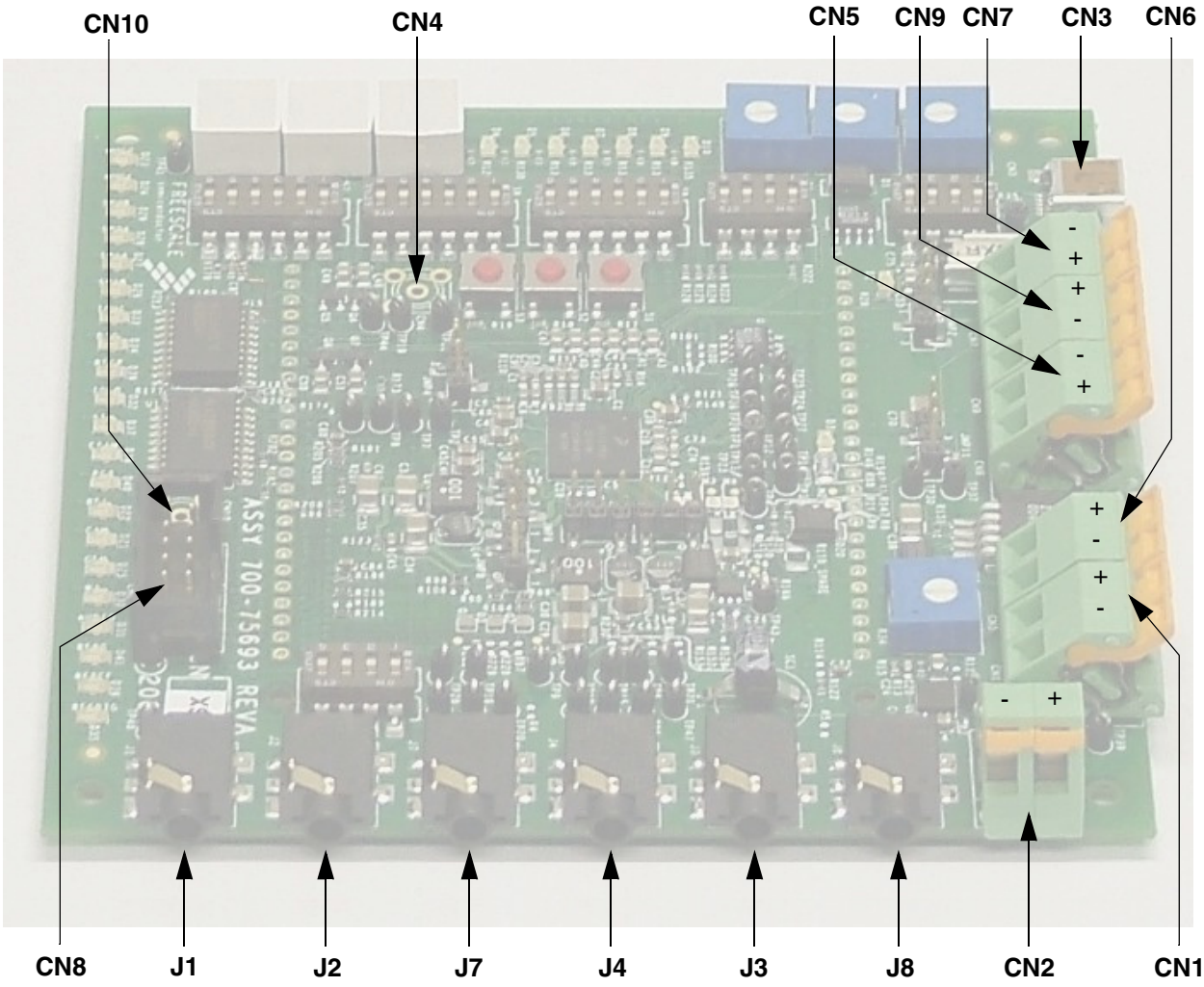
J3 is the power connector for the CPU board and the ADS. It is a DIN type barrel connector.

4.4MC13783 Board Connectors

The MC13783 Audio and Power Management chip is a multifunctional device with a number of capabilities. The ADS Base board provides access to many of these functions, but some are directly accessible on the MC13783 board itself. Table 4-50 describes MC13783 Board connector functions. Figure 4-40 shows the locations of the connectors on the MC13783 board. See paragraph 4.2 for descriptions of MC13783 board connectors J5 and J6, which mate with connectors P5 and P6 of the Base board.

Table 4-50. MC13783 Board Connectors

Connector	Type	Description
CN1	Wire Clamp Terminals	Right Stereo Speaker Output
CN2	Wire Clamp Terminals	Earpiece Speaker Output (Mono)
CN3	USB Connector	MC13783 USB Interface
CN4	Subminiature A	External 32 kHz Clock Input
CN5	Wire Clamp Terminals	Battery Charger Input
CN6	Wire Clamp Terminals	Left Stereo Speaker Output
CN7	Wire Clamp Terminals	External Battery Input
CN8	10-pin Header	MC13783 Touch Screen Interface
CN9	Wire Clamp Terminals	Lithium Battery Input
CN10	Subminiature A	External Audio Bus Clock Input (CLIA, CLIB)
J1	Miniature Audio Jack	RX Line Input (Stereo)
J2	Miniature Audio Jack	RX Line Output (Stereo)
J3	Miniature Audio Jack	Headset Microphone Input 2 (Mono)
J4	Miniature Audio Jack	Handset Microphone Input 1 (Stereo)
J5	215-pin	Connects MC13783 board to Base board
J6	215-pin	Connects MC13783 board to Base board
J7	Miniature Audio Jack	TX Line Input
J8	Miniature Audio Jack	Headphone Output (Stereo)



NOTE: J5 AND J6 ARE LOCATED ON THE UNDERSIDE OF THE BOARD.

Figure 4-40. MC13783 Boarc Connectors

4.4.1 Power Connectors

CN5, CN7, and CN9 are pairs of wire clamp terminals that provide for connection of external batteries and a battery charger. Each pair of terminals provides one power input connection and one power ground connection.

4.4.2 Audio Connectors

All the audio connectors on the MC13783 board provide connections to the audio function pins of the MC13783. See the specification sheet (on the ADS CD) for detailed signal and drive specifications.

4.4.2.1 Miniature Audio Jacks

Audio connectors J1-J4, J7, and J8 are standard stereo mini-jacks. Figure 4-41 shows jack terminals. Table 4-51 describes the signals and termination.

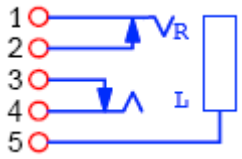


Figure 4-41. Audio Jack Diagram

Table 4-51. Audio Jack Signal Descriptions

Jack	Termination				
	1	2	3	4	5
1	RXINL	NC	NC	RXINR	GND
2	RXOUTL	NC	NC	RXOUTR	GND
3	GND	NC	NC	MC2IN	GND
4	MC1RIN	NC	NC	MC1LIN	GND
7	TXIN	NC	NC	GND	GND
8	HSL	NC	GND	HSR	GND

Signal Description	
RXINL	RX IN LEFT
RXINR	RX IN RIGHT
RXOUTL	RX OUT LEFT
RXOUTR	RX OUT RIGHT
MC2IN	MICROPHONE 2 ANALOG INPUT
MC1RIN	MICROPHONE 1 ANALOG INPUT RIGHT
MC1LIN	MICROPHONE 1 ANALOG INPUT LEFT
TXIN	TX INPUT
HSL	HEADSET ANALOG OUTPUT LEFT
HPOUTR	HEADSETANALOG OUTPUT RIGHT
GND	SIGNAL GROUND

4.4.2.2 Audio Terminals

CN1, CN2, and CN6 are pairs of wire clamp terminals that provide for connection of external speakers. CN1 and CN6 provide connections for left and right stereo speakers. CN6 provides a connection for an earpiece speaker. All have one analog signal connection and one signal ground connection.

4.4.3 USB OTG Connector

CN3 is a USB mini AB connector. It connects to the MC13783 USB OTG interface. Figure 4-42 shows pin assignments and Table 4-52 describes the signals.

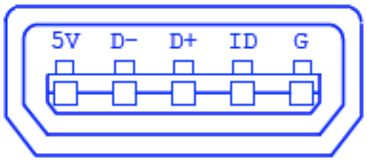


Figure 4-42. USB OTG Connector CN3 Pin Assignment

Table 4-52. USB Connector CN3 Signal Description

Pin	Signal	Description
1	5V	5 VDC BUS VOLTAGE
2	D-	USB DATA MINUS
3	D+	USB DATA PLUS
4	ID	BUS ID
5	GND	GROUND

4.4.4 Touchscreen Connector

CN8 connects to the MC13783 touch screen interface pins. Figure 4-43 shows pin assignments and Table 4-53 describes the signals.

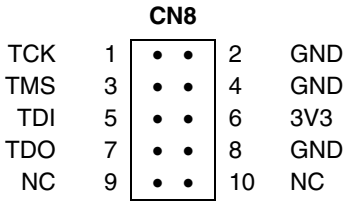


Figure 4-43. Touchscreen Connector CN8 Pin Assignment

Table 4-53. Touchscreen Connector CN8 Signal Description

Pin	Signal	Description
1	TSX1	TOUCH SCREEN X-AXIS 1
2	GND	SIGNAL GROUND
3	TSX2	TOUCH SCREEN X-AXIS 2
4	GND	SIGNAL GROUND
5	GND	SIGNAL GROUND
6	GND	SIGNAL GROUND
7	TSY1	TOUCH SCREEN Y-AXIS 1
8	GND	SIGNAL GROUND
9	TSY2	TOUCH SCREEN Y-AXIS 2
10	GND	NO CONNECTION

4.4.5 Subminiature Clock Connectors

Subminiature connectors CN4 and CN10 provide external clock signal connections. CN4 provides an external input for the 32 KHz clock signal. CN10 provides an input for the MC13783 audio bus clock signals CLIA and CLIB.