**Advance Information**

MPC8255TS/D
Rev. 2.2, 10/2001

MPC8255
PowerQUICC ™ II
Technical Summary

**M MOTOROLA** intelligence everywhere™

*digitaldna*™

Freescale Semiconductor, Inc.

The MPC8255 PowerQUICC II™ is a versatile communications processor that integrates a high-performance RISC microprocessor that implements the PowerPC architecture, a flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems. The MPC8255 is a Footprint-compatible, lower-cost version of the MPC8260.

The core is an embedded variant of the 603e microprocessor, referred to as the G2 core, with 16 Kbytes of instruction cache, 16 Kbytes of data cache, and a floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system (and many other peripherals), making this device a complete system on a chip.

The communications processor module (CPM) includes all the peripherals found in the MPC860, with the addition of two high-performance communications channels that support new emerging protocols (for example, 155-Mbps ATM and Fast Ethernet). The MPC8255 has dedicated hardware that can handle up to 128 full-duplex, time-division-multiplexed logical channels.

This document describes the functional operation of the MPC8255, with an emphasis on peripheral functions. Additional information about this microprocessor can be found in the *MPC603e RISC Microprocessors User's Manual* (order number: MPC603EUM/AD).

## 1.1   Features

The following is an overview of the MPC8255 feature set:

- Dual-issue integer core
  — A core version of the MPC603e microprocessor
  — System core microprocessor supporting frequencies of 150–200 MHz
  — Separate 16-Kbyte data and instruction caches:
    – Four-way set associative
    – Physically addressed
    – LRU replacement algorithm
  — PowerPC architecture-compliant memory management unit (MMU)
  — Common on-chip processor (COP) test interface
  — High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones

> MIPS at 200 MHz)
>
> — Supports bus snooping for cache coherency
>
> — Floating-point unit (FPU)

- Low-power (less than 2.5 W in HiP3, less than 2.0 W in HiP4) See the MPC8260 Power Consumption Calculator on the Smart Networks Web Page for the 8260 Family at www.motorola.com.

- Separate power supply for internal logic (2.5 V in HiP3, 2.0 V in HiP4) and for I/O (3.3 V)

- Separate PLLs for G2 core and for the CPM

  - G2 core and CPM can run at different frequencies for power/performance optimization

  - Internal G2 core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios

  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios

- 64-bit data and 32-bit address 60x bus

  - Bus supports multiple master designs

  - Supports single- and four-beat burst transfers

  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

  - Supports data parity or ECC and address parity

- 32-bit data and 18-bit address local bus

  - Single-master bus, supports external slaves

  - Eight-beat burst transfers

  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

- System interface unit (SIU)

  - Clock synthesizer

  - Reset controller

  - Real-time clock (RTC) register

  - Periodic interrupt timer

  - Hardware bus monitor and software watchdog timer

  - IEEE 1149.1 JTAG test access port

- Twelve-bank memory controller

  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals

  - Byte write enables and selectable parity generation

  - 32-bit address decodes with programmable bank size

  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine

  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)

  - Dedicated interface logic for SDRAM

- Disable CPU mode

- Communications processor module (CPM)

  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals

— Interfaces to G2 core through on-chip 24-Kbyte dual-port RAM and DMA controller

— Serial DMA channels for receive and transmit on all serial channels

— Parallel I/O registers with open-drain and interrupt capability

— Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers

— Two fast communications controllers (FCC1 and FCC2) supporting the following protocols:

  – 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)

  – ATM—Full-duplex SAR at 155 Mbps, UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections

  – Transparent

  – HDLC—Up to T3 rates (clear channel)

— One multichannel controller (MCC2)

  – Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.

  – Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces

— Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:

  – Ethernet/IEEE 802.3 CDMA/CS

  – HDLC/SDLC and HDLC bus

  – Universal asynchronous receiver transmitter (UART)

  – Synchronous UART

  – Binary synchronous (BISYNC) communications

  – Transparent

— Two serial management controllers (SMCs), identical to those of the MPC860

  – Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

  – Transparent

  – UART (low-speed operation)

— One serial peripheral interface identical to the MPC860 SPI

— One $I^2C$ controller (identical to the MPC860 $I^2C$ controller)

  – Microwire compatible

  – Multiple-master, single-master, and slave modes

— Up to four TDM interfaces

  – Supports one group of four TDM channels for a total of four TDMs

  – 2,048 bytes of SI RAM

  – Bit or byte resolution

  – Independent transmit and receive routing, frame synchronization

  – Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Motorola interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

— Four independent 16-bit timers that can be interconnected as two 32-bit timers

# 1.2    MPC8255 Architecture Overview

As shown in Figure 1, the MPC8255 has three major functional blocks:

- 64-bit G2 core derived from the MPC603e with MMUs and cache
- System interface unit (SIU)
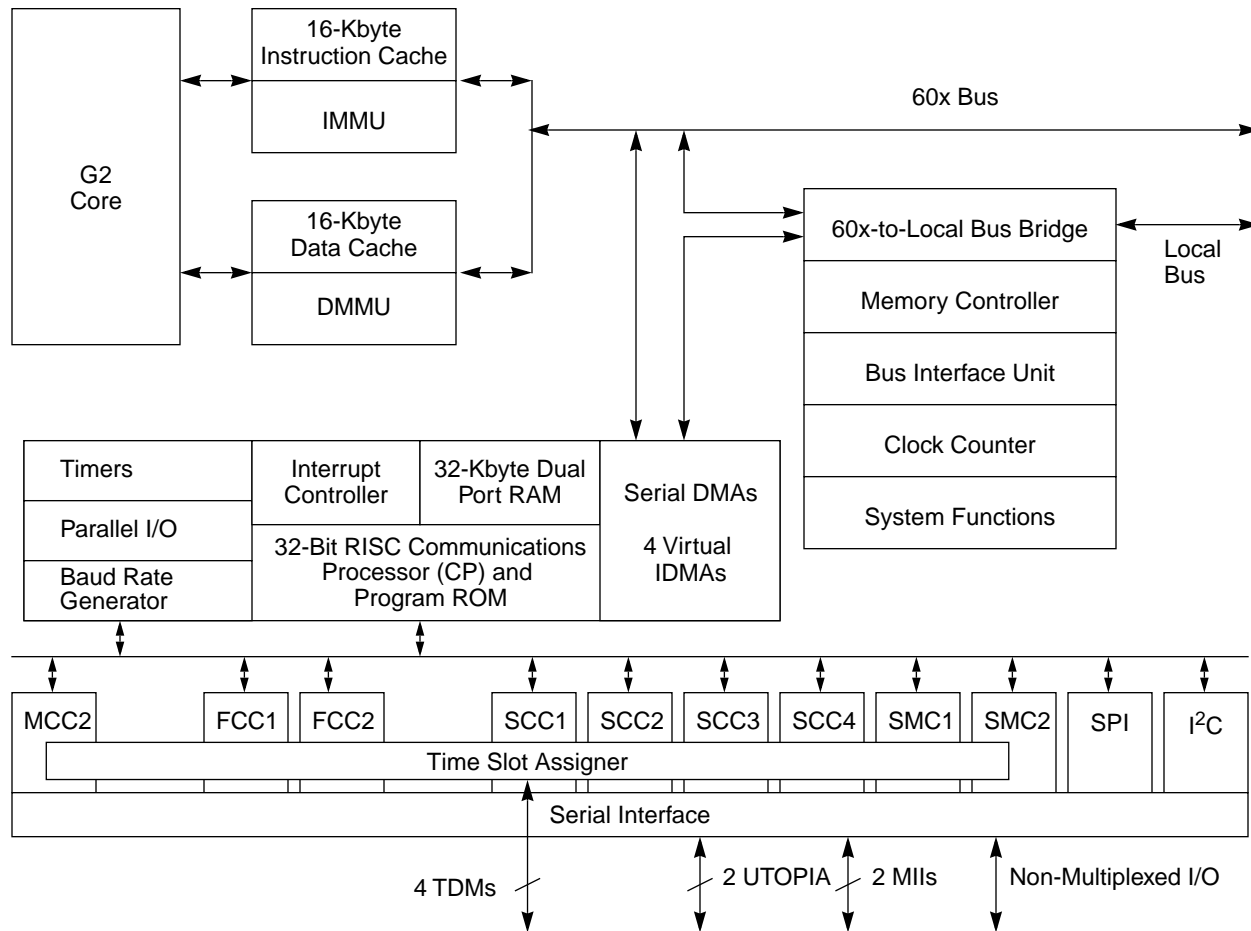- Communications processor module (CPM)



**Figure 1. MPC8255 Block Diagram**

The MPC8255 has two external buses to accommodate bandwidth requirements from the high-speed system core and the very fast communications channels.

Both the system core and the CPM have an internal PLL, which allows independent optimization of the frequencies at which they run. The system core and CPM are both connected to the 60x bus.

## 1.2.1    G2 Core

The G2 core is derived from the MPC603e microprocessor without the floating-point unit and with power management modifications. The core is a high-performance low-power implementation of the family of reduced instruction set computer (RISC) microprocessors that implement the PowerPC architecture. The G2

core implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses and integer data types of 8, 16, and 32 bits. The G2 cache provides snooping to ensure data coherency with other masters. This helps ensure coherency between the CPM and system core.

The core includes 16 Kbytes of instruction cache and 16 Kbytes of data cache. It has a 64-bit split-transaction external data bus which is connected directly to the external MPC8255 pins.

The G2 core has an internal common on-chip (COP) debug processor. This processor allows access to internal scan chains for debugging purposes. It is also used as a serial connection to the core for emulator support.

The G2 core performance for the SPEC95 benchmark for integer operations ranges between 4.4 and 5.1 at 200 MHz. In Dhrystone 2.1 MIPS, the G2 is 280 MIPS at 200 MHz (compared to the MPC860's 86 MIPS at 66 MHz).

The G2 core can be disabled. In this mode, the MPC8255 functions as a slave peripheral to an external core or to another MPC8255 device with its core enabled.

## 1.2.2 System Interface Unit (SIU)

The SIU consists of the following:

- A 60x-compatible parallel system bus configurable to 64-bit data width supports 64-, 32-, 16-, and 8-bit port sizes. The MPC8255 internal arbiter arbitrates between internal components that can access the bus (system core, CPM, and one external master). This arbiter can be disabled, and an external arbiter can be used if necessary.

- A local bus (32-bit data, 32-bit internal, and 18-bit external address)—This bus is used to enhance the operation of the very high-speed communications controllers. Without requiring extensive manipulation by the core, the bus can be used to store connection tables for ATM or buffer descriptors (BDs) for the communications channels or raw data that is transmitted between channels. The local bus is synchronous to the 60x bus and runs at the same frequency.

- A memory controller that supports 12 memory banks which can be allocated for either the system or the local bus. It supports all MPC860 features as well as SDRAM with page mode and address data pipeline. It also supports three user-programmable machines.

- A JTAG controller IEEE 1149.1 test access port (TAP)

- A bus monitor that prevents 60x bus lock-ups, a real-time clock, a periodic interrupt timer, and other system functions useful in embedded applications

- Glueless interface to L2 cache (MPC2605) and 4-/16-K-entry CAM (MCM69C232/MCM69C432)

## 1.2.3 Communications Processor Module (CPM)

The CPM contains features that allow the MPC8255 to excel in a variety of applications targeted mainly for networking and telecommunication markets.

The MPC8255 CPM is a superset of the MPC860 PowerQUICC™ CPM, with enhanced CP performance. The CPM also has additional hardware and microcode routines that support high bit rate protocols like ATM (up to 155 Mbps full-duplex) and Fast Ethernet (100-Mbps full-duplex).

The following list summarizes the major features of the CPM:

- The communications processor (CP) is an embedded 32-bit RISC controller residing on a separate bus (CPM local bus) from the 60x bus (used by the system core). With this separate bus, the CP does not affect the performance of the G2 core. The CP handles the lower layer tasks and DMA control activities, leaving the G2 core free to handle higher layer activities. The CP has an instruction set optimized for communications, but can also be used for general-purpose applications, relieving the system core of small often repeated tasks.

- Two serial DMAs (SDMAs) that can do simultaneous transfers, optimized for burst transfers to the 60x bus and to the local bus

- Two full-duplex, serial fast communications controllers (FCC1 and FCC2) supporting ATM (155 Mbps) protocol through UTOPIA2 interface (there are two UTOPIA interfaces on the MPC8255), IEEE 802.3 and Fast Ethernet protocols, HDLC up to E3 rates (45 Mbps) and totally transparent operation. Each FCC can be configured to transmit fully transparent and receive HDLC or vice-versa.

- One multichannel controller (MCC1) that can handle an aggregate of 128 x 64 Kbps HDLC or transparent channels, multiplexed on up to four TDM interfaces. The MCC also supports super-channels of rates higher than 64 Kbps and subchanneling of the 64-Kbps channels.

- Four full-duplex serial communications controllers (SCCs) supporting IEEE 802.3/Ethernet, high-level synchronous data link control, HDLC, local talk, UART, synchronous UART, BISYNC, and transparent.

- Two full-duplex serial management controllers (SMC) supporting GCI, UART, and transparent operations

- Serial peripheral interface (SPI) and $I^2C$ bus controllers

- Time-slot assigner (TSA) that supports multiplexing of data from any of the four SCCs, three FCCs, and two SMCs

## 1.3 Compatibility Issues

### 1.3.1 Software

The MPC8255 CPM features are similar to previous devices, such as the MPC860. The code flow ports easily from previous devices to the MPC8255, except for new protocols.

Although many registers are new, it is helpful to understand the programming models of the MC68360, MPC860, or MPC850 since most registers retain the old status and event bits. Note that the MPC8255 initialization code requires changes from the MPC860 initialization code

### 1.3.2 MPC8260 Hardware

The MPC8255 is a Footprint-compatible, drop-in replacement for the MPC8260 and is ideally suited for applications which do not require the additional performance provided by the MPC8260's higher core, CPM and bus frequencies. The MPC8255 runs at the maximum frequencies of 200 MHz on the core, 133 MHz on the CPM, and 50 MHz for the bus. Also, the MPC8255 has two FCCs and one MCC, whereas the MPC8260 has three FCCs and two MCCs.

As the MPC8260 family migrates to smaller geometries, the core voltage will reduce from 2.5 V to 1.8 V. A programmable voltage regulator is recommended for future compatibility. See the *MPC8260 Hardware Specifications* for the electrical requirements and the AC and DC characteristics.

# 1.4   MPC8255 Application Examples

The following section provides block diagrams of different MPC8255 applications. The MPC8255 is a very flexible device and can be configured to meet many system application needs. In order to build a system, many factors should be taken into consideration.

## 1.4.1   Examples of Communications Systems

Following are some examples of communications systems:

- Remote access server
- Regional office router
- LAN-to-WAN bridge router
- Cellular base station
- Telecom switch controller
- SONET transmission controller

### 1.4.1.1   Remote Access Server

See Figure 2 for a remote access server configuration.
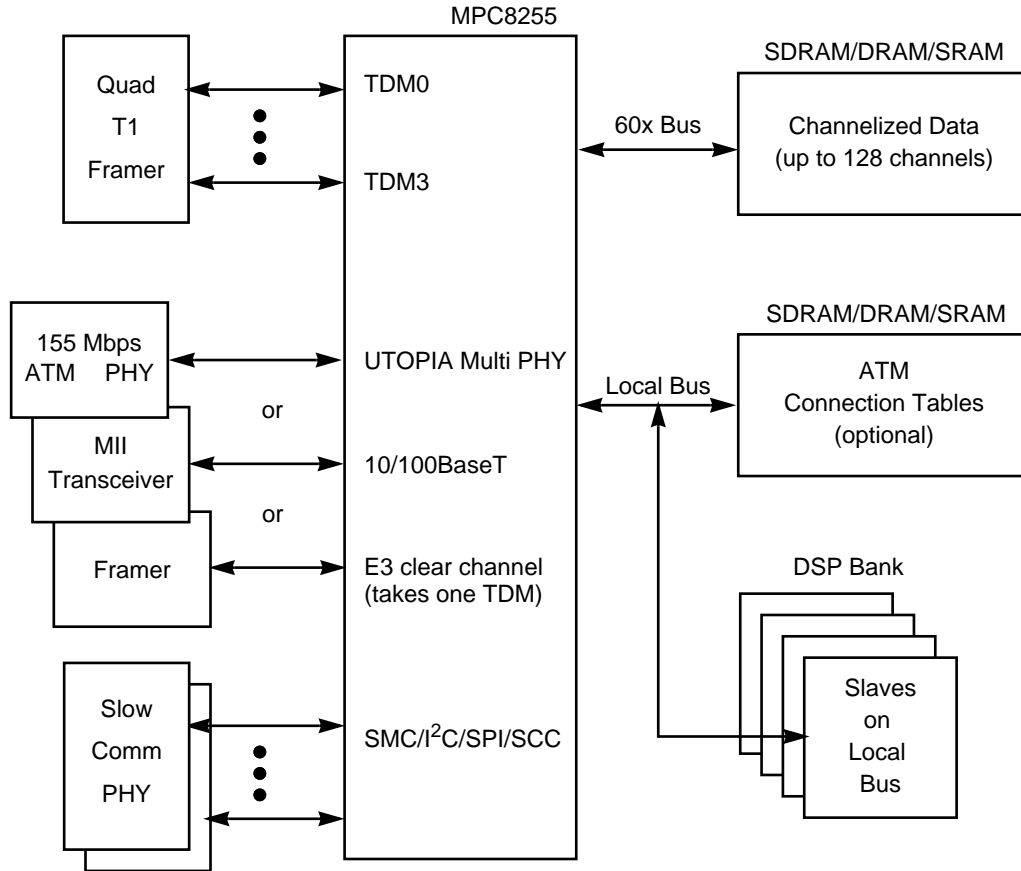
**Figure 2. Remote Access Server Configuration**

In this application, four TDM ports are connected to an external framer. In the MPC8255, the group of four ports support up to 128 channels. One TDM interface can support 32–128 channels. The MPC8255 receives and transmits data in transparent or HDLC mode, and stores or retrieves the channelized data from memory. The data can be stored either in memory residing on the 60x bus or in memory residing on the local bus.

The main trunk can be configured as one of the following:

- 155 Mbps full-duplex ATM, using the UTOPIA interface
- 10/100BaseT Fast Ethernet with MII interface
- High-speed serial channel (up to 45 Mbps).

In ATM mode, there may be a need to store connection tables in external memory on the local bus (if more than 128 active connections are needed). The need for local bus depends on the total throughput of the system. The MPC8255 supports automatic (without software intervention) cross connect between ATM and MCC, routing ATM AAL1 frames to MCC slots.

The local bus can be used as an interface to a bank of DSPs that can run code that performs analog modem signal modulation. Data to and from the DSPs can be transferred through the parallel bus with the internal virtual IDMA.

The MPC8255 memory controller supports many types of memories, including page-mode, pipeline SDRAM and EDO DRAM for efficient burst transfers.

## 1.4.1.2   Regional Office Router

Figure 3 shows a regional office router configuration.
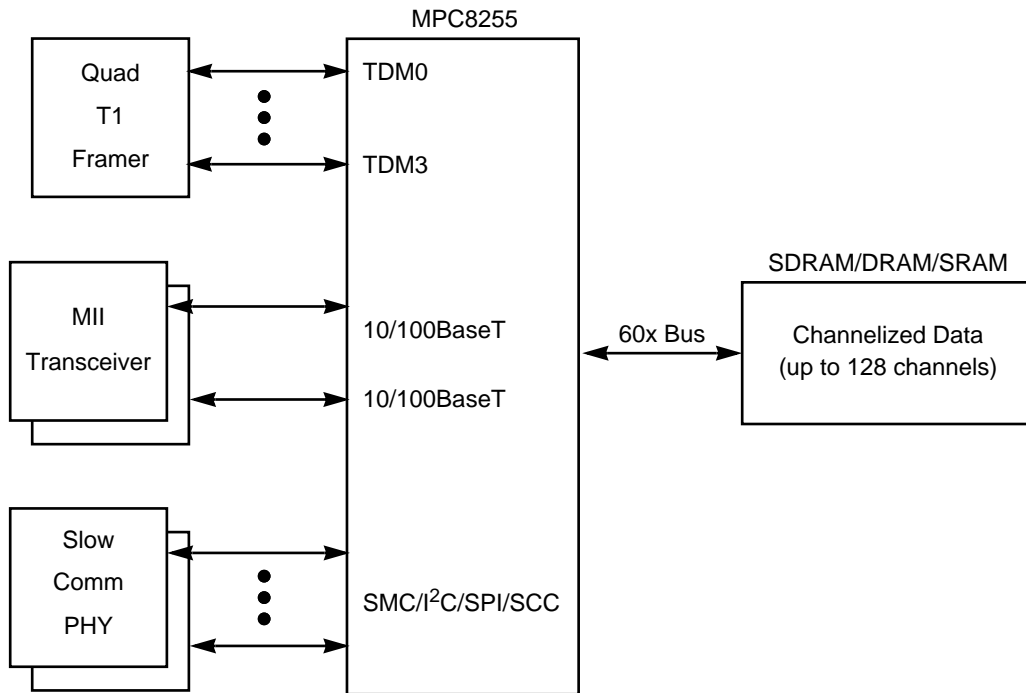


**Figure 3. Regional Office Router Configuration**

In this application, the MPC8255 is connected to four TDM interfaces with up to 128 channels. Each TDM port supports 32–128 channels. If 128 channels are needed, each TDM port can be configured to support 32 channels. In this application there are two MII ports for 10/100BaseT LAN connections.

In all the examples, the SCC ports can be used for management.

## 1.4.1.3   LAN-to-WAN Bridge Router

Figure 4 shows a LAN-to-WAN router configuration, which is similar to the previous example.
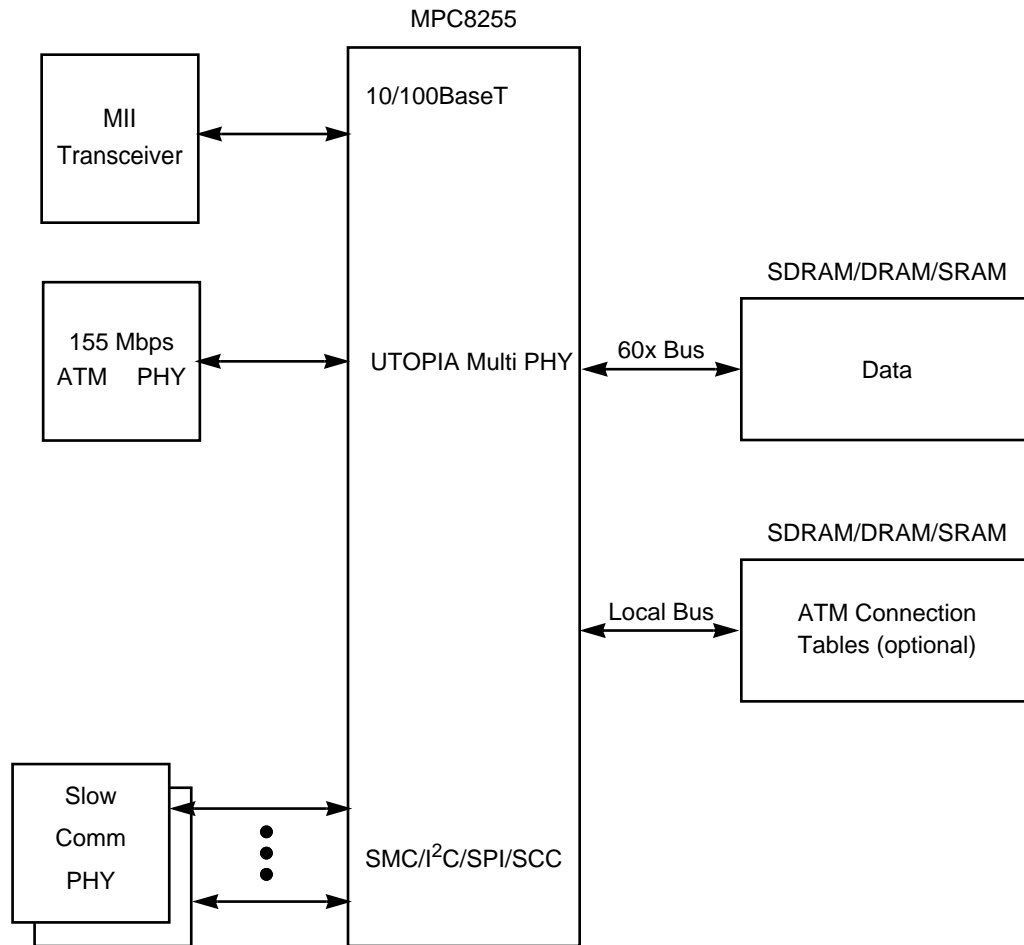
**Figure 4. LAN-to-WAN Bridge Router Configuration**

## 1.4.1.4   Cellular Base Station

Figure 5 shows a cellular base station configuration.
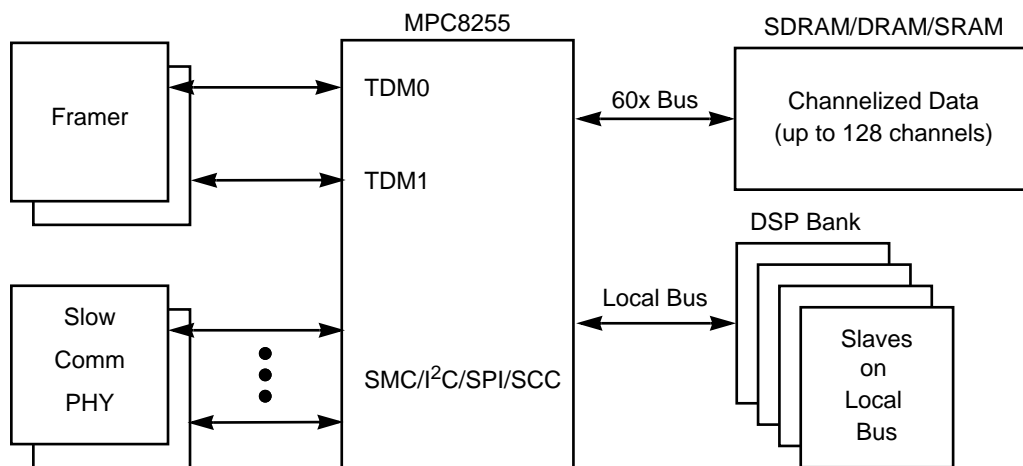


**Figure 5. Cellular Base Station Configuration**

---

Here the MPC8255 channelizes one E1 (up to 128, 16-Kbps channels). The local bus can control a bank of DSPs. Data to and from the DSPs can be transferred through the parallel bus to the host port of the DSPs with the internal virtual IDMA.The slow communications ports (SCCs, SMCs, $I^2C$, SPI) can be used for management and debug functions.

## 1.4.1.5 Telecommunications Switch Controller

Figure 6 shows a telecommunications switch controller configuration.
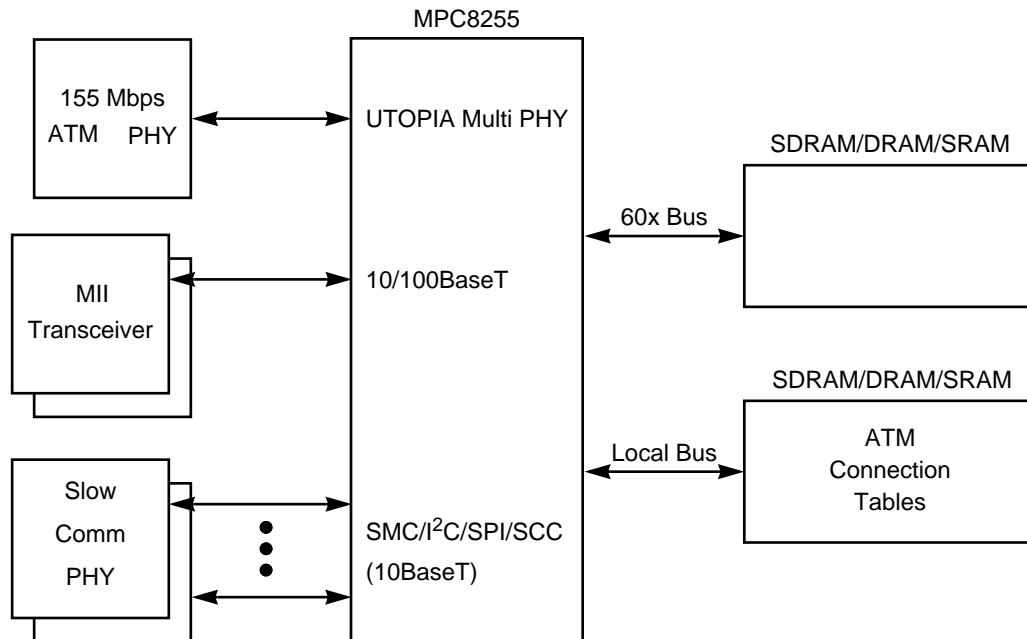


**Figure 6. Telecommunications Switch Controller Configuration**

The MPC8255 CPM supports a total aggregate throughput of 510 Mbps at 100 MHz. This includes one full-duplex 100BaseT and one full-duplex 155 Mbps for ATM. The G2 core can operate at a higher speed, if the application requires it.

## 1.4.1.6 SONET Transmission Controller

Figure 7 shows a SONET transmission controller configuration.
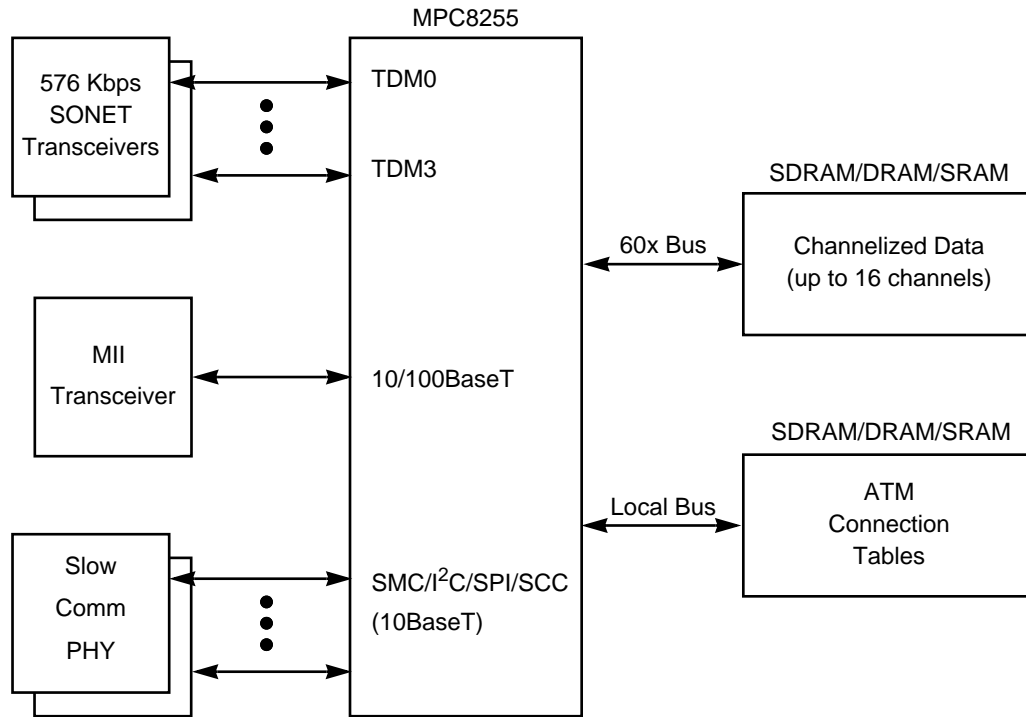
MPC8255



**Figure 7. SONET Transmission Controller Configuration**

In this application, the MPC8255 implements super channeling with the multichannel controller (MCC). Nine 64-Kbps channels are aggregated to form a 576-Kbps channel. The MPC8255 also supports subchanneling (under 64 Kbps) with its MCC.

# 1.4.2   Bus Configurations

There are three possible bus configurations:

- Basic system
- High-performance communications
- High-performance system core

## 1.4.2.1   Basic System

In the basic system configuration, shown in Figure 8, the MPC8255 core is enabled and uses the 64-bit 60x data bus. The 32-bit local bus data is needed to store connection tables for many active ATM connections. The local bus may also be used to store data that does not need to be heavily processed by the core. The CP can store large data frames in the local memory without interfering with the operation of the system core.
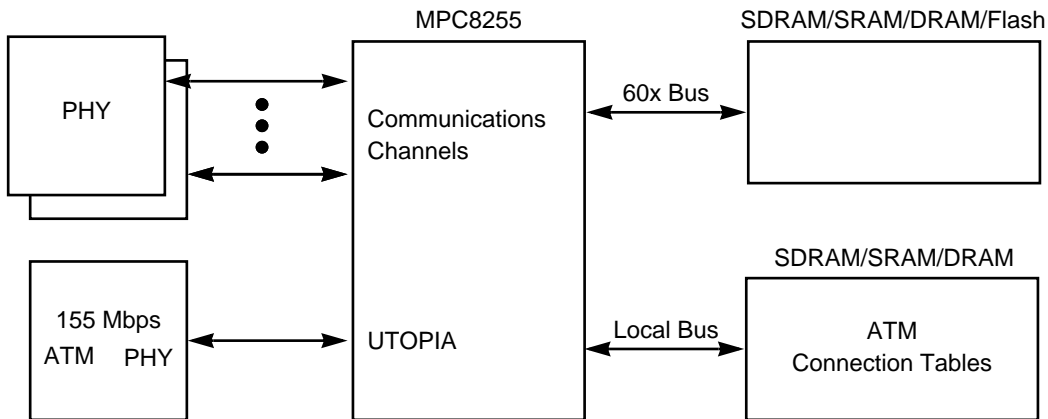
**Figure 8. Basic System Configuration**

## 1.4.2.2 High-Performance Communications

Figure 9 shows a high-performance communications configuration.
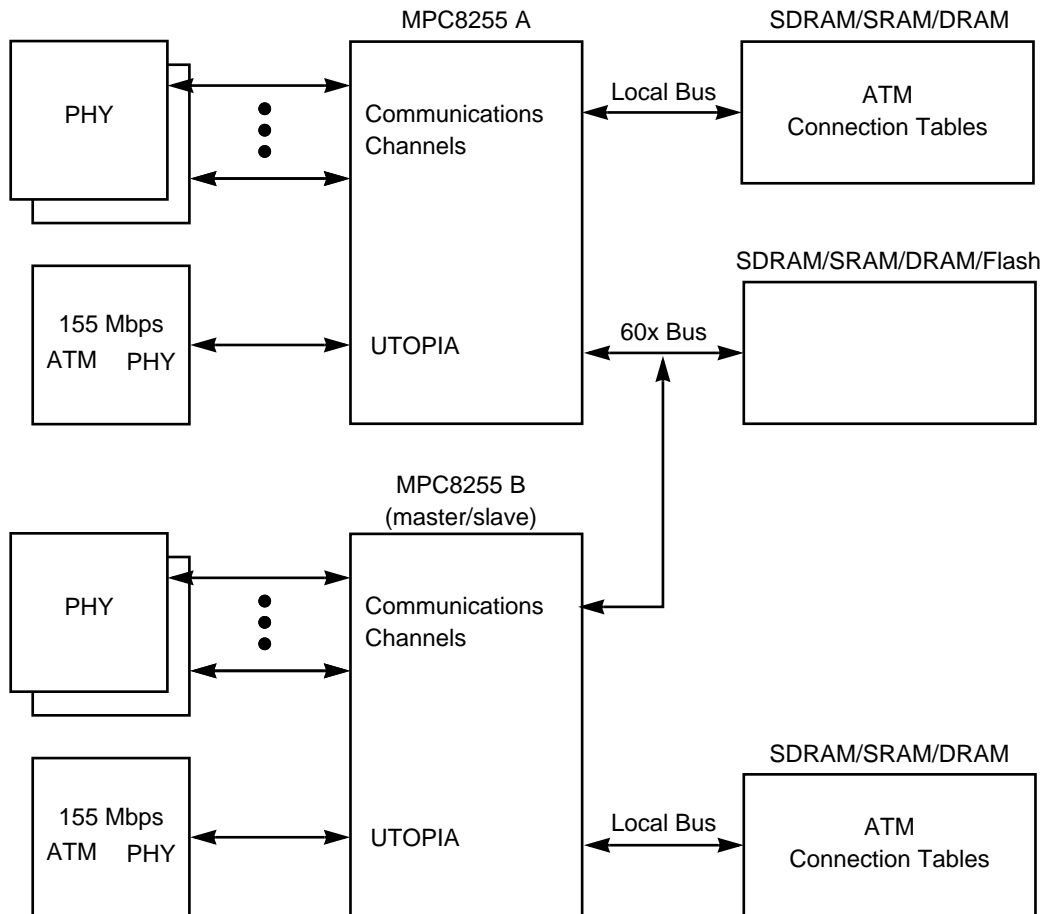


**Figure 9. High-Performance Communications**

This system enhances the serial throughput by connecting one MPC8255 in master or slave mode (with system core enabled or disabled) to another MPC8255 in master mode (core enabled).

The core in MPC8255 A can access the memory on the local bus of MPC8255 B.

## 1.4.2.3  High-Performance System Microprocessor

Figure 10 shows a configuration with a high-performance system microprocessor (MPC755).
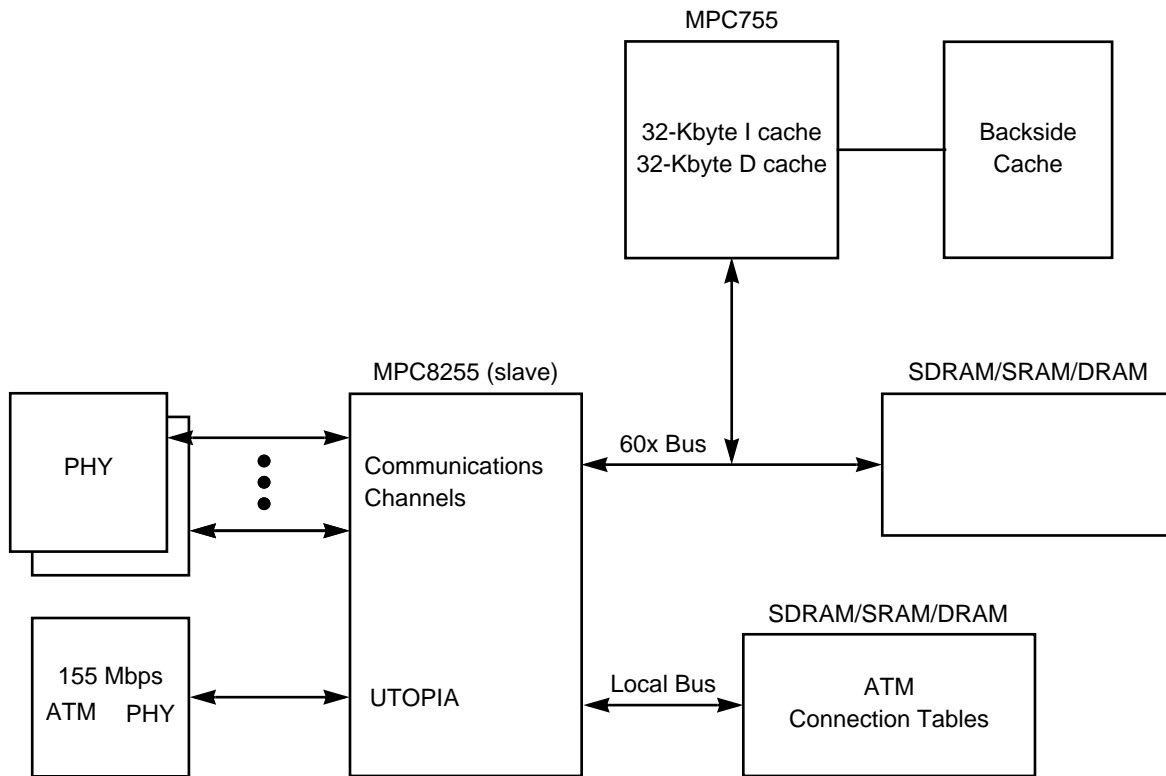


**Figure 10. High-Performance System Microprocessor Configuration**

In this system, the MPC603e core is disabled and an external high-performance microprocessor is connected to the 60x bus.

**Table 1. Document Revision History**

| Revision Number (Rev.) | Changes |
|:---:|:---|
| 0 | — |
| 2.2 | Edited some corrections to manual. |

# Freescale Semiconductor, Inc.

MPC8255TS/D