Freescale Semiconductor
Product Brief

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MPC5645S Microcontroller Product Brief

32-bit MCU for instrument cluster applications

1 Introduction

The MPC5645S represents a new generation of 32-bit microcontrollers targeting single-chip automotive instrument cluster applications. MPC5645S devices are part of the MPC56xxS family of Power Architecture®-based devices. This family has been designed with an emphasis on providing cost-effective and high quality graphics capabilities in order to satisfy the increasing market demand for color Thin Film Transistor (TFT) displays within the vehicle cockpit. Traditional cluster functions, such as gauge drive, real time counter, and sound generation are also integrated on each device.

MPC56xxS devices contain from 256 KB to 2 MB internal flash memory. The MPC56xxS family allows for easy expansion and covers a broad range of cluster applications from low to high-end enabling users to design a complete platform around one common architecture. Serial flash memory and DRAM interfaces are provided to allow even greater system flexibility.

Contents

The MPC5645S:

- Includes 2 MB internal flash memory, 1 MB internal graphics SRAM and 64 KB system SRAM
- Offers high processing performance operating at speeds up to 125 MHz
- Is optimized for low power consumption

The MPC5645S is designed to reduce development and production costs of TFT-based instrument cluster displays by providing a single-chip solution with the processing and storage capacity to host and execute real-time application software and drive TFT displays directly.

The MPC5645S features a 2D OpenVG 1.1 graphics accelerator, Video Input Unit (VIU2) and two on-chip display control units (DCU3 and DCULite) designed to drive two color TFT displays simultaneously. The MPC5645S includes a enhanced QuadSPI Serial Flash Controller and an optional DRAM controller allowing graphics RAM expansion externally.

The MPC5645S is compatible with the existing development infrastructure of current Power Architecture devices and are supported with software drivers, operating systems and configuration code to assist with application development. See Section 4, “Developer support,” for more information.

2 Features

2.1 Device comparison

Table 1. MPC5645S device comparison

Feature	MPC5645S		
Package	176 LQFP	208 LQFP	416 TEPBGA
CPU	e200z4d 4 KB Instruction-Cache 16-entry Memory Management Unit (MMU) Floating Point Unit (FPU) Signal Processing Extension (SPE)		
Execution speed	Static–125 MHz		
Flash memory (ECC)	2 MB		
RAM (ECC)	64 KB		
On-chip graphics RAM (no ECC)	1 MB		
MPU	16 entry		
eDMA	16 channels		
DRAM controller	No		Yes
OpenVG Graphics Accelerator (GFX2D)	Yes (OpenVG 1.1)		
Display Control Unit (DCU3)	Yes		
Display Control Unit Lite (DCULite)	No	Yes	

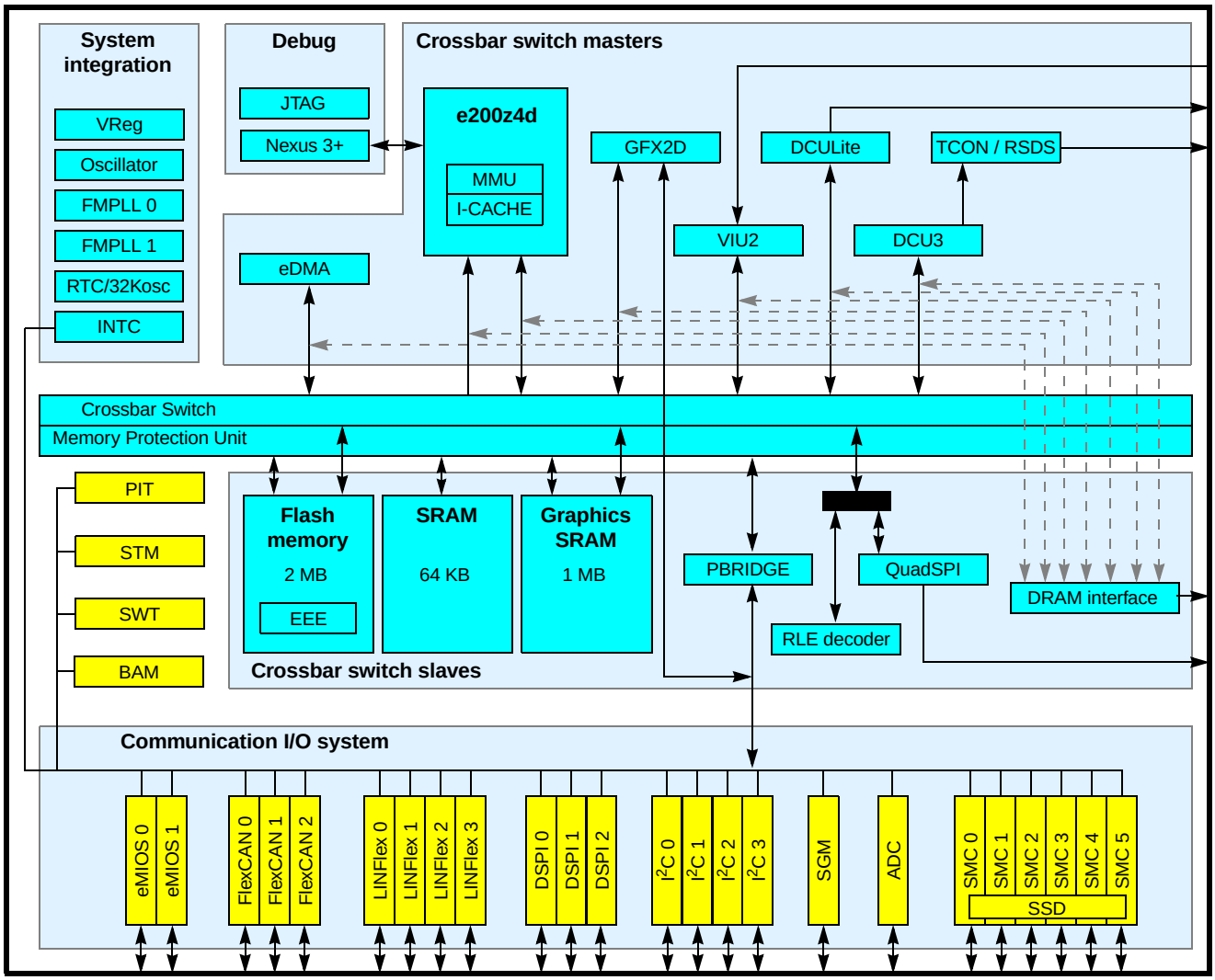
Table 1. MPC5645S device comparison (continued)

Feature	MPC5645S		
Package	176 LQFP	208 LQFP	416 TEPBGA
Timing Controller (TCON) and RSDS interface	No	Yes	
Video Input Unit (VIU2)	Yes		
QuadSPI serial flash interface	Yes		
Stepper Motor Controller (SMC)	4 motors	6 motors	
Stepper Stall Detect (SSD)	Yes		
Sound Generator Module (SGM)	Yes		
32 kHz external crystal oscillator	Yes		
Real Time Counter and Autonomous Periodic Interrupt (RTC/API)	Yes		
Periodic interrupt timer (PIT)	8 ch, 32-bit		
Software Watchdog Timer (SWT)	Yes		
System Timer Module (STM)	4 ch, 32-bit		
Timed I/O[1]	20 ch, 16-bit: IC / OC / OPWM 8 ch, 16-bit: IC / OC 4 ch, 16-bit: IC / OC / OPWM / QDEC		
Analog-to-Digital Converter (ADC)[2]	16 channels, 10-bit	20 channels, 10-bit	
CAN (64 mailboxes)	3 × FlexCAN		
CAN sampler	Yes		
Serial communication interface	3 × LINFlex	4 × LINFlex	
SPI	2 × DSPI	3 × DSPI	
I^2C	4		
GPIO	128	150	177[3]
Debug	Nexus Class 3 (4×MDO)[4]		Nexus Class 3 (12×MDO)

NOTES:
1 IC-Input Capture, OC-Output Compare, OPWM-Output Pulse Width Modulation, QDEC- Quadrature Decode Mode
2 Support for external multiplexer enabling up to 8 channels
3 The 416-pin GPIO count does not include the DRAM interface, which is dedicated to DRAM only.
4 Nexus pins are multiplexed with other functional pins on 176 LQFP and 208 LQFP package options.

2.2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5645S microcontroller.



ADC – Analog-to-Digital Converter
BAM – Boot Assist Module
eDMA – Enhanced Direct Memory Access Controller
DCU3 – Display Control Unit
DCULite – Display Control Unit Lite
DSPI – Serial Peripherals Interface
eMIOS – Enhanced Modular Input/Output System
FlexCAN – Controller Area Network Controller
FMPLL – Frequency-Modulated Phase-Locked Loop
GFX2D – OpenVG Graphics Accelerator
INTC – Interrupt Controller
JTAG – Joint Test Action Group interface
MMU – Memory Management Unit
QuadSPI – Quad IO serial flash interface
PBRIDGE – Peripheral Bridge
PIT – Periodic Interrupt Timer
RLE – Run Length Encoding
RSDS – Reduced-Swing Differential Signal interface
RTC – Real Time Clock
SGM – Sound Generator Module
SMC – Stepper Motor Controller
SSD – Stepper Stall Detect
STM – System Timer Module
SWT – Software Watchdog Timer
TCON – Timing Controller
VIU2 – Video Input Unit
VReg – Voltage regulator

Figure 1. MPC5645S block diagram

2.3 Feature list

- Dual-issue, 32-bit Power Architecture Book E compliant CPU core complex (e200z4d)
  - Memory Management Unit (MMU)
  - 4 KB, 2/4-way instruction cache
- 2 MB on-chip ECC flash memory with:
  - Flash memory controller
  - Prefetch buffers
- 64 KB on-chip ECC SRAM
- 1 MB on-chip non-ECC graphics SRAM with two-port graphics SRAM controller
- Memory Protection Unit (MPU) with up to 16 region descriptors and 32-byte region granularity to provide basic memory access permission and ensure separation between different codes and data
- Interrupt Controller (INTC) with 181 peripheral interrupt sources and eight software interrupts
- Two Frequency-Modulated Phase-Locked Loops (FMPLLs)
  - Primary FMPLL (FMPLL0) provides a system clock up to 125 MHz
  - Auxiliary FMPLL (FMPLL1) is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules, QuadSPI and as alternate clock to the DCU and DCU-Lite for pixel clock generation
- Crossbar switch architecture enables concurrent access of peripherals, flash memory or RAM from multiple bus masters
- 16-channel Enhanced Direct Memory Access controller (eDMA) with multiple transfer request sources using a DMA channel multiplexer
- Boot Assist Module (BAM) with 8 KB dedicated ROM for embedded boot code supports boot options including download of boot code via a serial link (CAN or SCI)
- Two Display Control Units (DCU3 and DCULite) for direct drive of up to two TFT LCD displays up to XGA resolution
- Timing Controller (TCON) and RSDS interface for the DCU3 module
- 2D OpenVG 1.1 and raster graphics accelerator (GFX2D)
- Video Input Unit (VIU2) supporting 8/10-bit ITU656 video input, YUV to RGB conversion, video down-scaling, de-interlacing, contrast adjustment and brightness adjustment.
- DRAM controller supporting DDR1, DDR2, LPDDR1 and SDR DRAMs
- Stepper Motor Controller (SMC)
  - High-current drivers for up to six instrument cluster gauges driven in full dual H-bridge configuration
  - Stepper motor return-to-zero and stall detection module
  - Stepper motor short circuit detection
- Sound Generator Module (SGM)
  - 4-channel mixer
  - Supports PCM wave playback and synthesized tones
  - Optional PWM or I^2S outputs

- Two 16-channel Enhanced Modular Input Output System (eMIOS) modules
  - Support a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation and Quadrature Decode functions
- 10-bit Analog-to-Digital Converter (ADC) with a maximum conversion time of 1 µs
  - Up to 20 internal channels
  - Up to 8 external channels
- Three Deserial Serial Peripheral Interface (DSPI) modules for full-duplex, synchronous, communications with external devices
- QuadSPI serial flash memory controller
  - Supports single, dual and quad IO serial flash memory
  - Interfaces to external, memory-mapped serial flash memories
  - Supports simultaneous addressing of 2 external serial flashes to achieve up 80 MB/s read bandwidth
- RLE decoder supporting memory to memory decoding of RLE data in conjunction with eDMA
- Four local interconnect network (LINFlex) controller modules
  - Capable of autonomous message handling (master), autonomous header handling (slave mode), and UART support
  - Compliant with LIN protocol rev 2.1
- Three controller-area network (FlexCAN) modules
  - Compliant with the CAN protocol version 2.0 C
  - 64 configurable buffers
  - Programmable bit rate of up to 1 Mb/s
- Four Inter-Integrated Circuit (I^2C) internal bus controllers with master/slave bus interface
- Low-power loop controlled pierce crystal oscillator supporting 4–16MHz external crystal or resonator
- Real Time Counter (RTC) with clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wake-up with 1 ms resolution with maximum timeout of 2 seconds
  - Support for real time counter (RTC) with clock source from external 32 KHz crystal oscillator, supporting wake-up with 1 s resolution and maximum timeout of one hour
  - RTC optionally clocked by fast 4–16 MHz external oscillator
- System timers:
  - Four-channel 32-bit System Timer Module (STM)
  - Eight-channel 32-bit Periodic Interrupt Timer (PIT) module (including ADC trigger)
  - Software Watchdog Timer (SWT)
- System Integration Unit Lite (SIUL) module to manage external interrupts, GPIO and pad control
- System Status and Configuration Module (SSCM)
  - Provides information for identification of the device, last boot mode, or debug status
  - Provides an entry point for the censorship password mechanism

- Clock Generation Module (MC_CGM) to generate system clock sources and provide a unified register interface, enabling access to all clock sources
- Clock Monitor Unit (CMU)
  - Monitors the integrity of the fast (4–16 MHz) external crystal oscillator and the primary FMPLL (FMPLL0)
  - Acts as a frequency meter, measuring the frequency of one clock source and comparing it to a reference clock
- Mode Entry Module (MC_ME)
  - Controls the device power mode, i.e., RUN, HALT, STOP, or STANDBY
  - Controls mode transition sequences
  - Manages the power control, voltage regulator, clock generation and clock management modules
- Power Control Unit (MC_PCU) to implement standby mode entry/exit and control connections to power domains
- Reset Generation Module (MC_RGM) to manage reset assertion and release to the device at initial power-up
- Nexus Development Interface (NDI) per IEEE-ISTO 5001-2008 Class 3 standard with additional Class 4 features:
  - Watchpoint Triggering
  - Processor Overrun Control
- Device/board boundary-scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating the 3.3–5 V supply voltage down to 1.2 V for core logic (requires external ballast transistor)
- Package:[1]
  - 176 LQFP, 0.5 mm pitch, 24 mm × 24 mm outline
  - 208 LQFP, 0.5 mm pitch, 28 mm × 28 mm outline
  - 416 TEPBGA, 1mm ball pitch, 27 mm × 27 mm outline

2.4 Feature details

2.4.1 Low-power operation

The MPC5645S is designed for optimized low-power operation and dynamic power management of the CPU and peripherals. Power management features include software-controlled clock gating of peripherals and multiple power domains to minimize leakage in low-power modes.

There are three low-power modes:

1. See the device comparison table for package offerings for each device in the family.

- STANDBY
- STOP
- HALT

and five dynamic power modes — RUN[0..3] and DRUN. All low-power modes use clock gating to halt the clock for all or part of the device.

STANDBY mode turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be awakened from STANDBY mode via from any of up to 23 I/O pins, a reset or from a periodic wake-up using a low power oscillator. If required, it is possible to enable the internal 16 MHz oscillator, the external 4–16 MHz oscillator, and the external 32 KHz oscillator.

In STANDBY mode the contents of the CPU, on-chip peripheral registers, and potentially some of the volatile memory are lost. The two possible configurations in STANDBY mode are:

- The device retains 64 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.
- The device retains 8 KB of the on-chip SRAM, but the content of the graphics SRAM is lost.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest-power STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the CPU and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wake-up from STOP mode is triggered by an external event or by the internal periodic wake-up, if enabled.

RUN modes are the main operating modes where the entire device can be powered and clocked and from which most processing activity is done. Four dynamic RUN modes are supported—RUN0 - RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed, and system clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the CPU system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

Table 2 summarizes the operating modes of the MPC5645S.

Table 2. Operating mode summary

Operating mode	SoC features					Clock sources						Periodic Wake-up	Wake-up input	VREG mode	Wake-up time[1]						
	CPU GFX accelerator DRAM controller	Peripherals	Flash	SRAM	Graphics RAM	Primary PLL	Auxiliary PLL	16MHz IRC	4-16MHz OSC	128KHz IRC	32KHz X OSC				VREG start-up	IRC Wake-up	Flash Recovery	OSC Stabilization	PLL Lock	S/W Reconfig	Mode switch over
RUN	On	OP	OP	OP[2]	On	OP	OP	On	OP	On	OP	—	—	FP	—	—	—	—	—	—	—
HALT	CG	OP	OP	OP[2]	On	OP	OP	On	OP	On	OP	OP	OP	FP	—	—	—	—	—	—	TBD
STOP	CG	CG	CG	OP[2]	CG	CG	CG	OP	OP	On	OP	OP	OP	LP	350 µs	4 µs	20 µs	1 ms	200 µs	—	24 µs
STANDBY	Off	Off	Off	64K[3]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	350 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
	Off	Off	Off	8K[4]	Off	Off	Off	OP	OP	On	OP	OP	OP	LP	200 µs	8 µs	100 µs	1 ms	200 µs	Var	28 µs
POR															500 µs	8 µs	100 µs	1 ms	200 µs		BAM[5]

Table key:
- On — Powered and clocked
- OP — Optionally configurable to be enabled or disabled (clock gated)
- CG — Clock Gated, Powered but clock stopped
- Off — Powered off and clock gated
- FP — VREG Full Performance mode
- LP — VREG Low Power mode, reduced output capability of VREG but lower power consumption
- Var — Variable duration, based on the required reconfiguration and execution clock speed
- BAM — Boot Assist Module Software and Hardware used for device start-up and configuration

NOTES:
1. A high level summary of some key durations that need to be considered when recovering from low power modes. This does not account for all durations at wake up. Other delays will be necessary to consider including, but not limited to the external supply start-up time.
   IRC Wake-up time must not be added to the overall wake-up time as it starts in parallel with the VREG.
   All other wake-up times must be added to determine the total start-up time.
2. Either 64 KB or 8 KB available.
3. 64 KB of the RAM contents is retained, but not accessible in STANDBY mode.
4. 8 KB of the RAM contents is retained, but not accessible in STANDBY mode.
5. Dependent on boot option after reset.

Additional notes on low power operation:

- Fast wake-up using the on-chip 16 MHz internal RC oscillator allows rapid execution from RAM on exit from low power modes
- The 16 MHz internal RC oscillator supports low speed code execution and clocking of peripherals when it is selected as the system clock and can also be used as the PLL input clock source to provide fast start-up without the external oscillator delay
- The device includes an internal voltage regulator that includes the following features:
  - Regulates input to generate all internal supplies
  - Manages power gating

- External ballast transistor for high power regulator
- Low-Power and Ultra-Low-Power regulators support operation when in STOP and STANDBY modes, respectively, to minimize power consumption
- Startup on-chip regulators in <350µs for rapid exit of STOP and STANDBY modes
- Low voltage detection on main supply and 1.2 V regulated supplies

2.4.2 e200z4d core

The e200z4d Power Architecture® core provides the following features:

- Dual issue, 32-bit *Power Architecture Book E* compliant CPU
- Implements the VLE APU for reduced code footprint
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
  - Dedicated branch address calculation adder
  - Branch target prefetching using 8-entry BTB
- Supports independent instruction and data accesses to different memory subsystems, such as SRAM and Flash memory via independent Instruction and Data BIUs.
- Load/store unit
  - 2 cycle load latency
  - Fully pipelined
  - Big and Little endian support
  - Misaligned access support
- 64-bit General Purpose Register file
- Dual AHB 2.v6 64-bit System buses
- Memory Management Unit (MMU) with 16-entry fully-associative TLB and multiple page size support
- 4 KB, 2/4-Way Set Associative Instruction Cache
- Signal Processing Extension (SPE1.1) APU supporting SIMD fixed-point operations using the 64-bit General Purpose Register file
- Embedded Floating-Point (EFP2) APU supporting scalar and vector SIMD single-precision floating-point operations, using the 64-bit General Purpose Register file
- Nexus Class 3 real-time Development Unit
- Dynamic power management of execution units, cache and MMU

2.4.3 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between seven master ports and eight slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows concurrent transactions to occur from any master port to any slave port but one of those transfers must be an instruction fetch from internal flash. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters having equal priority are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- Seven master ports:
  - e200z4d core instruction port
  - e200z4d core complex load/store data port
  - eDMA controller
  - DCU
  - DCULite
  - VIU
  - 2D Graphics Accelerator (GFX2D)
- Seven slave ports:
  - Platform Flash Controller (2 Ports)
  - Platform SRAM Controller
  - Graphics SRAM Controller (2 Ports)
  - QuadSPI serial flash Controller and RLE Decoder
  - Peripheral Bridge
- 32-bit internal address bus, 64-bit internal data bus
- Programmable Arbitration Priority
  - Requesting masters can be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access, or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

2.4.4 Enhanced Direct Memory Access (eDMA)

The eDMA module is a controller capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- 16 channels support independent 8-, 16-, or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant

- Each transfer is initiated by a peripheral, CPU, periodic timer interrupt or eDMA channel request
- Each DMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, QuadSPI, RLE Decoder, DSPIs, I^2C, ADC, eMIOS, and General Purpose I/Os (GPIOs)
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with up to a total of 64 potential request sources

2.4.5 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS. The INTC provides the following features:

- Unique 9-bit vector for each of the possible 128 separate interrupt sources
- Eight software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
  - Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
- External non maskable interrupt directly accessing the main CPU critical interrupt mechanism
- 32 external interrupts

2.4.6 QuadSPI serial flash memory controller

The QuadSPI module enables use of external serial flash memories supporting single, dual, and quad modes of operation. It features the following:

- Maximum serial clock frequency 80 MHz

- Memory mapped read access for AHB crossbar switch masters
- Automatic serial flash read command generation by CPU, eDMA, DCU, or DCULite read access on AHB bus
- Supports single, dual, and quad serial flash read commands
- Simultaneous mode:
  - Supports concurrent read of two external serial flashes
  - The quad data streams from the two flashes can be recombined in the QuadSPI to achieve up to 80 MB/s read bandwidth with 80 MHz serial flash
- 16×64-bit buffer with speculative fetch and buffer flush mechanisms to maximize read bandwidth of serial flash
- DMA support
- All Serial Flash program, erase, read, and configuration commands available via IP bus interface

2.4.7 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.

The GPIO features the following:

- Up to four levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs
- Direct readback of the pin value supported on all digital output pins through the SIU
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts
- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset

2.4.8 On-chip flash memory with ECC

The MPC5645S microcontroller has the following flash memory features:

- 2 MB of flash memory
  - Typical flash memory access time: 0 wait-state for buffer hits, 3 wait-states for page buffer miss at 125 MHz
  - Two 4×128-bit page buffers with programmable prefetch control
    - One set of page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access

  - One set of page buffers allocated to Display Controller Units, Graphics Accelerator, and the eDMA
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Small block flash arrangement to support features such as boot block, EEPROM Emulation, operating system block
  - 8×16 KB
  - 2×64 KB
  - 2×128 KB
  - 6×256 KB
- Hardware managed flash writes, erase and verify sequence
- Censorship protection scheme to prevent Flash content visibility

2.4.9 SRAM

The MPC5645S microcontroller has 64 KB general-purpose on-chip SRAM with the following features:

- Typical SRAM access time: 1 wait-state for reads and 32-bit writes
- 32-bit ECC with single-bit correction, double bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), word (32-bit), and double-word (64-bit) writes for optimal use of memory
- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domains applied to 56 KB and 8 KB SRAM blocks during STANDBY modes to retain contents during low power mode

2.4.10 On-chip graphics SRAM

The MPC5645S microcontroller has 1 MB on-chip graphics SRAM with the following features:

- Two crossbar slave ports:
  - One dedicated to the 2D Graphics Accelerator (GFX2D) access
  - One dedicated to all other crossbar masters
- Usable as general purpose SRAM
- Supports byte (8-bit), half word (16-bit), word (32-bit), and double-word (64-bit) writes for optimal use of memory
- RAM controller with hardware RAM fill function supporting all-zeroes or all-ones SRAM initialization
- Independent data buffers (one per AHB port) for maximum system performance
  - Optimized for burst transfers (read + write)
  - Programmable read prefetch capabilities

2.4.11 Memory Protection Unit (MPU)

The MPU features the following:

- Sixteen region descriptors for per master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 4 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

2.4.12 2D Graphics Accelerator (GFX2D)

- Native vector graphics rendering
  - Compatible with OpenVG1.1
  - Complete hardware OpenVG 1.1 rendering pipeline
  - Both geometry and pixel processing
  - Adaptive processing of Bezier curves and strokes
- 16-sample edge anti-aliasing
  - High image quality, font scalability, etc.
  - 4× Rotated Grid Supersampling (RGSS) AA for Flash
- 3D perspective texturing, reflections, and shadowing
- Shading (linear or radial gradient)
- Separate 2D engine for BitBlt, fill, and ROP operations
- Significant performance improvement when compared to software or 3D GPU-based OpenVG implementations

2.4.13 Display Control Unit (DCU3)

The DCU3 is a display controller designed to drive TFT LCD displays up to WVGA resolution using direct blit graphics and video.

The DCU3 generates all the necessary signals required to drive the TFT LCD displays: up to 24-bit RGB data bus, Pixel Clock, Data Enable, Horizontal-Sync, and Vertical-Sync.

The flexible architecture of the DCU3 enables the display of OpenVG-rendered frame buffer content and direct blit rendered graphics simultaneously.

An optional Timing Controller (TCON) and RSDS interface is available to directly drive the row and column drivers of a display panel.

Internal memory resource of the device allows to easily handle complex graphics contents (pictures, icons, languages, fonts).

The DCU3 supports 4-plane blending and 16 graphics layers. Control Descriptors (CDs) associated with each of the 16 layers enable effective merging of different resolutions into one plane to optimize use of internal memory buffers. A layer may be constructed from graphic content of various resolutions including indexed colors of 1, 2, 4, and 8 bpp, direct colors of 16, 24, and 32 bpp, and a YUV 4:2:2 color space. The ability of the DCU3 to handle input data in resolutions as low as 1bpp, 2bpp, and 4bpp enables a highly efficient use of internal memory resources of the MPC5645S. A special tiled mode can be enabled on any of the 16 layers to repeat a pattern optimizing graphic memory usage.

A hardware cursor can be managed independently of the layers at blending level increasing the efficient use of the internal DCU3 resources.

To secure the content of all critical information to be displayed, a safety mode can be activated to check the integrity of critical data along the whole system data path from the memory to the TFT pads.

The DCU3 features the following:

- Display color depth: up to 24 bpp
- Generation of all RGB and control signals for TFT
- Four-plane blending
- Maximum number of Input Layers: 16 (fixed priority)
- Dynamic Look-Up-Table (Color and Gamma Look-Up)
- α–blending range: up to 256 levels
- Transparency Mode
- Gamma Correction
- Tiled mode on all the layers
- Hardware Cursor
- Supports YCrCb 4:2:2 input data format
- RLE decode inline supporting direct read of RLE compressed images from system memory
- Critical display content integrity monitoring for Functional Safety support
- Internal Direct Memory Access (DMA) module to transfer data from internal and / or external memory

The DCU3 also features a Parallel Data Interface (PDI) to receive external digital video or graphic content into the DCU3. The PDI input is directly injected into the DCU3 background plane FIFO. When the PDI is activated, all the DCU3 synchronization is extracted from the external video stream to guarantee the synchronization of the two video sources.

The PDI can be used to:

- Connect a video camera output directly to the PDI
- Connect a secondary display driver as slave with a minimum of extra cost
- Connect a device gathering various Video sources
- Provide flexibility to allow the DCU to be used in slave mode (external synchronization)

The PDI features the following:

- Supported color modes:

  - 8-bit mono
  - 8-bit color multiplexed
  - RGB565
  - 16-bit/18-bit RAW color
- Supported synchronization modes:
  - embedded ITU-R BT.656-4 (RGB565 mode 2)
  - HSYNC, VSYNC
  - Data Enable
- Direct interface with DCU3 background plane FIFO
- Synchronization generation for the DCU3

2.4.14 Display Control Unit Lite (DCULite)

The DCULite is a display controller designed to enable the MPC5645S to drive a second TFT LCD display up to XGA resolution using direct blit graphics and video. The DCULite includes all features of the DCU3, including the PDI with the following exceptions:

- Reduced from 4-plane to 2-plane blending
- Reduced from 16 layers to 4 layers
- Reduced CLUT size

2.4.15 Timing Controller (TCON) and RSDS interface

The TCON enables direct drive of the row and column drivers of display panels enabling emulation of TCON ICs used in display panels.

- Programmable Timing Generation unit featuring 12 waveform generators allowing high degree of flexibility in panel waveform generation
- Reduced Swing Differential Signaling (RSDS) interface for RGB data and pixel clock
- Conforms to “RSDS ‘Intra Panel’ Interface Specification” Rev. 1.0 (National Semiconductor)

2.4.16 RLE decoder

The RLE decoder is a crossbar slave sharing a slave port with the QuadSPI module. The platform eDMA is used to stream compressed image data into and extract decompressed data out of the RLE Decoder.

- Lossless decompression
- Pixel formats supported: 8 bpp, 16 bpp, 24 bpp, and 32 bpp
- AHB mapped read and write registers in RLE_DEC to achieve higher throughput
- Programmable fill levels of read and write buffers for initiating burst transfers
- Crop feature: Support for selectively reading out a part of decompressed image data taking complete compressed data for the full image as input

2.4.17 DRAM controller

The DRAM controller is a multi-port DRAM controller supporting SDR, LPDDR1, DDR-1, and DDR-2 memories. The DRAM controller listens to the incoming requests to the seven buses in parallel and then sends commands to the DRAM from the highest priority bus at the current time

The seven incoming 64-bit buses are:

- DCU3
- DCULite
- e200z4d core — instruction bus
- e200z4d core — data bus
- VIU2
- GFX2D
- eDMA

The DRAM controller features the following:

- Supports CAS latency of 2, 3, and 4 clock cycles
- Master buses
  - 7 incoming master buses
  - Supports 16-byte and 32-byte bursts
  - Supports byte enables
  - Supports 4-bit priority signal for each bus
- Write buffer contains five 32-byte entries
- Supports 16-wide and 32-wide SDR, DDR1, DDR2, and LPDDR1 DRAM devices
- Controller supports one chip select, 8-bank DRAM system
- Supports dynamic on-die termination in the host device and in the DRAM
- Supports memory sizes as small as 64 Mbit

2.4.18 Video Input Unit (VIU2)

The VIU2 is a crossbar master module accepting an ITU656 compatible video input stream on a parallel interface, converting the pixel data to RGB or YUV format and transferring the video image to internal frame buffer memory or external DRAM if available.

- Supports 8-bit/10-bit ITU656 video input
- Output formats:
  - RGB888
  - RGB565
  - 8-bit monochrome
  - YCrCb 4:2:2
- Video downscaling
- Contrast and Brightness adjustment

- De-interlace for interlaced video image
- Internal DMA engine for data transfer to memory

2.4.19 Boot Assist Module (BAM)

The BAM is a block of read-only memory that is programmed once by Freescale. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via FlexCAN or LINFlex and then executed)
- Booting from external memory

Additionally the BAM:

- Enables and manages the transition of the MCU from reset to user code execution
- Configures device for serial bootload
- Enables multiple bootcode starting locations out of reset through implementation of search for valid Reset Configuration Halfword

2.4.20 Enhanced Modular Input/Output System (eMIOS)

This device has two eMIOS modules, each with 16 channels supporting a range of 16-bit Input Capture, Output Compare, Pulse Width Modulation, and Quadrature Decode functions.

- Selectable clock source from primary FMPLL, secondary FMPLL, external 4 - 16 MHz oscillator or 16 MHz Internal RC oscillator on a per module basis
- Timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Edge aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- Programmable phase shift between channels
- 4 channels of Quadrature Decode
- DMA transfer support

2.4.21 Analog-to-Digital Converter (ADC)

The ADC features the following:

- 10-bit A/D resolution
- 0–5 V or 0–3.3 V common mode conversion range

- Supports conversions speeds of up to 1µs
- 20 internal and 8 external channels support
- Up to 20 single-ended inputs channels
  - 10 channels configured as input only pins
    - 10-bit ± 2 counts accuracy (TUE)
  - 10 channels configured to have alternate function as general purpose input/output pins
    - 10-bit ± 3 counts accuracy (TUE)
- External multiplexer support to increase up to 27 channels
  - Automatic 1 × 8 multiplexer control
  - External multiplexer connected to a dedicated input channel
  - Shared register between the 8 external channels
- Result register available for every non-multiplexed channel
- Configurable Left or Right aligned result format
- Supports for one-shot, scan, and injection conversion modes
- Injection mode status bit implemented on adjacent 16-bit register for each result
  - Supports Access to Result and injection status with single 32-bit read
- Independently enabling of function for channels:
  - Pre-sampling
  - Offset error cancellation
  - Offset Refresh
- Conversion Triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT)
- Four configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range
- All unused analog pins available as general purpose input pins
- Selected unused analog pins available as general purpose pins
- Power Down mode
- Optional support for DMA transfer of results

2.4.22 Deserial Serial Peripheral Interface (DSPI)

The DSPI modules provide a synchronous serial interface for communication between the MCU and external devices.

The DSPI features:

- Full duplex, synchronous transfers
- Master or slave operation

- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 3 chip select lines available, depending on package and pin multiplexing, enable 8 external devices to be selected using external muxing from a single DSPI
- Eight clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA

2.4.23 FlexCAN

The MPC5645S includes up to three controller area network (FlexCAN) modules. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each FlexCAN module offers the following:

- Compliant with CAN protocol specification, Version 2.0B active
- 64 mailboxes, each configurable as transmit or receive
  - Mailboxes configurable while module remains synchronized to CAN bus
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen only mode capabilities
- CAN Sampler

- Can catch the 1st message sent on the CAN network while the MCU is stopped, which guarantees a clean startup of the system without missing messages on the CAN network
- The CAN sampler is connected to one of the CAN RX pins

2.4.24 Serial communication interface module (LINFlex)

The MPC5645S devices include up to four LINFlex modules and support for LIN Master mode, LIN Slave mode, and UART mode. The modules are LIN state machine compliant to the LIN 1.3, 2.0, and 2.1 Specifications and handle LIN frame transmission and reception without CPU intervention.

Other features include:

- Autonomous LIN frame handling
- Message buffer to store identifier and up to eight data bytes
- Supports message length of up to 64 bytes
- Detection and flagging of LIN errors
- Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
- Classic or extended checksum calculation
- Configurable Break duration of up to 36-bit times
- Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
- Diagnostic features
  - Loop back
  - Self Test
  - LIN bus stuck dominant detection
- Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Discarding of irrelevant LIN responses using up to 16 ID filters
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise, and framing errors
  - Interrupt driven operation with 4 interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wakeup methods

2.4.25 Inter-Integrated Circuit (I^2C) controller modules

The MPC5645S includes four I^2C modules. Each module features the following:

- Two-wire bi-directional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multi-master operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

2.4.26 System clocks and clock generation modules

The system clock on the MPC5645S can be derived from an external oscillator, an on-chip FMPLL, or the internal 16 MHz oscillator.

The source system clock frequency can be changed via an on-chip programmable clock divider (÷1 to ÷32). An additional programmable peripheral bus clock divider (ratios ÷1 to ÷15) is also available.

The MPC5645S has two on-chip FMPLLs (primary and secondary). Each features the following:

- Input clock frequency from 4 MHz to 16 MHz
- Lock detect circuitry continuously monitors lock status
- Loss Of Clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and reduction of number of external components required)
- Support for frequency ramping from PLL

The primary FMPLL module is for use as a system clock source. The secondary FMPLL is available for use as an alternate, modulated or non-modulated clock source to eMIOS modules and as alternate clock to the DCU for pixel clock generation.

The fast external oscillator provides the following features:

- Input frequency range 4–16 MHz
- Square-wave input mode
- Oscillator input mode 3.3 V (5.0 V)
- Automatic level control
- Low power consumption

- PLL reference

The MPC5645S also includes the following oscillators:

- 32 KHz low power external oscillator for slow execution, low power, and RTC
- Dedicated internal 128 kHz RC oscillator for low power mode operation and self wake-up
  - ±10% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support improved accuracy with in-application calibration
- Dedicated 16 MHz internal RC oscillator
  - Used as default clock source out of reset
  - Provides a clock for rapid start-up from low power modes
  - Provides a back-up clock in the event of PLL or External Oscillator clock failure
  - Offers an independent clock source for the SWT
  - ±5% accuracy across voltage and temperature (after factory trimming)
  - Trimming registers to support frequency adjustment with in-application calibration

2.4.27 Periodic Interrupt Timer (PIT)

The PIT features the following:

- Eight general purpose interrupt timers
- Two dedicated interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency

2.4.28 Real Time Counter (RTC)

The Real Timer Counter supports wake-up from Low Power modes or Real Time Clock generation

- Configurable resolution for different timeout periods
  - 1 s resolution for >1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources from external 32 KHz crystal, external 4–16 MHz crystal, internal 128 kHz RC oscillator or divided internal 16 MHz RC oscillator

2.4.29 System Timer Module (STM)

The STM is a 32-bit timer designed to support commonly required system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel. The counter is driven by the system clock divided by an 8-bit prescale value (1 to 256).

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel

- Counter can be stopped in debug mode

2.4.30 Software Watchdog Timer (SWT)

The SWT features the following:

- Watchdog supporting software activation or enabled out of Reset
- Supports normal or windowed mode
- Watchdog timer value writable once after reset
- Watchdog supports optional halting during low power modes
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Clock source: 128 kHz RC oscillator

2.4.31 Stepper Motor Controller (SMC)

The SMC module is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has twelve PWM channels associated with two pins each (24 pins in total) driving up to 6 stepper motors.

The SMC module includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Output slew rate control
- Output Short Circuit Detection

This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

2.4.32 Stepper Stall Detect (SSD)

The SSD module provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ).

The SSD module features the following:

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register
- 16-bit modulus down counter with interrupt

2.4.33 Sound Generator Module (SGM)

The SGM features the following:

- 4-channel audio mixer
- Each channel capable of independent Tone generation or Wave playback
- Individual channel volume control (8-bit resolution)
- Tone Mode:
  - Programmable Tone frequency
  - Programmable amplitude envelope: attack, duration, and decay
  - Programmable number of tone pulses and inter-tone duration
- Wave Mode:
  - One FIFO per channel working in conjunction with eDMA
  - Supports standard audio sampling rates (4 kHz, 8 kHz, 11.025 kHz, 16 kHz, 22.050 kHz, 32 kHz, 44.100 kHz, 48 kHz)
  - Same sample rate applies to all channels
  - 8-bit, 12-bit, 16-bit input data formats
  - Programmable wave duration and inter-wave duration
  - Repeat mode with programmable number of wave playbacks
- SGM Output:
  - 16-bit PWM channel
  - Integrated I^2S master interface for connection to external audio DAC

2.4.34 IEEE 1149.1 JTAG controller (JTAGC)

JTAGC features the following:

- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Support for boundary scan testing

2.4.35 Nexus Development Interface (NDI)

The Nexus 3 module is compliant with Class 3 of the IEEE-ISTO 5001-2008 standard, with additional Class 4 features available. The following features are implemented:

- Program Trace via Branch Trace Messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.
- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace

Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.

- Run-time access to embedded processor memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint Messaging via the auxiliary pins provides visibility when debugging.
- Watchpoint Trigger enablement of Program and/or Data Trace Messaging enhances debug capability.
- Data Acquisition Messaging (DQM) allows code to be instrumented to export customized information to the Nexus Auxiliary Output Port.
- Address Translation Messaging via program correlation messages displays updates to the TLB for use by the debugger in correlating virtual and physical address information.
- Auxiliary interface for higher data input/output.
- Registers for Program Trace, Data Trace, Ownership Trace, and Watchpoint Trigger.
- All features are controllable and configurable via the JTAG port.
- Nexus Auxiliary port is supported on the 416BGA package.

3 Application examples

3.1 Instrument cluster with TFT display

Figure 2 outlines an Instrument Cluster application supporting two color TFT display built around the MPC5645S microcontroller. With its dual internal display control units, it is capable of directly driving color TFT displays using internal memory resources only. Increased graphical content can be achieved using external serial flash memory connected to the QuadSPI interface. The graphics capabilities of the MPC5645S can be further extended with external DRAM in the 324-pin package option.

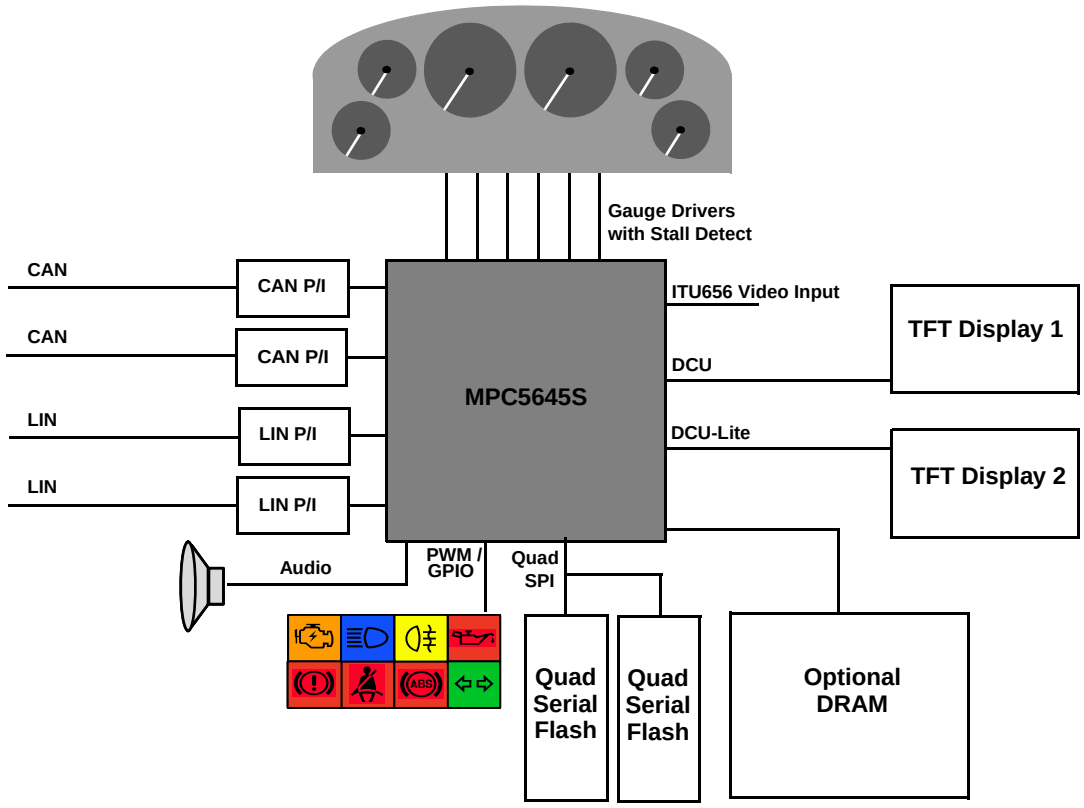


Figure 2. Instrument cluster using the MPC5645S microcontroller

4 Developer support

This family of MCUs is supported by similar tools as other Freescale MPC5500/MPC5600 products offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus debug interface.

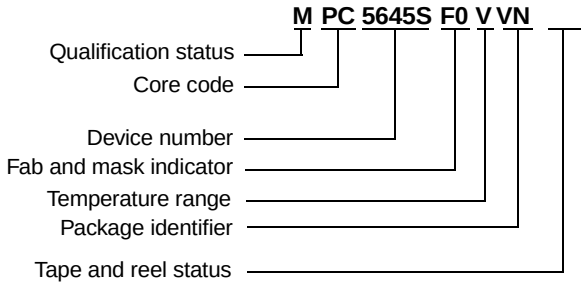
The following development support will be available:

- Automotive Evaluation Boards (EVB) featuring CAN, LIN interfaces and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces

The following software support will be available:

- OSEK solutions will be available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

5 Orderable parts



Temperature range

C = –40 °C to 85 °C
V = –40 °C to 105 °C

Package identifier

LU = 176 LQFP Pb-free
LT = 208 LQFP Pb-free
VU = 416 TEPBGA Pb-free

Tape and reel status

R = Tape and reel
(blank) = Trays

Qualification status

P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices. Refer to Table 3.

Figure 3. Commercial product code structure

Table 3. Orderable part number summary

Part number[1]	Flash/SRAM	Package	Speed (MHz)
PPC5645SF0VLUA	2 MB/64 KB	176 LQFP (Pb free)	125
PPC5645SF0VLTA	2 MB/64 KB	208 LQFP (Pb free)	125
PPC5645SF0VVUA	2 MB/64 KB	416 TEPBGA (Pb free)	125

NOTES:
1 All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete. Not all configurations are available in the PPC parts.

6 Revision history

Table 4. Revision history

Revision (Date)	Description
1 (30 Sep 2009)	Initial release.
2 (26 Feb 2010)	Editorial changes and improvements. Revised some module abbreviations and names to be consistent with the other documents for this device. Deleted the term “z160” from the OpenVG graphics accelerator name. Changed “OpenVG” to “OpenVG 1.1”. In the device-comparison table: • Revised the “Timed I/O” entry. • Changed “Nexus 3” to “Nexus Class 3”. In the block diagram: • Modified the connection between the core, crossbar switch, and DRAM controller. • Changed the port splitter from a blue rectangle to a thick solid line. • Modified the connection between GFX2D and PBRIDGE. In the feature list: • Revised the information for the TCON and RSDS interface. • In the ADC entry, changed “20 internal channels” to “Up to 20 internal channels”. • In the QuadSPI entry, changed “quad modes of operation” to “quad IO serial flash memory”. • In the DCU3 and DCULite entry, changed “WVGA” to “XGA”. In the feature details: • In the QuadSPI section, changed “Maximum frequency 80 MHz” to “Maximum serial clock frequency 80 MHz” • In the FlexCAN section, changed “The FlexCan modules offer” to “Each FlexCAN module offers”. • In the GFX2D section, deleted “and Adobe Flash 7”. • In the DCULite section, changed “WVGA” to “XGA”. Added orderable part numbers. Revised the “Commercial product code structure” figure.

Table 4. Revision history (continued)

Revision (Date)	Description
3 (21 Jun 2010)	Editorial changes and improvements. In the device-comparison table, changed the GPIO count for the 176-pin package (was 127, is 128). In the feature list: • Changed “4 KB, 2-way instruction cache” to “4 KB, 2/4-way instruction cache”. • Changed “32 kHz crystal oscillator” to “32 KHz crystal oscillator”. • Changed “188 peripheral interrupt sources” to “181 peripheral interrupt sources”. • Changed “Primary FMPLL” to “Primary FMPLL (FMPLL0)”. • Changed “Auxiliary FMPLL” to “Auxiliary FMPLL (FMPLL1)”. • In the crossbar switch description, deleted the reference to AMBA. • In the SGM description, changed “WAV file” to “PCM wave”. • Revised the RLE decoder description. • In the SIUL description, deleted “resets”. • In the CMU section, changed “PLL” to “primary FMPLL (FMPLL0)”. In the feature details: • Changed “32 kHz oscillator” to “32 KHz oscillator”. • Changed “128 KHz oscillator” to “128 kHz oscillator”. • Revised the “Low-power operation” section. • Revised the DCU3 section. • In the “On-chip graphics SRAM” section, added an entry for independent data buffers. • In the MPU section, changed “Protection offered for 3 concurrent read ports” to “Protection offered for 4 concurrent read ports”. • In the ADC section, changed “0 to 5V common mode conversion range” to “0–5 V or 0–3.3 V common mode conversion range”.

4
(29 Apr 2011)
	Editorial changes and improvements.
	In the device-comparison table:
	• Changed “324 TEPBGA” to “416 TEPBGA” and updated the footnote.
	In the feature list:
	• Changed 324 TEPBGA package to 416, and dimensions (both) from 23 mm to 27 mm.
	• Changed RTC optional clocking from “main“ to “fast“ 4-16 MHz external oscillator.
	• Changed CMU monitor feature from “main crystal oscillator“ to “fast (4–16 MHz) external crystal oscillator”.
	In the feature details:
	• Changed “DCU-Lite” to “DCULite” throughout the section.
	• Changed “324” BGA to “416” in the “Nexus Development Interface“ section.
	• Changed “main oscillator“ to “external oscillator“ in the “System clocks and clock generation modules“ section.
	• In the “Operating mode summary“ table:
	  • Changed the “RAM” column to “SRAM”.
	  • Changed “STOP” for “16MHz IRC” from “OP” to “On”.
	  • Changed “STOP” for “Graphics RAM” from “On” to “CG”.
	  • Changed “STANDBY” for “128KHz IRC” from “OP” to “ON” (both cases).
	In the “Orderable part number summary“ table:
	• Changed “324” to “416”.
	• Updated the part numbers.

5 (07 Jun 2011)	• Formatting and editorial changes.

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