Freescale Semiconductor
Product Brief

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MCF5271 Integrated Microprocessor Product Brief

by: Microcontroller Division

The MCF5271 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent features and functions of the MCF5271 family. The MCF5271 family includes the MCF5271 and MCF5270 microprocessors. The differences between these parts are summarized below in Table 1. This document is written from the perspective of the MCF5271 and unless otherwise noted, the information applies also to the MCF5270.

The MCF5271 family delivers a new level of performance and integration on the popular version 2 ColdFire core with over 144 (Dhrystone 2.1) MIPS at 150 MHz. Positioned for applications requiring a low cost, strong performance, 32-bit solution, the MCF5271 family features a 10/100 Ethernet MAC and optional hardware encryption to ensure the application can be connected and protected. In addition, the MCF5271 family features an enhanced multiply accumulate unit (eMAC), large on-chip memory (64 Kbytes SRAM, 8 Kbytes configurable cache), and a 32-bit SDR SDRAM memory controller.

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To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

1 MCF5271 Family Configurations

Table 1. MCF5270/71 Family Configurations

Module	5270	5271
ColdFire V2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x
System Clock	up to 150 MHz	
Performance (Dhrystone/2.1 MIPS)	up to 144	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	64 Kbytes	
Interrupt Controllers (INTC)	2	2
Edge Port Module (EPORT)	x	x
External Interface Module (EIM)	x	x
4-channel Direct-Memory Access (DMA)	x	x
SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	x	x
Cryptography Hardware Accelerators	—	x
Watchdog Timer (WDT)	x	x
Four Periodic Interrupt Timers (PIT)	x	x
32-bit DMA Timers	4	4
QSPI	x	x
UART(s)	3	3
I^2C	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x
Package	160 QFP 196 MAPBGA	160 QFP 196 MAPBGA

2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array process ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

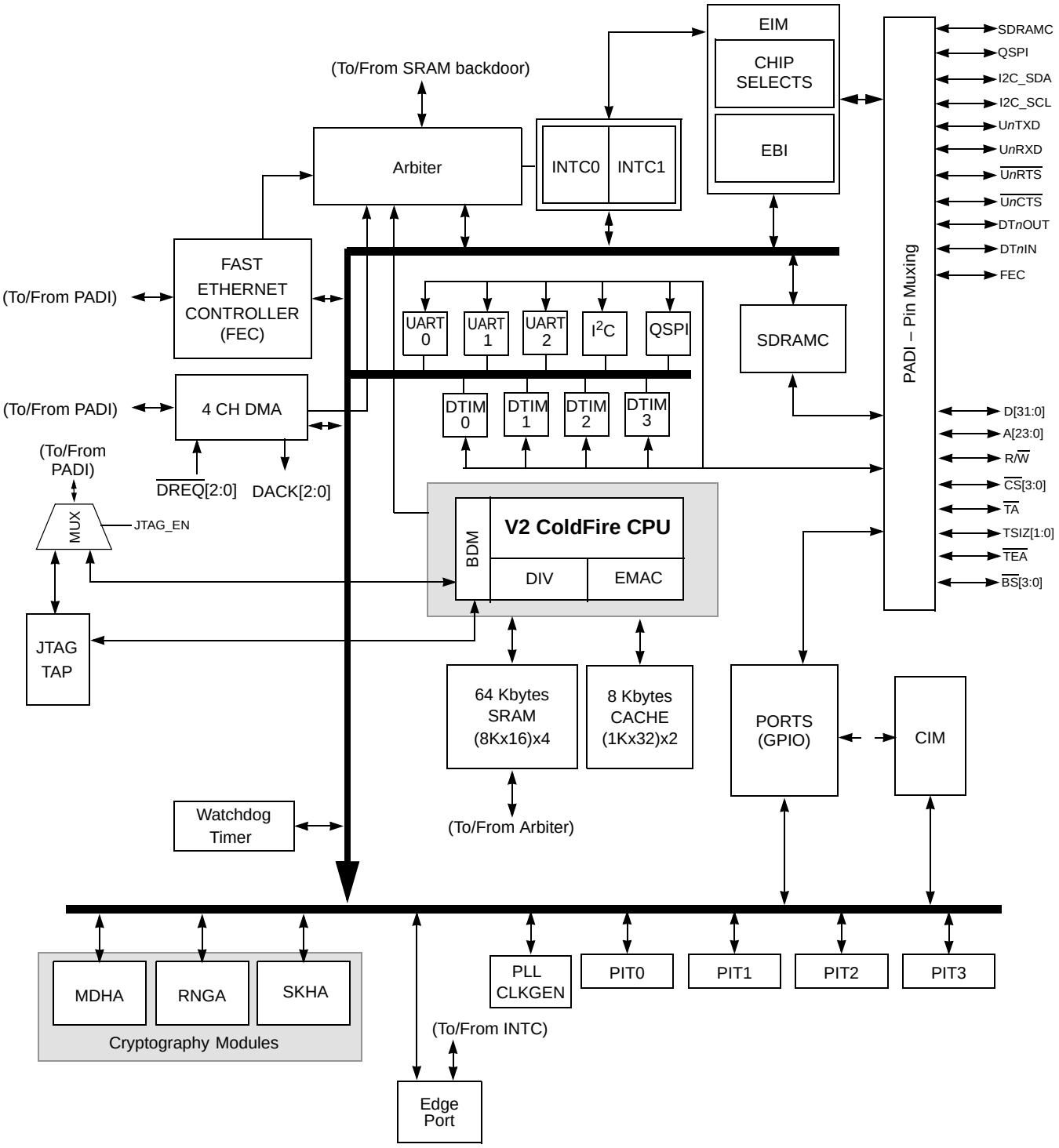

Figure 1. MCF5271 Block Diagram

3 Features

The below section briefly describes the features of the device. Subsequent sections provide more information about the individual modules.

3.1 Feature Overview

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data path on-chip
  - Processor core runs at twice the bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Implements the ColdFire Instruction Set Architecture, ISA_A, with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
  - Enhanced Multiply-Accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging
  - Real time debug support, with two user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - 8-Kbyte cache, configurable as instruction-only, data-only, or split I-/D-cache
  - 64-Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (e.g., DMA, FEC)
- Fast Ethernet Controller (FEC)
  - 10 BaseT capability, half duplex or full duplex
  - 100 BaseT capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII) to external transceiver (PHY)
- Three Universal Asynchronous Receiver Transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic
  - Maskable interrupts
  - DMA support

  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send ($\overline{\text{URTS}}$) and clear-to-send ($\overline{\text{UCTS}}$) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued Serial Peripheral Interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable master bit rates
  - Up to 16 pre-programmed transfers
- Four 32-bit DMA Timers
  - 13-ns resolution at 75 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input-capture capability with programmable trigger edge on input pin
  - Output-compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or reference-compare
  - DMA trigger capability on input capture or reference-compare
- Four Periodic Interrupt Timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software Watchdog Timer
  - 16-bit counter
  - Low power mode support
- Phase Locked Loop (PLL)
  - Crystal or external oscillator reference
  - 8 to 25 MHz reference frequency for normal PLL mode

  - 24 to 75 MHz oscillator reference frequency for 1:1 mode
  - Separate clock output pin
- Interrupt Controllers (x2)
  - Support for up to 41 interrupt sources organized as follows:
    - 34 fully-programmable interrupt sources
    - 7 fixed-level external interrupt sources
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA Controller
  - Four fully programmable channels
  - Dual-address and single-address transfer support with 8-, 16- and 32-bit data capability along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable connections between the four DMA channels and the 14 DMA requesters in the UARTs (6), 32-bit timers (4), and external logic (4)
- External Bus Interface
  - Glueless connections to external memory devices (e.g., SRAM, Flash, ROM, etc.)
  - SDRAM controller supports 8-, 16-, and 32-bit wide memory devices
  - Support for n-1-1-1 burst fetches from page mode Flash
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 32-bit bidirectional data bus
  - 24-bit address bus
  - Up to eight chip selects available
  - Byte/write enables (byte strobes)
  - Ability to boot from external memories that are 8, 16, or 32 bits wide
- Chip Integration Module (CIM)
  - System configuration during reset
  - Selects one of four clock modes
  - Sets boot device and its data port width
  - Configures output pad drive strength

  - Unique part identification number and part revision number
  - Reset
    - Separate reset in and reset out signals
    - Six sources of reset: Power-on reset (POR), External, Software, Watchdog, PLL loss of clock, PLL loss of lock
    - Status flag indication of source of last reset
- General Purpose I/O interface
  - Up to 142 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

3.2 V2 Core Overview

The processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage Instruction Fetch Pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the Operand Execution Pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5271 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands and a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

3.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on the 683xx family of parts.

The on-chip breakpoint resources include a total of 8 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), an address attribute register, a trigger definition register, and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor’s supervisor mode programming model. The breakpoint registers can be

configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

3.4 JTAG

The MCF5271 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 330-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5271 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5271 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5271 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

3.5 On-chip Memories

3.5.1 Cache

The 8-Kbyte cache can be configured into one of three possible organizations: an 8-Kbyte instruction cache, an 8-Kbyte data cache or a split 4-Kbyte instruction/4-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory, organized as 512 lines, each containing 16 bytes of data. The memories consist of a 512-entry tag array (containing addresses and control bits) and a 8-Kbyte data array, organized as 2048 x 32 bits.

If the desired address is mapped into the cache memory, the output of the data array is driven onto the ColdFire core's local data bus, completing the access in a single cycle. If the data is not mapped into the tag memory, a cache miss occurs and the processor core initiates a 16-byte line-sized fetch. The cache module includes a 16-byte line fill buffer used as temporary storage during miss processing. For all data cache configurations, the memory operates in write-through mode and all operand writes generate an external bus cycle.

3.5.2 SRAM

The SRAM module provides a general-purpose 64-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64-Kbyte boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA and FEC non-core bus masters. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

3.6 Fast Ethernet Controller (FEC)

The MCF5271's integrated Fast Ethernet Controller (FEC) performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media.

3.7 UARTs

The MCF5271 contains three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an externally supplied clock. They can use DMA requests on transmit-ready and receive-ready as well as interrupt requests for servicing. Flow control via U*n*$\overline{\text{CTS}}$ and U*n*$\overline{\text{RTS}}$ pins is provided on all three UARTS.

3.8 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

3.9 QSPI

The queued serial peripheral interface module provides a high-speed synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, eliminating CPU intervention between transfers.

3.10 Cryptography

The superset device, MCF5271, incorporates small, fast, dedicated hardware accelerators for random number generation, message digest and hashing, and the DES, 3DES, and AES block cipher functions

allowing for the implementation of common Internet security protocol cryptography operations with performance well in excess of software-only algorithms.

3.11 DMA Timers (DTIM0-DTIM3)

There are four independent, DMA-transfer-generating 32-bit timers (DTIM[3:0]) on the MCF5271. Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN*n* signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCR*n*). Each of these timers can be configured for input capture or reference compare mode. By configuring the internal registers, each timer may be configured to assert an external signal, generate an interrupt on a particular event or cause a DMA transfer.

3.12 Periodic Interrupt Timers (PIT0-PIT3)

The four periodic interrupt timers (PIT[3:0]) are 16-bit timers that provide precise interrupts at regular intervals with minimal processor intervention. Each timer can either count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

3.13 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

3.14 Clock Module and Phase Locked Loop (PLL)

The clock module contains a crystal oscillator (OSC), phase-locked loop (PLL), reduced frequency divider (RFD), status/control registers, and control logic. To improve noise immunity, the PLL and OSC have their own power supply inputs, VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD, VSS, OVDD, and OVSS.

3.15 Interrupt Controllers (INTC0, INTC1)

There are two interrupt controllers on the MCF5271, each of which can support up to 63 interrupt sources each for a total of 126. Each interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 56 of the 63 sources of a given controller provide a programmable level [1-7] and priority within the level.

3.16 DMA Controller

The Direct Memory Access (DMA) Controller Module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four channels (DMA0-DMA3) that allow

byte, word, longword or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR*n*[START] bit. Other sources include the DMA timer, external sources via the DREQ signal, and UARTs. The DMA controller supports dual address to off-chip or on-chip devices.

3.17 External Interface Module (EIM)

The external bus interface handles the transfer of information between the core and memory, peripherals, or other processing elements in the external address space. Features have been added to support external Flash modules, for secondary wait states on reads and writes, and a signal to support Active-Low Address Valid (a signal on most Flash memories).

Programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from read-only access.

3.18 SDRAM Controller

The SDRAM controller provides all required signals for glueless interfacing to a variety of JEDEC-compliant SDRAM devices. SRAS/SCAS address multiplexing is software configurable for different page sizes. To maintain refresh capability without conflicting with concurrent accesses on the address and data buses, SD_SRAS, SD_SCAS, SD_WE, SD_CS[1:0] and SD_CKE are dedicated SDRAM signals.

3.19 Reset

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. The power management registers for the internal low-voltage detect (LVD) circuit are implemented in the reset module. There are six sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software

External reset on the RSTOUT pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

3.20 GPIO

Like the MC68332, unused bus interface and peripheral pins on the MCF5271 can be used as discrete general-purpose inputs and outputs. These are managed by a dedicated GPIO module that logically groups all pins into ports located within a contiguous block of memory-mapped control registers.

All of the pins associated with the external bus interface may be used for several different functions. Their primary function is to provide an external memory interface to access off-chip resources. When not used for this, all of the pins may be used as general-purpose digital I/O pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

The digital I/O pins on the MCF5271 are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

4 Documentation

A list of available documentation which provides a complete description of the MCF5271 and their development support tools is available on the Freescale web page, http://www.freescale.com/coldfire. Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the above Freescale web address.

5 Document Revision History

Table 3 provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Substantive Change(s)
0	- Initial version
1.0	- Device is now available in 150 MHz versions. Updated specs where necessary to reflect this improvement. - Changed instances of Motorola with Freescale throughout. - Corrected various mistakes in Figure 1 block diagram including: removed overbar from DACK signals and added overbars to $\overline{U\textit{n}CTS}$ and $\overline{U\textit{n}RTS}$. - Removed documentation table in Section 4, “Documentation” as it was outdated. Point users to the Freescale web site for the latest list of available documentation.

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