



MPC823 Pin Functions Implemented From MPC821

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MPC821 Pin Description	MPC823 Pin Description	823 Pins
<i>PORT A</i>		
PA15/RXD1	PA15/ USBRXD	1
PA14/TXD1	PA14/ USBOE	1
PA13/RXD2	PA13/RXD2	1
PA12/TXD2	PA12/TXD2	1
PA11/L1TXDB		
PA10/L1RXDB		
PA9/L1TXDA	PA9/L1TXDA/ SMRXD2	1
PA8/L1RXDA	PA8/L1RXDA/ SMTXD2	1
PA7/CLK1.TIN1.L1RCLKA/BRGO1	PA7/CLK1/TIN1/L1RCLKA/BRGO1	1
PA6/CLK2.BRGCLK1/TOUT1	PA6/CLK2/BRGCLK1/TOUT1	1
PA5/CLK3.TIN2.L1TCLKA/BRGO2	PA5/CLK3/TIN2/L1TCLKA/BRGO2	1
PA4/CLK4/TOUT2	PA4/CLK4/ BRGCLK2 /TOUT2	1
PA3/CLK5.TIN3/BRGO3		
PA2/CLK6.L1RCLKB.BRGCLK2/TOUT3		
PA1/CLK7/TIN4/BRGO4		
PA0/CLK8/L1TCLKB/TOUT4		
<i>PORT B</i>		
PB31/RRJCT/SPISEL	PB31/SPISEL/ LCD_A	1
PB30/SPICLK	PB30/SPICLK	1
PB29/SPIMOSI	PB29/SPIMOSI	1
PB28/SPIMISO/BRGO4	PB28/SPIMISO	1
PB27/BRGO1/I2CSDA	PB27/BRGO1/I2CSDA	1
PB26/BRGO2/I2CSCL	PB26/BRGO2/I2CSCL	1
PB25/SMTXD1	PB25/SMTXD1	1
PB24/SMRXD1	PB24/SMRXD1	1
PB23/SMSYN1/SDACK1	PB23/SMSYN1/SDACK1	1

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PB22/SMSYN2/SDACK $\bar{2}$	PB22/SDACK2/SMSYN $\bar{2}$	1
PB21/SMTXD2/L1CLKOB		
PB20/SMRXD2/L1CLKOA		
PB19/L1ST1/RTS $\bar{1}$	PB19/L1ST1/LCD_B	1
PB18/L1ST2/RTS $\bar{2}$	PB18/L1ST2/RTS $\bar{2}$	1
PB17/L1ST3/L1RQB	PB17/L1ST3/LCD_C	1
PB16/L1ST4/L1RQA	PB16/L1ST4/L1RQA	1
PB15/BRGO3		
PB14/RSTRT $\bar{1}$		
<i>PORT C</i>		
PC15/DREQ $\bar{1}$ /RTS1/L1ST1	PC15/DREQ $\bar{1}$ /L1ST5	1
PC14/DREQ2/RTS2/L1ST2	PC14/DREQ2/RTS2/L1ST6	1
PC13/L1RQB/L1ST3	PC13/L1ST7	1
PC12/L1RQA/L1ST4	PC12/L1RQA/L1ST8	1
PC11/CTS $\bar{1}$	PC11/USBRXP	1
PC10/CD1/TGATE $\bar{1}$	PC10/USBRXN/TGATE $\bar{1}$	1
PC9/CTS2	PC9/CTS2	1
PC8/CD2/TGATE $\bar{2}$	PC8/CD2/TGATE $\bar{1}$	1
PC7/L1TSYNCB/SDACK $\bar{2}$	PC7/USBTXP	1
PC6/L1RSYNCB	PC6/USBTXN	1
PC5/L1TSYNCA/SDACK $\bar{1}$	PC5/L1TSYNCA/SDACK $\bar{1}$	1
PC4/L1RSYNCA	PC4/L1RSYNCA	1
<i>PORT D</i>		
PD15/LD8	PD15/LD8/VD7	1
PD14/LD7	PD14/LD7/VD6	1
PD13/LD6	PD13/LD6/VD5	1
PD12/LD5	PD12/LD5/VD4	1
PD11/LD4	PD11/LD4/VD3	1
PD10/LD3	PD10/LD3/VD2	1
PD9/LD2	PD9/LD2/VD1	1
PD8/LD1	PD8/LD1/VD0	1
PD7/LD0	PD7/LD0/FIELD	1
PD6/LCD_AC/LOE	PD6/LCD_AC/LOE//BLANK	1

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PD5/FRAME.VSYNC	PD5/FRAME/VSYNC	1
PD4/LOAD.HSYNC	PD4/LOAD/HSYNC	1
PD3/SHIFT.CLK	PD3/SHIFT/CLK/CLK	1
<i>INTERRUPTS</i>		
IRQ0	IRQ0	1
IRQ1	IRQ1	1
RSV/IRQ2	RSV/IRQ2	1
CR/IRQ3		
KR/RETRY/IRQ4/SPKROUT	KR/RETRY/IRQ4/SPKROUT	1
FRZ/IRQ6	FRZ/IRQ6	1
DP0/IRQ3	DP0/IRQ3	1
DP1/IRQ4	DP1/IRQ4	1
DP2/IRQ5	DP2/IRQ5	1
DP3/IRQ6	DP3/IRQ6	1
IRQ7	IRQ7	1
<i>CLOCKS</i>		
CLKOUT	CLKOUT	1
XFC	XFC	1
XTAL	XTAL	1
EXTAL	EXTAL	1
EXTCLK	EXTCLK	1
TEXP	TEXP	1
RESET		
PORESET	PORESET	1
HRESET	HRESET	1
SRESET	SRESET	1
RSTCONF	RSTCONF	1
<i>JTAG</i>		
TDI/DSDI	TDI/DSDI	1
TDO/DSDO	TDO/DSDO	1
TCK/DSDK	TCK/DSDK	1
TMS	TMS	1

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TRST	TRST	1
<i>BUS I/F</i>		
BS_A0		
BS_A1		
BS_A2		
BS_A3		
WE0/BS_B0/IORD	WE0/BS_AB0/IORD	1
WE1/BS_B1/IOWR	WE1/BS_AB1/IOWR	1
WE2/BS_B2/PCOE	WE2/BS_AB2/PCOE	1
WE3/BS_B3/PCWE	WE3/BS_AB3/PCWE	1
CS0	CS0	1
CS1	CS1	1
CS2	CS2	1
CS3	CS3	1
CS4	CS4	1
CS5	CS5	1
CS6/CE1_B	CS6/CE1_B	1
CS7/CE2_B	CS7/CE2_B	1
CE1_A		
CE2_A		
RD/WR	RD/WR	1
OE/GPL_A1/GPL_B1	OE/GPL_A1/GPL_B1	1
A(0:31)	A(6:31)	26
D(0:31)	D(0:31)	32
BB	BB	1
BG	BG	1
BR	BR	1
BURST	BURST	1
BDIP/GPL_B5	BDIP/GPL_B5	1
BI	BI	1
GPL_A2/GPL_B2/CS2	GPL_A2/GPL_B2/CS2	1
GPL_A3/GPL_B3/CS3	GPL_A3/GPL_B3/CS3	1

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GPL_A0/GPL_B0	GPL_A0/GPL_B0	1
UPWAITA/GPL_A4	UPWAITA/GPL_A4	1
GPL_A5	GPL_A5	1
UPWAITB/GPL_B4	UPWAITB/GPL_B4/ \overline{AS}	1
\overline{TS}	\overline{TS}	1
\overline{TA}	\overline{TA}	1
\overline{TEA}	\overline{TEA}	1
TSIZ0	TSIZ0	1
TSIZ1/ \overline{REG}	TSIZ1/ \overline{REG}	1
ALE_A		
ALE_B/DSCK/AT1	ALE_B/DSCK/AT1	1
OP(0:1)		
OP2/MODCK1/ \overline{STS}	OP2/MODCK1/ \overline{STS}	1
OP3/MODCK2/DSDO	OP3/MODCK2/DSDO	1
<i>EXTERNAL MASTER</i>		
\overline{AS}		
BADDR(28:29)		
BADD(30)/ \overline{REG}		
<i>PCMCIA_A</i>		
$\overline{WAIT_A}$		
IP_A(0:1)		
IP_A2/ $\overline{IOIS16_A}$		
IP_A(3:7)		
<i>PCMCIA_B</i>		
$\overline{WAIT_B}$	$\overline{WAIT_B}$	1
IP_B(0:1)/IWP(0:1)/VFLS(0:1)	IP_B(0:1)/IWP(0:1)/VFLS(0:1)	2
IP_B2/ $\overline{IOIS16_B}$ /AT2	IP_B2/ $\overline{IOIS16_B}$ /AT2	1
IP_B3/IWP2/VF2	IP_B3/IWP2/VF2	1
IP_B4/LWP0/VF0	IP_B4/LWP0/VF0	1
IP_B5/LWP1/VF1	IP_B5/LWP1/VF1	1
IP_B6/DSDI/AT0	IP_B6/DSDI/AT0	1



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IP_B7/PTR/AT3	IP_B7/PTR/AT3	1
<i>MISC</i>		
VDDSYN	VDDSYN	1
VSSSYN	VSSSYN	1
VSSSYN1	VSSSYN1	1
KAPWR	KAPWR	1
VDDL	VDDL	4
SPARE(1:4)	SPARE(1:4)	4
226		187