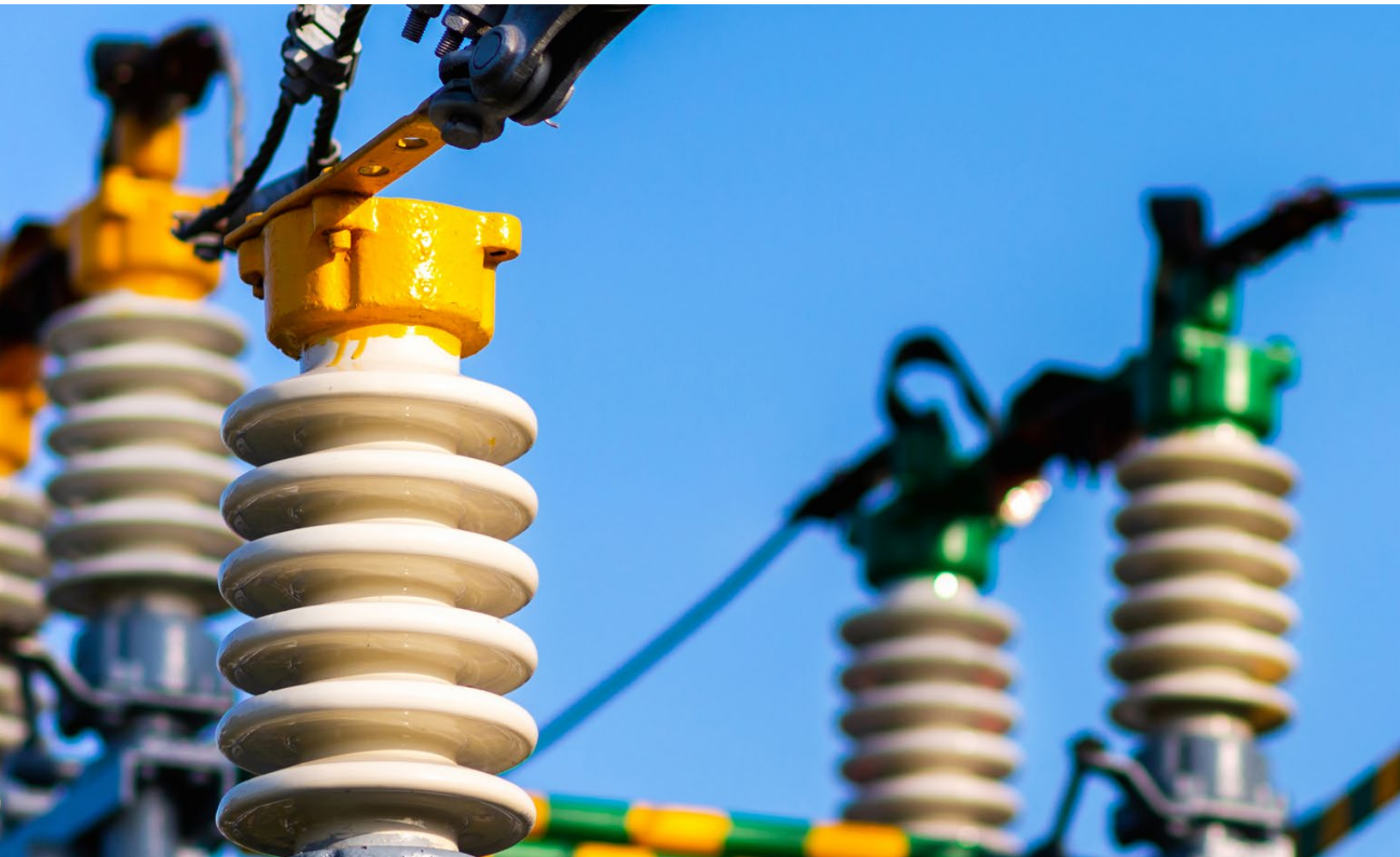**HOW TO MANAGE
MIXED-VOLTAGE
DESIGNS WITH NXP
LEVEL TRANSLATORS**

VOLTAGE
TRANSLATION

NXP

VOLTAGE
TRANSMISSION

HOW TO MANAGE MIXED-VOLTAGE DESIGNS WITH NXP LEVEL TRANSLATORS

Table of contents

SECTION 1

WHY VOLTAGE TRANSLATION MATTERS

In recent years, voltage translation has become an important part of electronic design, especially in portable applications. That's because the latest data and application processors for mobile applications are typically produced in advanced, low-power CMOS process technologies that use a supply voltage of 1.8 V or lower. But the peripherals they connect to, including memories, image sensors, relays, and RF transceivers, are more likely to use older, lower-cost process technologies that operate at higher levels, at or above 3 or 5 V. Voltage level translators (Figure 1-1) enable these different devices to work together, without producing damaging current flow or signal loss, so the system operates more efficiently and saves power.
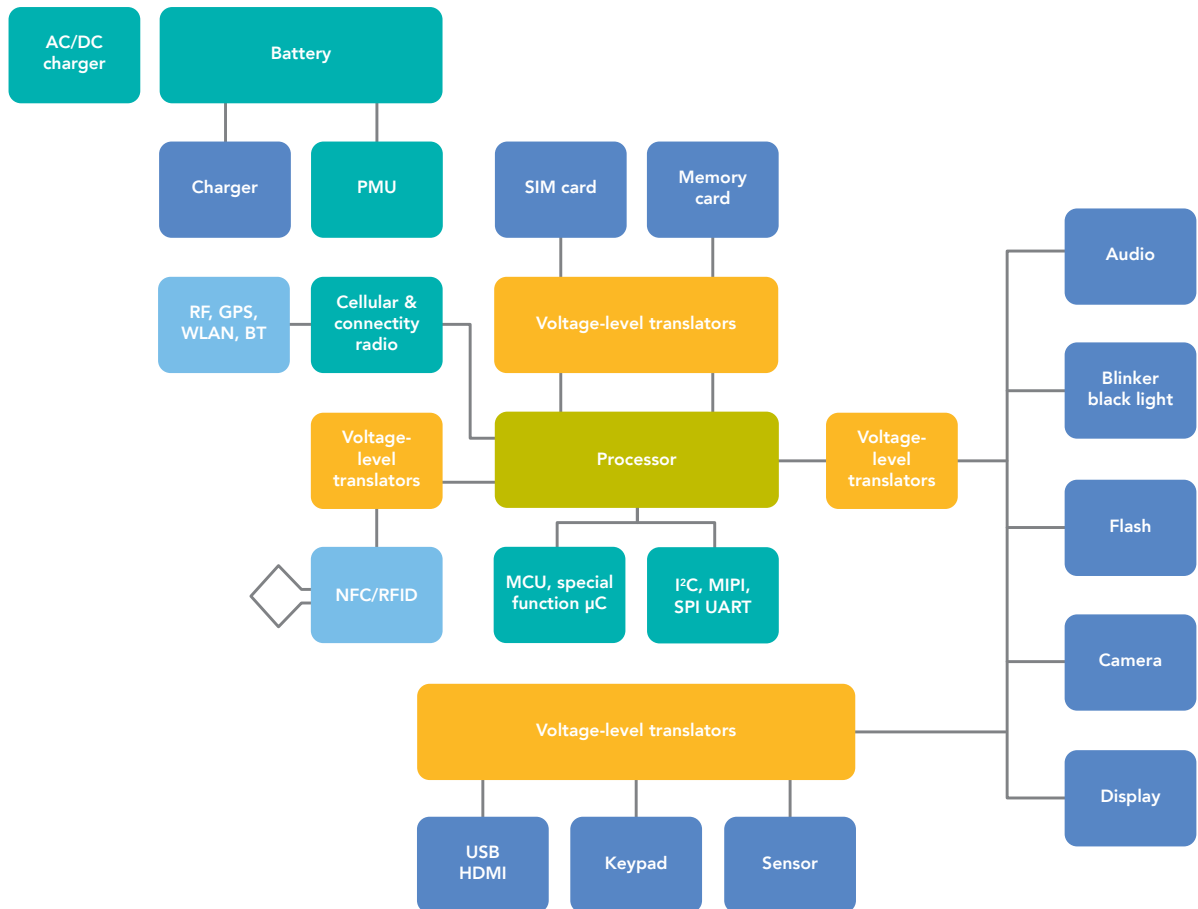
Figure 1-1. Typical portable application with voltage-level translators
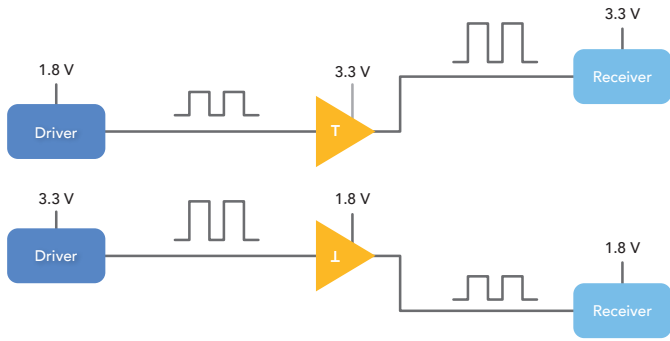
Figure 1-2. Shifting the output voltage level up or down

A QUICK OVERVIEW

In most mixed-voltage designs, the output voltage level of a driver device needs to be shifted up or down so that the receiver device can interpret it correctly, or vice versa (Figure 1-2).

There are often variations in the logic switching input (V_{IH} and V_{IL}) and the output levels (V_{OH} and V_{OL}) for commonly used logic devices in the range of 3 and 5 V (Figure 1-3).

Figure 1-3. Switching input and output levels for 3 V and 5 V logic devices

Figure 1-4. Incompatible voltages can cause unpredictable system behavior

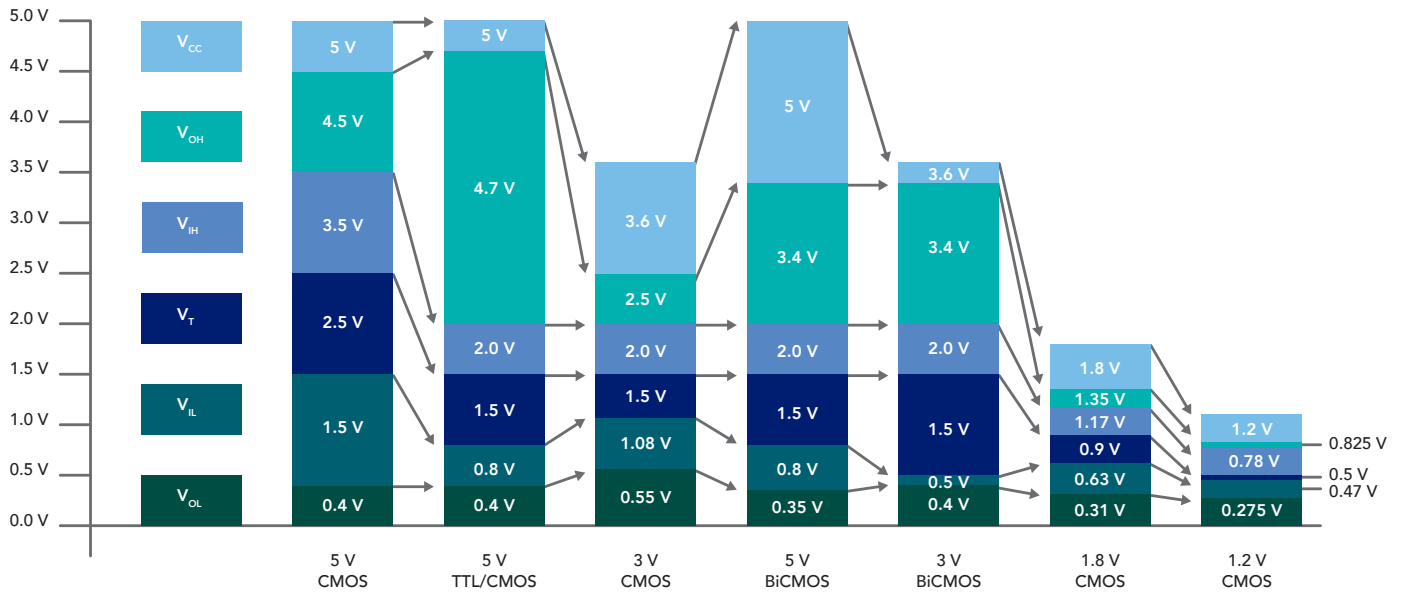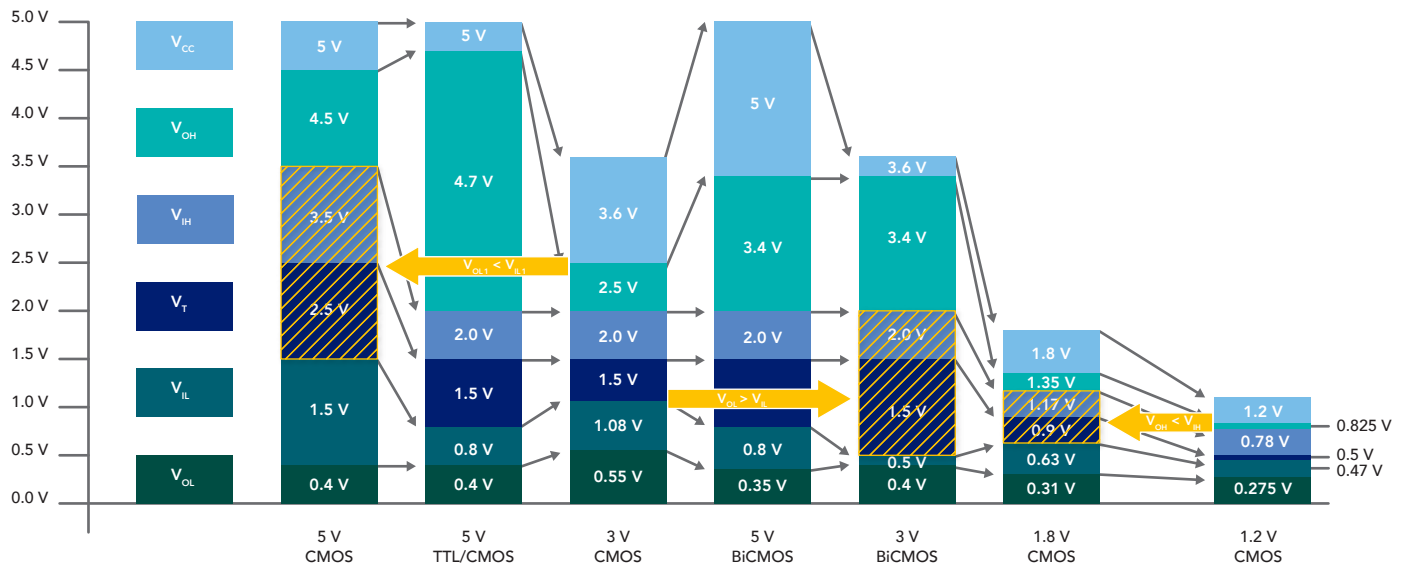When the driver V_{OH} is less than the receiver V_{IH}, and/or the driver V_{OL} is greater than the receiver V_{IL}, system behavior becomes unpredictable (Figure 1-4).

Configuring the system to translate voltages from high to low or from low to high, according to the recommended guidelines for the input and output voltage levels of each component, makes the system more predictable, improves overall performance, and saves energy.

UNIDIRECTIONAL AND BIDIRECTIONAL DEVICES

Devices that translate voltages from low to high levels or from high to low levels also transfer data. The data transfer can work in one direction (unidirectional) or in two directions (bidirectional). Figure 1-5 shows a digital camera that uses the 74AUP1T45, a bidirectional logic level translator, to translate between the color processor, which uses 1.8 V signals, and the memory subsystem, which uses 3.3 V signals.
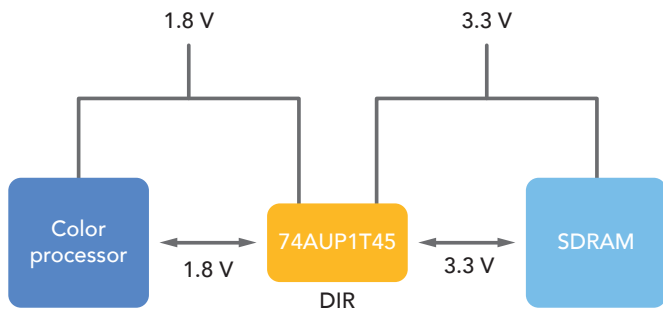
Figure 1-5. Low-to-high level translation in a digital camera

Some bidirectional translators like the 74AUP1T45 have a direction pin (DIR) to control the direction of data. Others have both DIR and Output Enable (OE) pins for tri-stating the output, ideal for applications connecting to a single bus. Another feature, called autodirection sensing, has no DIR pin. This feature eliminates the need for a separate direction control pin since they can change the direction of the data flow automatically. Autodirection sensing helps reduce the number of control pins required in the system for data flow, for example I²C-Bus where there is an acknowledge every 8 bits.

FIND THE RIGHT TRANSLATOR FOR YOUR DESIGN

NXP offers level translators for specific protocols and translators that work in general-purpose applications. This guide can help you find the right one for your design.

Table 1-1 lists the families available from NXP. Active devices include a CMOS output stage with a specific source and sink currents. Passive devices do not have CMOS outputs; the sink and source currents come from the supply voltage.

TABLE 1-1. NXP LEVEL TRANSLATORS

TYPE	DRIVE	NXP FAMILIES	DESCRIPTION
Bidirectional with direction pin	Active	GTL	These devices perform bidirectional level translation and have a direction pin that sets the direction of the data flow. GTL level translators are specially designed to support GTL logic, which is widely used on processors. They convert GTL levels to LVTTL levels.
Bidirectional with auto direction sensing	Active	NTB, PCA	These devices perform bidirectional level translation without a direction pin. The NTB and NTS translators integrate one-shot edge accelerators. The NTB and PCA families support buffered outputs. The NTS and NTB families have integrated pull-ups, and are a good choice for applications that use interfaces based on I²C, SMBus, SPI, or UARTs. The NTS are preferred for open drain applications and the NTB for push pull applications. The NVT and PCA9306 are good for both open drain and push pull applications. The PCA95xx and PCA96xx are exclusively for I2C or SMBus applications.
	Passive	NTS, NVT	
Application specific	Active	NVT level shifters for SIM and SD cards	The NVT SIM and SD card level shifters contain an LDO that can deliver two different voltages, from a typical mobile phone battery voltage, and convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller. There are SIM/SD level shifters that do not have an internal LDO. An external LDO can be used to supply the power to the SIM/SD card.
	Passive	PCA muxes and switches for I²C	These multiplexers and switches split the I²C-bus into several branches, so the I²C leader can select and address multiple identical devices without address conflicts. They also permit a single controller to interface with multiple targets with different power-supply voltages.

SECTION 2

BIDIRECTIONAL LEVEL TRANSLATORS WITH DIRECTION PIN

Voltage translators that are equipped with two supply voltages, each supporting a different voltage range, can be used to translate from low to high or from high to low, and are typically available in versions that support either unidirectional or bidirectional level translation.

The devices in this section use the DIR pin to control the direction of translation, from the A to the B port or from the B to the A port. Integrated I_{OFF} circuitry eliminates damaging backflow current when outputs are disabled during suspend or power-down mode. They are active translators, meaning they have a CMOS output stage with specific source and sink currents.

Bidirectional translators equipped with a direction pin are available with the NXP GTL family.

GTL-TO-LVTTL LEVEL TRANSLATORS AND TRANSCEIVERS

Gunning transceiver logic (GTL) is a type of logic signaling used to drive electronic backplane buses. Defined by the JEDEC standard JESD 8-3, GTL has a voltage swing between 0.4 and 1.5 V — much lower than that used in TTL and CMOS logic — and performs symmetrical parallel resistive termination.

GTL is often found in front-side buses based on the Intel architecture. For GTL signals to be compatible with the rest of the system, GTL levels need to be translated to low-voltage TTL (LVTTL). NXP offers dedicated translators and transceivers for the GTL format.

TABLE 2-1. SELECT NXP DEVICES FOR GTL-TO-LVTTL TRANSLATION

TYPE NUMBER	DESCRIPTION	OPERATING RANGE (V)	LVTTL 5 V TOLERANCE	PACKAGE NAME
GTL2012	2-bit LVTTL to GTL transceiver	3.0 to 3.6	Yes (Input only)	TSSOP8
GTL2014	4-bit LVTTL to GTL transceiver	3.0 to 3.6	Yes (Input only)	TSSOP14
GTL2018	8-bit LVTTL to GTL transceiver	3.0 to 3.6	Yes (Input only)	TSSOP24
GTL2034	4-bit GTL to GTL buffer	3.0 to 3.6	No	TSSOP14

For the complete portfolio, visit www.nxp.com/VLT

BIDIRECTIONAL LEVEL TRANSLATORS WITH AUTO DIRECTION SENSING

These are dual-supply translators that use both the DIR and OE pins to tri-state the output; they automatically sense the direction of the data flow. This eliminates the need for an external direction pin and the associated control logic. Auto-direction sensing makes these devices especially suited for applications where the microcontroller doesn't have enough GPIO to change the direction of data flow, since the translators can be added to the design without external GPIO extenders or multiplexers on the PCB.

Level translators with auto direction sensing are available in active and passive formats. The active devices have a CMOS output stage with a specific source and sink. The passive devices do not have CMOS outputs; the sink and source currents come from the supply voltage. Level translators with auto direction sensing are available in active and passive formats. The active devices have a CMOS output stage with a specific source and sink.

3.1 Active devices for bidirectional level translation with auto direction

PCA: DUAL SUPPLY LEVEL-TRANSLATING BUS BUFFERS FOR I^{2}C APPLICATIONS

Systems that use I^{2}C (and SMBus or similar) devices operating at different voltage levels may need to be attached to a common bus. PCA dual supply bus buffers translate between 0.8 and 5.5 V, allowing devices specified for different voltages to be connected to the same bus. For example, a 5 V I^{2}C controller on one segment of the bus can communicate with a 1.8 V (non 5 V-tolerant) SMBus target on a different segment.

PCA bus buffers use active open drain drivers and isolate bus capacitance on each side of the device. The I^{2}C device maintains its functions and operating mode during the level shift, and the dual supply pins can be powered up in any sequence. When any of the supply pins are unpowered, the I/O are high-impedance.

Many PCA bus buffers are specifically designed for level-shifting applications with two supply pins. They are bidirectional and require no direction control. The level-shifting bus buffers support two I^{2}C (or SMBus) branches of up to 400 pF (Figure 4-1). They can be used to extend the bus to support loads larger than the 400 pF maximum.

The bus can be extended with more devices or longer bus lengths, or both. PCA devices are multi-controller capable and support arbitration and bus contention on any segment.
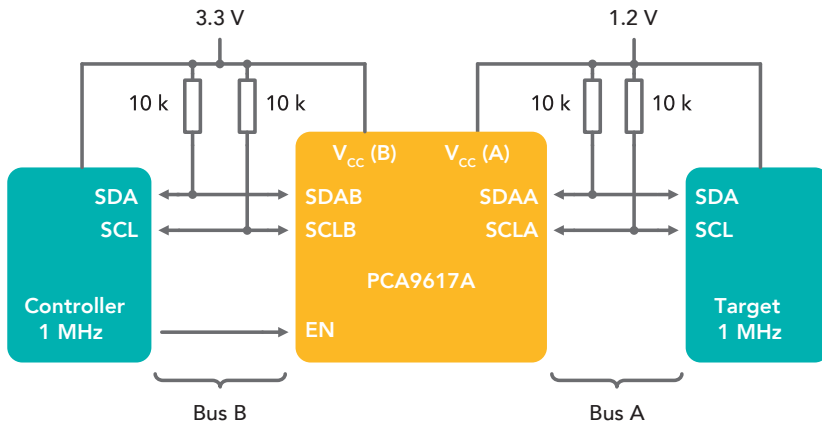
Figure 3-1. Typical application of PCA level-shifting bus buffer

PCA dual supply bus buffers can be used to extend or isolate the bus. See NXP application note AN10418.

TABLE 3-1. SELECT PCA DUAL SUPPLY BUS BUFFERS

TYPE NUMBER	DESCRIPTION	VCC(A) (V)	VCC(B) (V)	CHANNELS	A-SIDE OFFSET	B-SIDE OFFSET	PACKAGE NAME
PCA9507	2.7 V-to-5.5 V level shifter	2.7 to 5.5	2.7 to 5.5	2	Normal	Static offset	SO8, TSSOP8
PCA9508	0.9 V to 5.5 V level shifter with offset free hot-swap	0.9 to 5.5	2.7 to 5.5	2	Normal	Static offset	SO8, TSSOP8
PCA9509	1.0 V to 5.5 V level shifter	1.0 to $(V_{CC}(B) - 1)$	3.0 to 5.5	2	Static offset	Normal	SO8, TSSOP8, XQFN8
PCA9509P	0.8 to 5.5 V level shifter	0.8 to 2.0	2.3 to 5.5	2	Static offset	Normal	TSSOP8, XQFN8
PCA9512A	2.7 to 5.5 V level shifter	2.7 to 5.5	2.7 to 5.5	2	Incremental	Incremental	SO8, TSSOP8
PCA9517A	0.9 V to 5.5 V level shifter	0.9 to 5.5	2.7 to 5.5	2	Normal	Static offset	SO8, TSSOP8, HWSON8
PCA9519	1.1 V to 5.5 V quad level shifter	1.1 to $(V_{CC}(B) - 1)$	3.0 to 5.5	4	Static offset	Normal	TSSOP20, HVQFN24
PCA9527	3.0 V to 5.5 V level shifter	2.7 to 5.5	2.7 to 3.6	3	Normal	Static offset	TSSOP10
PCA9617A	0.8 V to 5.5 V level shifter	0.8 to 5.5	2.2 to 5.5	2	Normal	Static offset	TSSOP8, HWSON8

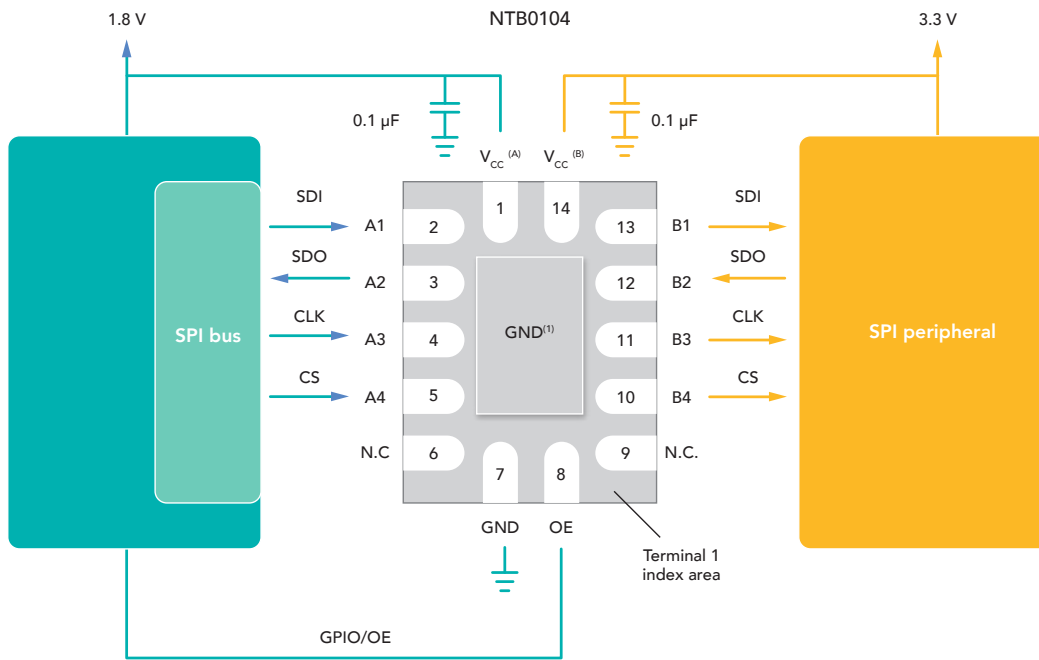For the complete portfolio, visit www.nxp.com/BusBuffer

Figure 3-2. Four-channel NTB0104 used in SPI level-shifting application

NTB LEVEL SHIFTERS: BIDIRECTIONAL LEVEL TRANSLATION WITH AUTO-DIRECTION SENSING

NTB level shifters (Figure 3-2) are ideal for use as push-pull or CMOS-type drivers that drive long-trace, capacitive, or high-impedance loads in applications that use SPI, Secure Digital, or UART interfaces. Figure 3-3 shows the architecture of one I/O channel of an NTB level translator. The translator incorporates a weak buffer with one-shot circuitry to improve switching speeds for rising and falling edges. When the A port is connected to a system driver and driven high, the weak 4 kΩ buffer drives the B port high in conjunction with the upper one shot, which becomes active when it senses a rising edge. The B port is driven high by both the buffer and the T1 PMOS, which lowers the output impedance seen on the B port while the one-shot circuit is active. On the falling edge, the lower one-shot is triggered and the buffer, along with the T2 NMOS, lowers the output impedance seen on the B port while the one-shot circuit is operating and the output is driven low.

Figure 3-4 shows the active circuitry in the NTB I/O channel during translations from low to high and high to low. The weak buffer is shown in orange and the active one-shot circuit is in green. Figure 3-5 gives the input and output waveforms with edge acceleration.
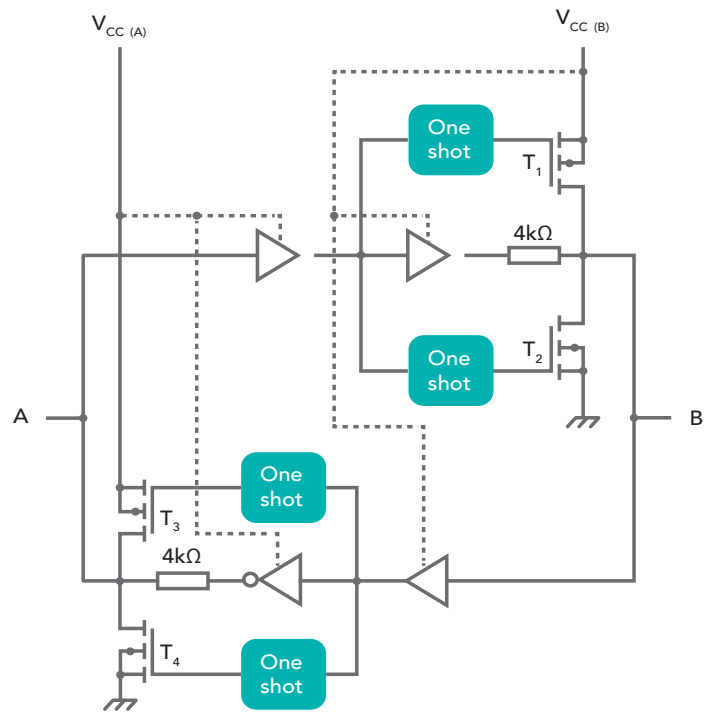
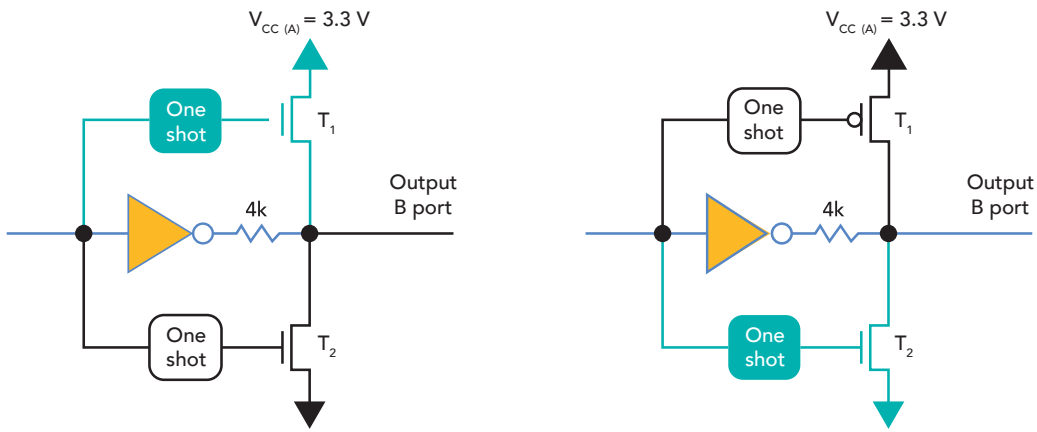Figure 3-3. Architecture of single NTB I/O cell

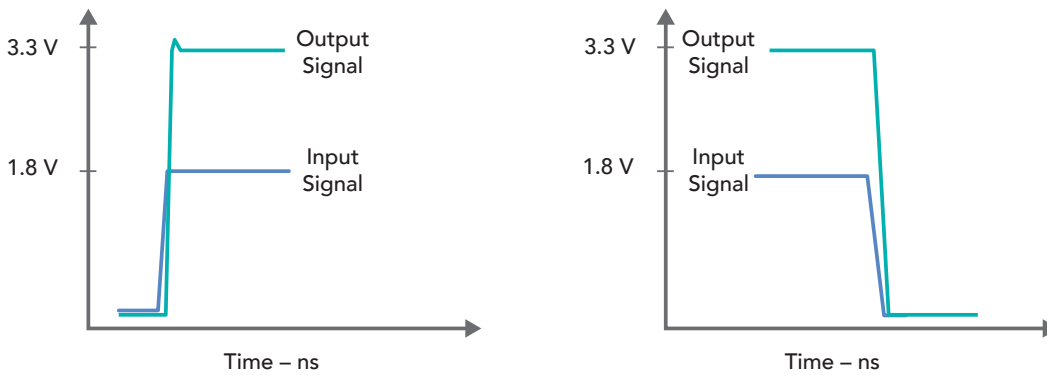Figure 3-4. Active one-shot and weak buffer structures in NTB I/O channel

Figure 3-5. Input and output waveforms with edge acceleration

The one-shot circuits in NTB devices reduce the output impedance during low-to-high and high-to-low transitions so that the propagation delays can be minimized with faster edges. Once the transition is complete, the one-shot circuit times out and port B is held high or low by the weak buffer and the integrated 4 kΩ resistor at the buffer output. NTB is a weak buffered device since the buffer is strong enough to hold the output port high or low in static state but is weak enough to be overridden by an external driver when the direction is changed.

INPUT DRIVER REQUIREMENTS

The input driver should have at least ±2 mA drive current capability to drive the I/O of NTB devices. Input current versus input voltage graph for NTB devices is shown in Figure 3-6.

VT : supply voltage of the external driver

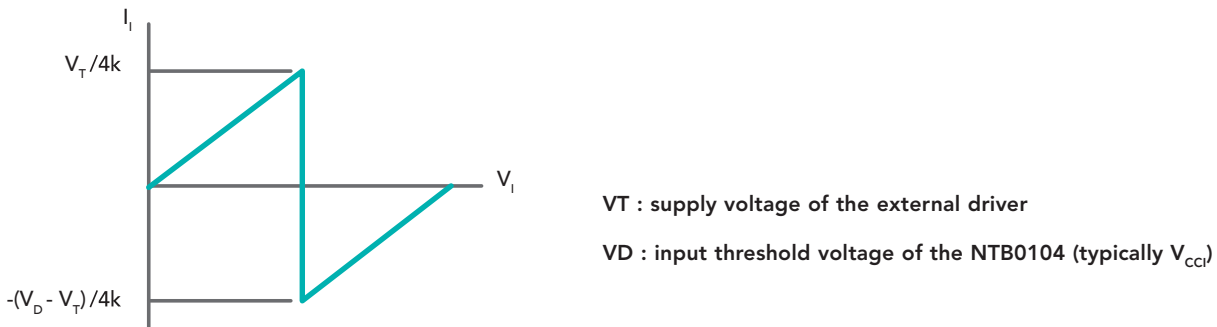**VD : input threshold voltage of the NTB0104 (typically V_{CCI})**

Figure 3-6. Typical input current versus input voltage (NTB)

Since NTB buffers are designed for driving high-impedance loads, it is important to carefully select the external pull-up or pull-down resistors if they are used in the application. For any external pull-up or pull-down resistor used with the NTB resistor, a resistor divider network is formed with a 4 kΩ buffer. The value of the external resistor should be large enough (typically greater than 50 kΩ) so that there is little change on V_{OH} or V_{OL} levels.

For example, the value of V_{OL} can be determined from the following equation, when a 50 kΩ external pull-up is used:

$$V_{OL} = 4k/50k + 4k \times V_{cco} = 0.075 \times V_{cco}$$

During output transitions, the typical output impedance is 70 Ω at V_{CCO} equals 1.2 to 1.8 V, 50 Ω at V_{CCO} equals 1.8 to 3.3 V and 40 Ω at V_{CCO} equals 3.3 to 5.0 V. When the circuits are active, a resulting high AC drive is realized by turning on T1 and the rising edge speeds up. The output port is maintained at a high signal level through this 4 kΩ internal resistor. During low-to-high transitions, one-shot circuits turn on the PMOS transistors T1 for a short time, accelerating the output edges. However, the one-shot circuits are turned off when output voltage reaches approximately 95% of the steady-state value. For high-to-low output transitions, the one-shot turns off when output voltage reaches approximately 5% of the steady-state value.

OUTPUT-ENABLE (OE) CONTROL

NTB level translators offer a maximum power consumption of 5 µA when OE is high. When the OE is low, the NTB translator buffer will be disabled and the outputs are put into high impedance for increased power savings. The OE pin is referenced to $V_{CC(A)}$ voltage supply and when outputs are disabled, the one-shot and 4 kΩ buffer are also disabled for both the A and B ports. In this state, output leakage I_{OZ} will be less than ±2 µA. If the application does not require output-enable control, the OE pin should be tied to $V_{CC(A)}$ supply and must never be left floating. A floating OE results in excessive quiescent current consumed by the device, which increases the total power consumption. Unwanted output oscillations may also result due to indeterminate logic level at /OE pin.

The outputs of NTB devices are tri-stated in case any of the two power supplies is 0 V. This feature, called V_{CC} isolation, means that if $V_{CC(B)}$ or $V_{CC(A)}$ equals 0 V, the I/O of A and B ports are in high impedance. These devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the presence of damaging backflow current when the device is powered down.

TABLE 3-2. SELECT NTB LEVEL SHIFTERS FOR BIDIRECTIONAL TRANSLATION

TYPE NUMBER	DESCRIPTION	$V_{CC(A)}$ (V)	$V_{CC(B)}$ (V)	OUTPUT DRIVE CAPABILITY (MA)	TPD (NS)	NUMBER OF BITS	TAMB (°C)	PACKAGE
NTB0101	1-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	1	-40 to +125	TSSOP6
NTB0102	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	2	-40 to +125	TSSOP8, XSON8
NTB0104	4-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	4	-40 to +125	DHVQFN14, XQFN12, WLCSP

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3.2 Passive devices for bidirectional level translation with auto direction

NTS LEVEL SHIFTERS: BIDIRECTIONAL LEVEL TRANSLATION WITH AUTO- DIRECTION SENSING AND OPEN-DRAIN OUTPUTS

NTS level shifters are switch-type translators suitable for open-drain drivers. They are FET-based devices that use an N-channel pass-gate transistor that ties the two ports together (Figure 3-7), and do not need an extra input signal to change the direction of data from port A to B or from port B to A.

The combination of an N-channel pass FET, integrated

10 kΩ pull-up resistors, and edge-rate acceleration circuits makes NTS translators ideal for interfacing devices or systems operating at disparate voltage levels, while also allowing for simple interfacing with open-drain drivers, as is required in I²C, 1-wire, and SD/MMC-card interface applications. Figure 3-8 shows the application of two- and four-channel NTS level shifters in an SD card reference design.
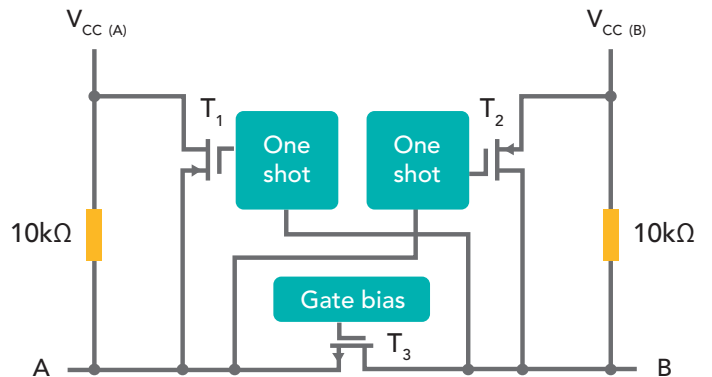
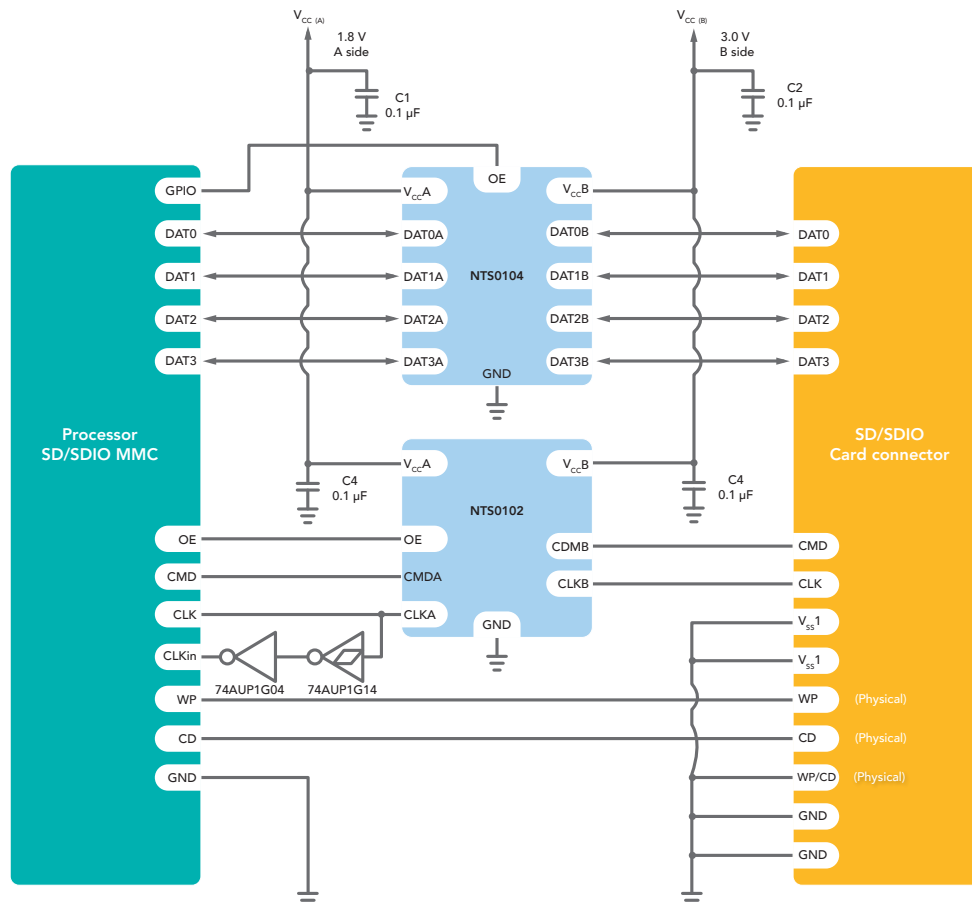Figure 3-7. Architecture of single I/O channel in NTS level shifter

Figure 3-8. NTS level shifter in SD-card reference design

The N-channel pass-gate transistor is used to open and close the connection between the A and B ports. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N-channel pass-gate transistor. The gate bias voltage of the pass-gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side.

During a low-to-high transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2), bypassing the 10 kΩ pull-up resistors, and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI/2}$, and is deactivated approximately 50 ns after the output reaches $V_{CCO/2}$. During the acceleration time, the driver output resistance is between approximately 50 and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn off before applying a signal in the opposite direction.

The pass-gate transistor T3 is on when V_{GS} is greater than VT. When one side of T3 is held low by an external driver, with the input to T3 at 0 V, T3 will be on and the output of T3 will be held to nearly 0 V due to the on-state resistance of T3. As the input voltage rises due to a rising edge, the output voltage of T3 tracks the input until the input voltage reaches V_{GATE} minus VT and T3 turns off. After T3 stops conducting, the input and output ports continue to rise to their respective supply voltages due to the internal pull-up resistors. In the second case, both ports start with high levels since the integrated pull-up resistors tie the inputs to the respective supply voltages, $V_{CC(A)}$ and $V_{CC(B)}$. When the input ports are pulled low by external drivers, T3 starts to conduct when V_{GS} is greater than VT and output starts tracking the input. The source current needed for this operation must be provided by the external driver connected to the A or B port.

To achieve faster data rates through the device, NTS translators include rising edge-rate acceleration circuitry to provide stronger AC-drive by bypassing the integrated 10 kΩ pull-up resistors through a low-impedance path during low-to-high signal transitions. A one-shot circuit with associated T1/T2 PMOS transistors is used to increase switching speeds for the rising-edge input signals. When a rising edge is detected by the one-shot circuit, the T1/T2 PMOS transistors turn on momentarily to rapidly drive the port high, effectively lowering the output impedance seen on that port and speeding up the rising-edge inputs.

INPUT DRIVER REQUIREMENTS

Since NTS level shifters are switch-type level shifters, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the maximum data rate high-to-low output transition time (tTHL) and the propagation delay (tPHL) depend on the output impedance and the edge rate of the external driver. The limits provided in the datasheet for these parameters assume use of a driver with output impedance below 50 Ω.

OUTPUT LOAD CONSIDERATIONS

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration. Capacitive loads up to 150 pF can be driven without any issues using NTS level shifters. Figure 3-9 shows the yellow input waveform and purple output waveform for an NTS0102 driving a load of 70 pF and 50 Ω. A supply voltage of 1.8 V is used for the $V_{CC(A)}$ rail and a supply voltage of 3.3 V is used for the $V_{CC(B)}$ rail. A 1.8 V input signal with a 50 kHz frequency is used, and output swings up to approximately 3.24 V.
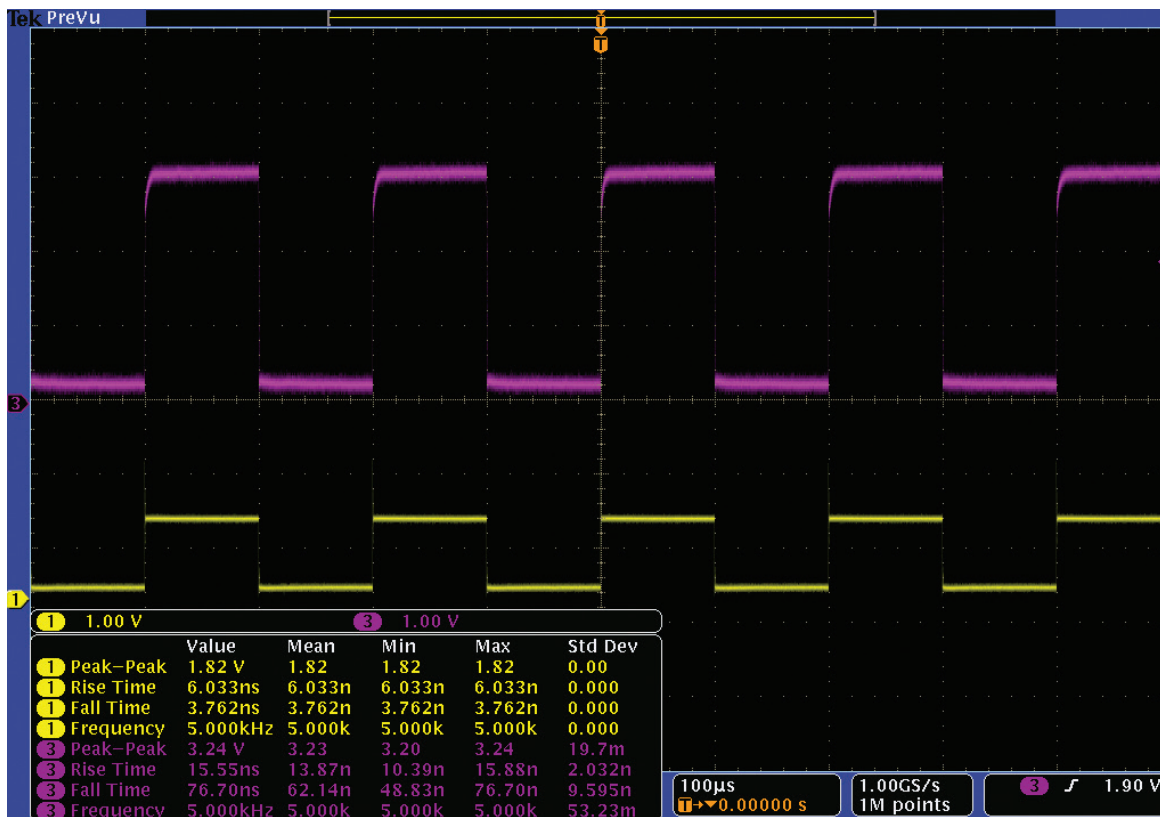
Figure 3-9. NTS0102 driving a load of 70 pF and 50 Ω

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, it's recommended to use short trace lengths and low-capacitance connectors on NTS0102 PCB layouts. To ensure low-impedance termination, and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). The NTS030x devices are designed with longer one shot length with ability to drive larger capacitance loads but at lower maximum frequencies.

POWER-UP CONSIDERATIONS

During operation, $V_{CC(A)}$ must never be higher than $V_{CC(B)}$. However, during power-up, having $V_{CC(A)}$ greater than $V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS devices include circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

ENABLE AND DISABLE OPERATION

An OE input is used to disable the device. Setting OE to low causes all I/O to assume the high-impedance off-state. The disable time (tdis with no external load) indicates the delay from when OE goes low and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken high. To ensure the high-impedance off-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

PULL-UP OR PULL-DOWN RESISTORS ON I/O LINES

Each A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$, and each B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 kΩ. This will affect the V_{OL} level. When OE goes low the internal pull-ups of the NTS0102 are disabled.

NTSX LEVEL SHIFTERS: BIDIRECTIONAL LEVEL TRANSLATION WITH AUTO-DIRECTION SENSING, OPEN-DRAIN OUTPUTS, AND DUAL-EDGE ACCELERATORS

NTSX level shifters are similar to NTS devices but use a modified architecture that enables use at higher capacitive loads (typically up to 600 pF). Figure 3-10 gives the architecture of a single NTSX I/O channel.

There are two N-channel pass-gate transistors that tie the ports together. There is an output edge-rate accelerator that detects and accelerates rising and falling edges on the I/O pins (Figure 3-11).

During an input transition, a one-shot accelerates the output transition by switching on the PMOS transistors (T1, T3) for a low-to-high transition. Alternatively, the one-shot switches on the NMOS transistors (T2, T4) for a high-to-low transition (Figure 3-12). Once activated, the one-shot is deactivated after approximately 25 ns. During the acceleration time, the driver output resistance is between approximately 10 and 35 Ω. To avoid signal contention, the application must not exceed the maximum data rate or must wait for the one-shot circuit to turn off before applying a signal in the opposite direction.

INPUT DRIVER REQUIREMENTS

Because the NTSX2102 is a switch-type translator, properties of the input driver directly affect the output signal. The external open-drain driver applied to an I/O determines the static current sinking capability of the system. The maximum data rate, output transition times (tTHL, tTLH), and propagation delays (tPHL, tPLH) depend on the output impedance and the edge-rate of the external driver.
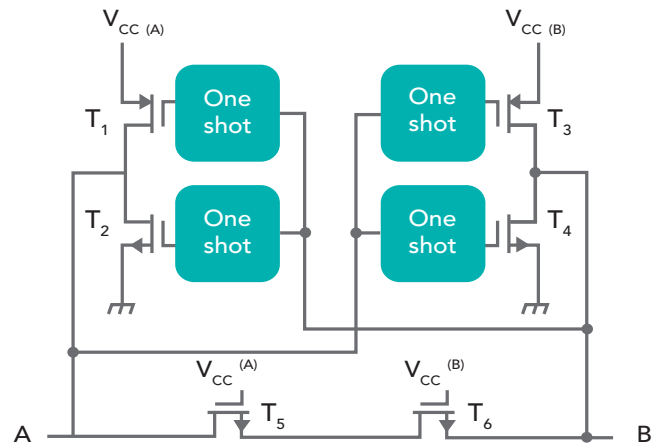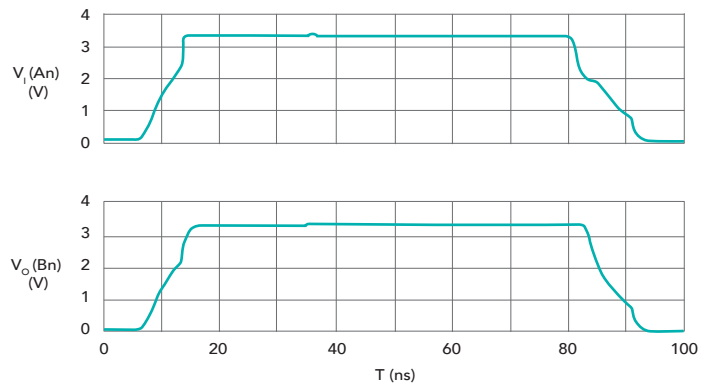

Figure 3-10. Architecture of NTSX2102 I/O channel

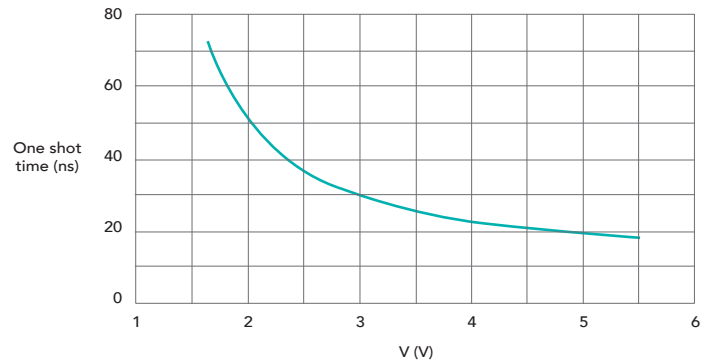Figure 3-11. Input and output waveforms showing edge-rate acceleration

Figure 3-12. One-shot pulse time versus V_{CCO}

OUTPUT LOAD CONSIDERATIONS

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration and has been tuned to 600 pF. In cases with higher capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and ensure correct triggering of the one-shot, use short trace lengths and low-capacitance connectors on NTSX2102 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration. Such a length ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

OUTPUT ENABLE (OE)

An OE input is used to disable the device. Setting OE to low causes all I/O to assume the high-impedance off-state. One of the advantages of NTSX translators is that either $V_{CC(A)}$ or $V_{CC(B)}$ can be powered up first. Defining the OE pin reduces dissipation during power-up. The OE pin can be connected via a pull-down resistor to GND or, if the application allows, hardwired to $V_{CC(A)}$. If the OE pin is hardwired to $V_{CC(A)}$, either supply can be powered up or down first. If a pull-down is used, the following sequences are recommended.

For power-up
1. Apply power to either supply pin
2. Apply power to the other supply pin
3. Enable the device by driving OE high

For power-down
1. Disable the device by driving OE low
2. Remove power from either supply pin
3. Remove power from the other supply pin

TABLE 3-3. SELECT NTS AND NTSX LEVEL SHIFTERS FOR BIDIRECTIONAL TRANSLATION

TYPE NUMBER	DESCRIPTION	VCC(A) (V)	VCC(B) (V)	OUTPUT DRIVE CAPABILITY (mA)	TPD (NS)	NUMBER OF BITS	Tamb (°C)	PACKAGE
NTS0101	1-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	-0.02	4.5	1	-40 to +125	TSSOP6
NTS0102	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	-0.02	4.5	2	-40 to +125	TSSOP8, XSON8, HXSON8, X2SON8
NTS0104	4-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	-0.02	4.5	4	-40 to +125	DHVQFN14, XQFN12, TSSOP14, WLCSP
NTSX2101	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	6	2	2	-40 to +125	XSON8, XQFN8, X2SON8
NTS0302	2-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	X2SON8
NTS0304E	4-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	TSSOP14, WLCSP12
NTS0308E	8-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	TSSOP20

For the complete portfolio, visit www.nxp.com/VLT

NVT LEVEL SHIFTERS: BIDIRECTIONAL LEVEL TRANSLATION WITH AUTO-DIRECTION SENSING, OPEN-DRAIN OUTPUTS, NO EXTERNAL PULL-UPS

NVT level shifters perform bidirectional translation using an array of matching N-channel pass transistors with their gates tied together internally at the enable (EN) pin (Figure 3-13).
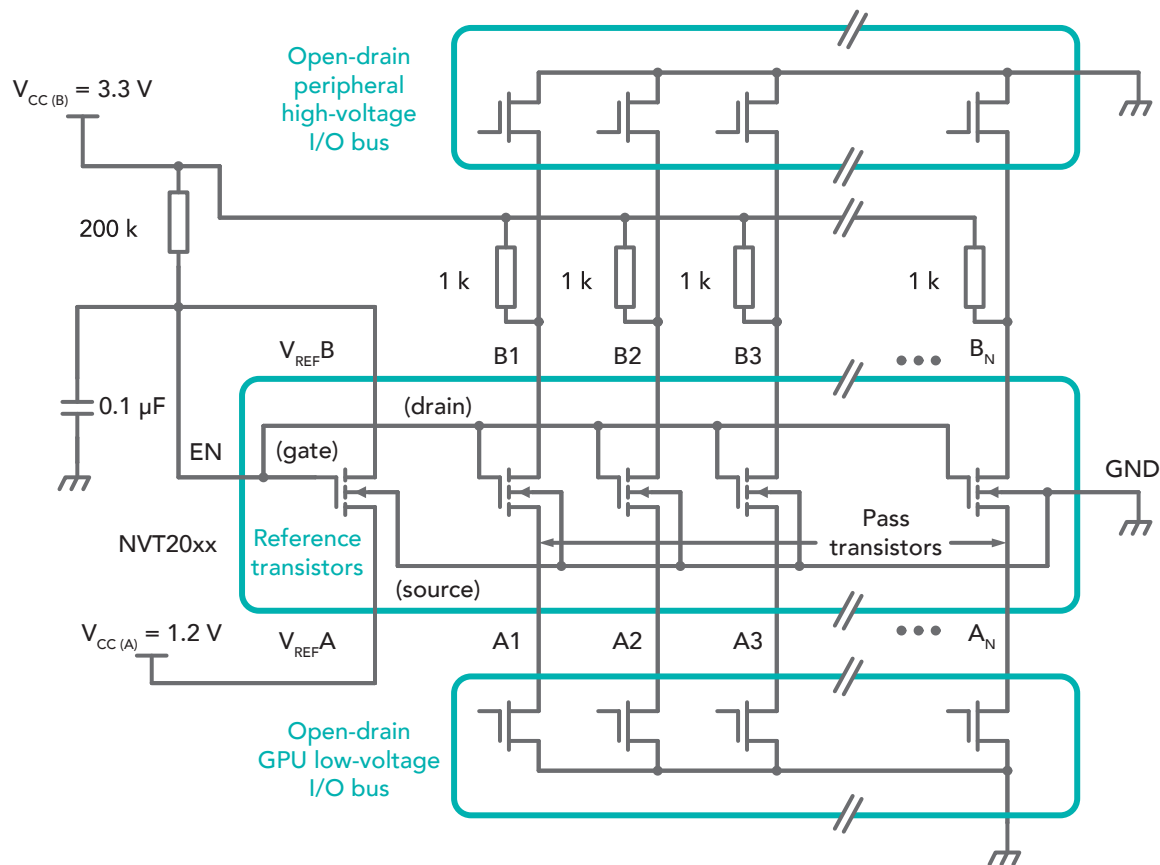

Figure 3-13. Typical NVT20xx device schematic

BASIC OPERATION

One of the Field-Effect Transistors (FETs) is used as a reference transistor, and the remainder as pass transistors. The low side (A1 to An) is the FET source, while the high side (B1 to Bn) is the FET drain. On the low side, the voltage of the reference transistor is the limit for the remaining pass transistors. The gate of the reference transistor should be tied to its drain to ensure that the FETs operate within the saturation region.

The reference transistor and one resistor are used to set V_{BIAS} and the gate voltage (VG) for all the pass transistors. The gate voltage is $V_{CC(A)}$ plus the gate-to-source voltage (V_{GS}). V_{GS} can vary from 0.6 to 1.0 V. The pass transistors on the low side are limited to $V_{CC(A)}$.

When either an An or Bn port is driven low, the FET is turned on and a low-resistance path exists between the An and Bn port. The low on-state resistance (R_{ON}) of the pass transistor allows connections to be made with minimal propagation delay.

Voltage translation: How to manage mixed-voltage designs using NXP level translators

When the Bn port is driven or pulled high, the voltage on the An port is limited to $V_{CC(A)}$. When the An port is driven or pulled high, the Bn port is pulled to $V_{CC(B)}$ by the pull-up resistors. $V_{CC(A)}$ is set equal to the I/O voltage level of the CPU and $V_{CC(B)}$ is set equal to the I/O voltage level of the peripheral device. This enables seamless translation between high and low levels without the need for directional control.

When EN is connected through a 200 kΩ pull-up resistor to a high-voltage $V_{CC(B)}$, and the An and Bn I/O are connected, the translator switch is on, allowing bidirectional data flow between ports. When EN is pulled low, the transistor switch is off and a high-impedance or disconnect state exists between ports. In this way, these translators protect new, lower-voltage devices from the overvoltage and ESD conditions applied by older, high-voltage devices, and make easy work of translating the V_{IH} and V_{OH} switching levels.

BIDIRECTIONAL LEVEL TRANSLATION WITH OPEN-DRAIN I/O

For bidirectional level translation, with open-drain the drivers on both sides of the translator either must be open-drain outputs or must be controlled to prevent contention between a high level on an output driver on one
side and a low level on the other.

Using an open-drain device means there have to be pull-up resistors on the B side, and the resistors have to be sized so as not to overload the output drivers.

With the NVT20xx, if $V_{CC(B)}$ minus $V_{CC(A)}$ is greater than 1 V, then pull-up resistors are not required on the A side. If, however, $V_{CC(B)}$ minus $V_{CC(A)}$ is less than 1 V, then pull-up resistors must be used on the A side to bring the An outputs to $V_{CC(A)}$. Note that if pull-up resistors are required on both the A and B sides, then the equivalent pull-up resistor value becomes the parallel combination of the two resistors when the pass transistor is on.

UNIDIRECTIONAL LEVEL TRANSLATION AND PUSH-PULL I/O

The translators support unidirectional level translation (low to high or high to low) with push-pull or totem-pole I/O, but the I/O must be the only driver on the bus during translation. Using this configuration for bidirectional push-pull control requires a direction control bit to determine which I/O is acting on the bus and prevent bus contention. Details for unidirectional translation are given in application note AN11127.
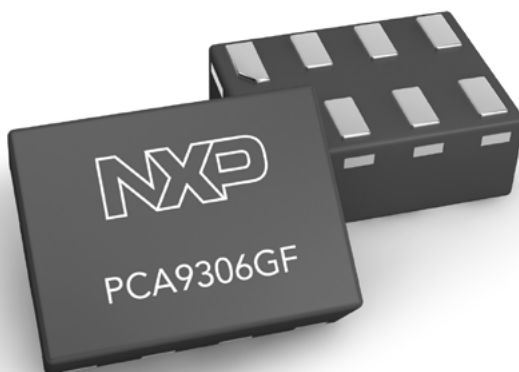
TABLE 3-4. SELECT NVT BIDIRECTIONAL TRANSLATORS

TYPE NUMBER	DESCRIPTION	$V_{CC(A)}$ (V)	$V_{CC(B)}$ (V)	NUMBER OF BITS	PACKAGE
NVT2001	1-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	1	XSON6
NVT2002*	2-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	2	TSSOP8, X2SON8
NVT2003	3-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	3	TSSOP10
NVT2006	6-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	6	DHVQFN16, HVQFN16, TSSOP16
NVT2008	8-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	8	DHVQFN20, TSSOP20
NVT2010	6-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	10	HVQFN24, TSSOP24

* The PCA9306 is the same as the NVT2002 but with more package options (SO8, VSSOP8, TSSOP8, XSON8 and XQFN8(U))
For the complete portfolio, visit nxp.com/VLT

APPLICATION-SPECIFIC LEVEL TRANSLATORS

This section discusses level translators that make it easier to work with SIM cards and special translators for the I²C-bus.

4.1 Translators for use with SIM cards

NVT4555 WLCSP BIDIRECTIONAL SIM CARD INTERFACE LEVEL TRANSLATOR AND SUPPLY VOLTAGE LDO

The NVT4555 interfaces between the host processor of a smartphone or any other equipment with cellular connection and its SIM card (Figure 4-1). Available in a tiny wafer-level chipscale package (WLCSP), it combines robust performance with the smallest available footprint. The device complies with the SIM power supply, includes EMI and ESD protection, and handles the shutdown sequence specified by the ISO 7816-3 specification.
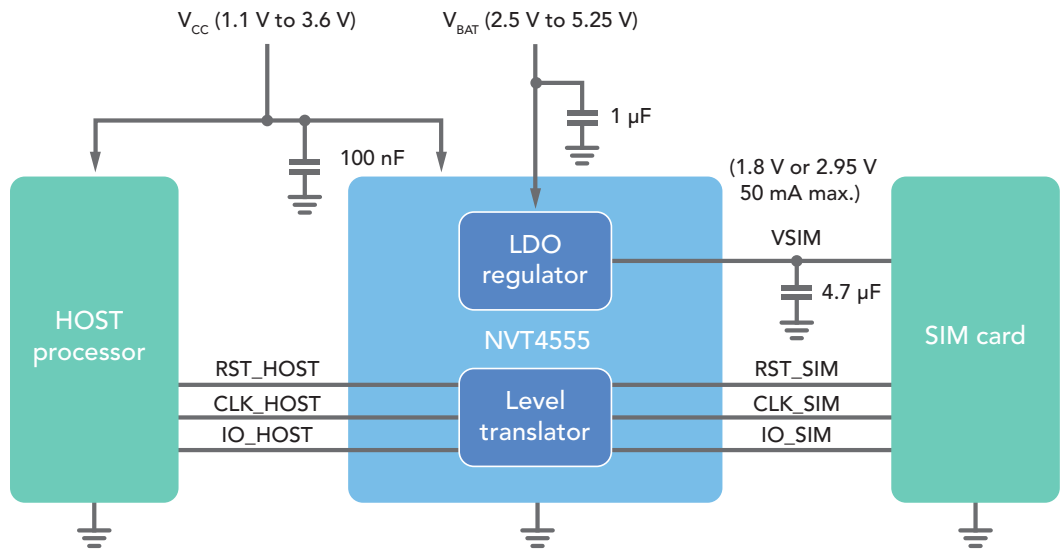

Figure 4-1. NVT4555 interfacing with a typical SIM card

The internal low-dropout (LDO) regulator supplies power to the SIM card using a high power supply rejection ratio (PSSR) at a very low dropout voltage (VBAT-VSIM). The NVT4555 provides two levels of fixed voltage regulation, at 1.8 or 2.95 V, selectable using the CTRL pin.

Using the ISO 7816-3 shutdown sequence for the SIM card signals ensures the card is properly disabled — and during hot swap, the shutdown sequence helps avoid data corruption and improper writes.

QUALCOMM REFERENCE DESIGN USES LEVEL TRANSLATORS WITH EXTERNAL LDO

NVT4557 and NVT4558 SIM Card
The reference design integrates the NVT4557HK and NVT4558HK, the 10-pin package SIM-card VLT with EN pin and not the 9-pin WLCSP package NVT4557UK (without EN pin). The EN pin meets the ISO standards related to the start-up / shut-down sequence between the host and SIM card. The final decision between 10-pin and 9-pin depends on the OEMs, trading off shut-down sequence with the smaller package size that has auto shut down based on VccB supply. The NVT4557HK is optimized for 1.8 V processor interface and the NVT4558 for 1.2 V with $0.65 \times V_{CCA}$ V_{IH} and $0.35 \times V_{CCA}$ V_{IL} HOST interface.

NVT4858 SD Card

The reference design uses the 16-pin package WLCSP package NVT4858UK because of its smaller size vs the lower price of the NVT4858HK (smaller die in plastic package). The final decision on package will depend on OEM, trading off board space vs component cost.
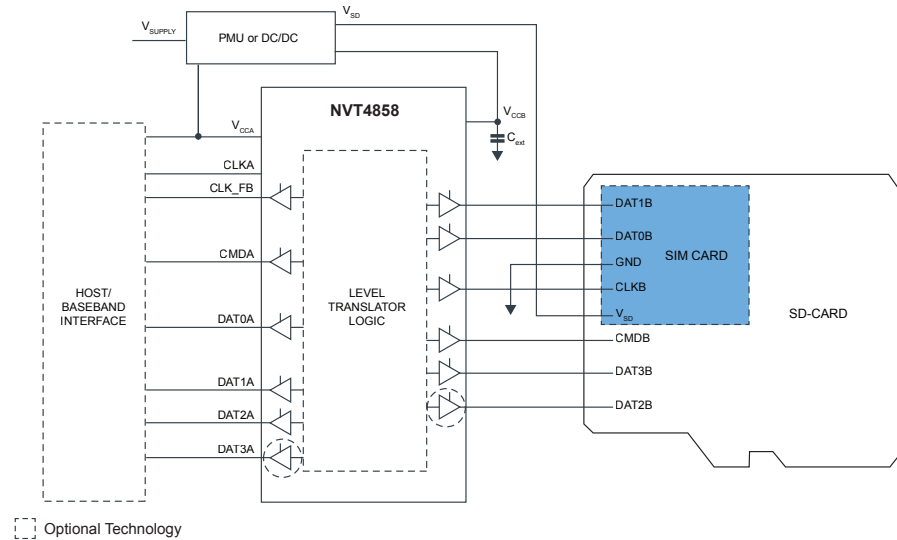
TARGET FUNCTION

Secure Digital (SD3.0) and SIM Voltage Level Translation CLASS B,C

END APPLICATION

Smartphones, Tablets, Digital Cameras, Wireless Modems

TYPICAL APPLICATION WITH EXTERNAL LDO

Optional Technology

SELECTION INFORMATION

EXTERNAL LDO

Application	Part Number	Package Option	HOST Voltage Range (V)	Card Voltage Range (V)	LDO Voltage Range (V)
SIM 1.8 V Host	NVT4557	WLCSP9 and XQFN10	1.08 to 1.98	1.62 to 3.6	NA
SIM 1.2 and 1.8 V Host	NVT4558	XQFN10	1.08 to 1.98	1.62 to 3.6	NA
SD and SIM	NVT4858	WLCSP16 and XQFN16	1.08 to 1.98	1.62 to 3.6	NA

INTERNAL LDO

Application	Part Number	Package Option	HOST Voltage Range (V)	Card Voltage Range (V)	LDO Voltage Range (V)
SIM	NVT4555	WLCSP12	1.1 to 3.6	1.8 or 2.95	2.5 to 5.25
SD and SIM	NVT4857	WLCSP20	1.1 to 2.0	1.8 or 3.0	2.9 to 3.6

ORDERING INFORMATION

Part Number	Package	Package Size (mm)	Package Pitch (mm)	Minimum Order Quantity	Orderable Part Number
NVT4555UK	WLCSP12	1.19 x 1.62 x 0.56	0.40	3000	NVT4555UKZ
NVT4557UK	WLCSP9	0.91 x 0.91 x 0.525	0.30	20000	NVT4557UKZ
NVT4557HK	XQFN10	1.4 x 1.8 x 0.5	0.40	4000	NVT4557HKX
NVT4558HK	XQFN10	1.4 x 1.8 x 0.5	0.40	4000	NVT4558HKX
NVT4857UK	WLCSP20	1.7 x 2.1 x 0.49	0.40	10000	NVT4857UKAZ
NVT4858UK	WLCSP16	2.6 x 1.8 x 0.5	0.35	3000	NVT4858UKZ
NVT4858HK	XQFN16	1.41 x 1.41 x 0.525	0.40	4000	NVT4858HKZ

All devices are shipped in 7" except NVT4557UK and NVT4857UK in 13" Tape and Reel with Pin 1 in Q1/T1

All devices are temperature range of T^{amb} = -40 °C to + 85 °C and ESD HBM 2 kV and Contact 8 kV

4.2 I²C muxes and switches that also perform bidirectional translation

PCA954X BIDIRECTIONAL TRANSLATING MUXES AND SWITCHES

Some specialized targets only have one I²C or SMBus address. When several identical targets are needed in the same system, targets can't be accessed individually. Multiplexers and switches split the I²C-bus into several branches and allow the I²C controller to select and address one of multiple identical targets without address conflicts up to 400 kHz.

Many I²C peripheral targets operate at different voltage levels due to the analog nature of the sensors. This would normally require a separate controller for each different power supply. Multiplexers and switches permit a single controller to interface with multiple peripheral targets that use different power supply voltages.

The PCA954x are I²C multiplexers and switches that also perform bidirectional translation (Figure 5-3).
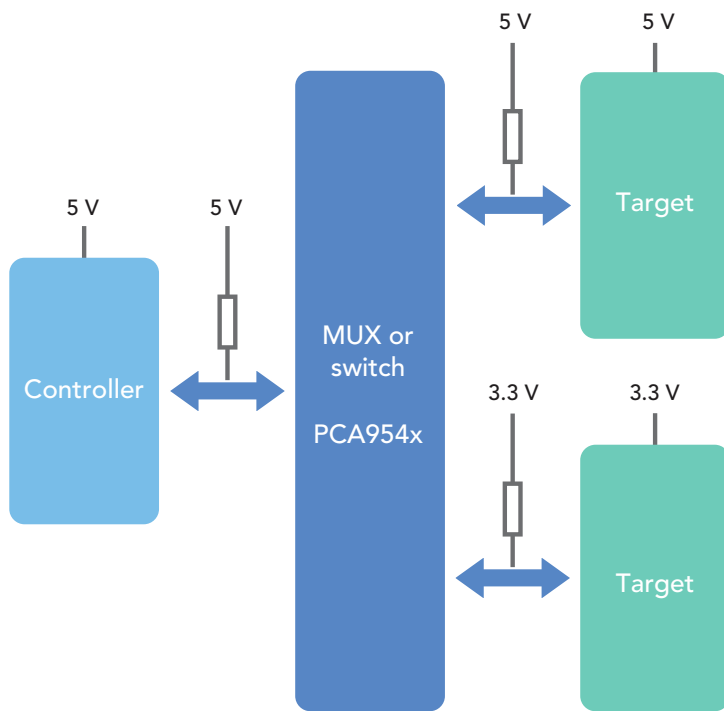
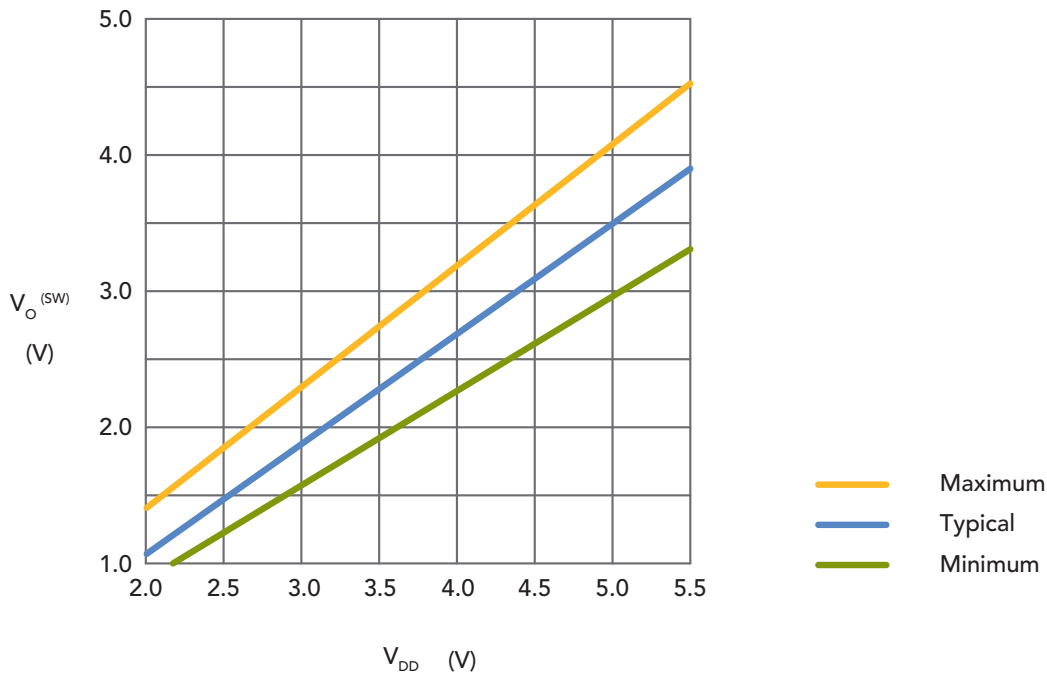Figure 5-3. Sample application using a PCA954x mux/switch

Figure 5-5. PCA954x voltage translation

For example, assume the upstream channel uses 5 V while the downstream channel uses 3.3 V. If the PCA954x is supplied with 3.3 V, it will clamp the voltage to about 2.3 V so the 5 V will not appear on the 3.3 V side. A pull-up resistor on the 3.3 V side then pulls it all the way up to the 3.3 V rail. In most situations, the design engineer should use the maximum voltage curve since this is the situation found over the entire temperature range. The important thing to note is that the multiplexer/switch should be supplied with the lowest I2C voltage needed to ensure proper level translation.

TABLE 4-1. PCA954X I²C MUXES AND SWITCHES

Type number	Function	Number of addresses	Hardware reset	Voltage range (V)	Package
PCA9540B	1:2 mux	1	No	2.3 to 5.5	SO8, TSSOP8
PCA9541	2:1 mux, controller selector	16	Yes	2.3 to 5.5	SO16, TSSOP16, HVQFN16
PCA9542A	1:2 mux	8	No	2.3 to 5.5	TSSOP14
PCA9543A	1:2 switch	4	Yes	2.3 to 5.5	SO14, TSSOP14
PCA9544A	1:4 mux	8	No	2.3 to 5.5	TSSOP20, HVQFN20
PCA9545	1:4 switch	4	Yes	2.3 to 5.5	SO20, TSSOP20, HVQFN20
PCA9546A	1:4 switch	8	Yes	2.3 to 5.5	SO16, TSSOP16, HVQFN16
PCA9547	1:8 mux	8	Yes	2.3 to 5.5	SO24, TSSOP24, HVQFN24
PCA9548A	1:8 switch	8	Yes	2.3 to 5.5	SO24, TSSOP24, HVQFN24
PCA9641	1 MHz 2:1 mux, controller selector	12	Yes	2.3 to 3.6	TSSOP16, HVQFN16

For the complete portfolio, visit www.nxp.com/MuxSwitch

PCA984X I²C BIDIRECTIONAL TRANSLATING MUXES AND SWITCHES

PCA984X Muxes and Switches operate in the same manner but allow 1 MHz bus operation, two address pins with supply/gnd/SCL/SDA as input for 16 possible addresses and have two supply pins to allow a larger voltage translation range

Type number	Function	Number of addresses	Hardware reset	Voltage range $V_{CC(A)}$	Voltage range $V_{CC(B)}$	Package
PCA9846	1:4 switch	16	Yes	0.8 to 3.6	1.65 to 3.6	TSSOP16
PCA9847	1:8 mux	16	Yes	0.8 to 3.6	1.65 to 3.6	TSSOP24
PCA9848	1:8 switch	16	No	0.8 to 3.6	1.65 to 3.6	TSSOP24, HVQFN24
PCA9849	1:4 mux	16	Yes	0.8 to 3.6	1.65 to 3.6	TSSOP16

For the complete portfolio, visit www.nxp.com/MuxSwitch