Advance Information

MCF5272PB/D
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MCF5272 Integrated
Microprocessor Product Brief

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This document provides an overview of the MCF5272 microprocessor features, including the major functional components.

1.1 Features

A block diagram of the MCF5272 is shown in Figure 1. The main features are as follows:

- Static Version 2 ColdFire variable-length RISC processor
  - 32-bit address and data path on-chip
  - 66-MHz processor core and bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Multiply-accumulate unit (MAC) for DSP and fast multiply operations
  - 63 Dhrystone 2.1 MIPS at 66 MHz
- On-chip memories
  - 4-Kbyte SRAM on CPU internal bus
  - 16-Kbyte ROM on CPU internal bus
  - 1-Kbyte instruction cache
- Power management
  - Fully-static operation with processor sleep and whole-chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
  - Software-controlled disable of external clock input for virtually zero power consumption (low-power stop mode)
- Two universal asynchronous/synchronous receiver transmitters (UARTs)
  - Full-duplex operation
  - Based on MC68681 dual-UART (DUART) programming model
  - Flexible baud rate generator
  - Modem control signals available ($\overline{\text{CTS}}$ and $\overline{\text{RTS}}$)
  - Processor interrupt and wake-up capability
  - Enhanced Tx, Rx FIFOs, 24 bytes each

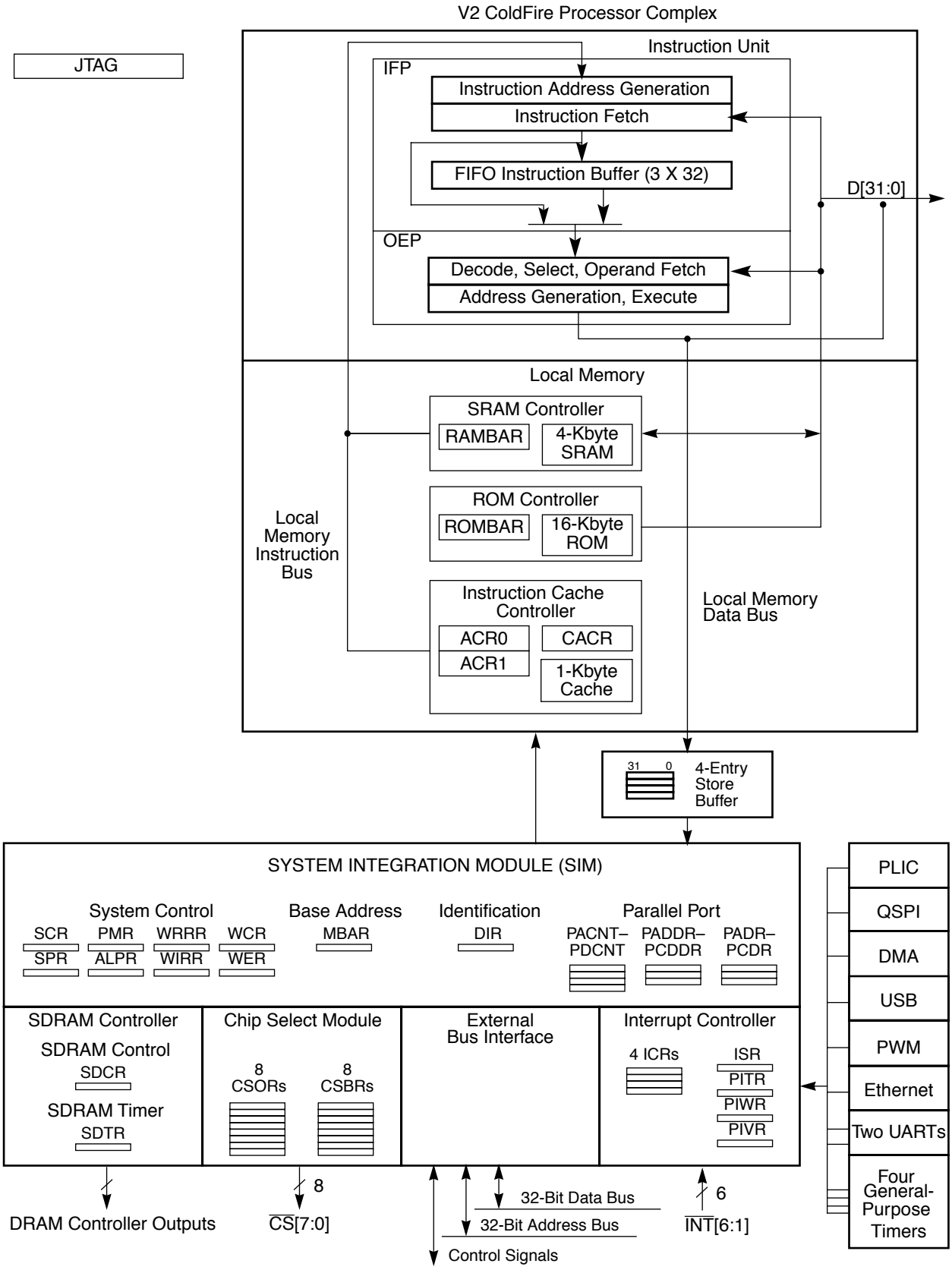

Figure 1. MCF5272 Block Diagram

- Ethernet Module
  - 10 baseT capability, half- or full-duplex
  - 100 baseT capability, half duplex and limited throughput full-duplex (MCF5272)
  - On-chip transmit and receive FIFOs
  - Off-chip flexible buffer descriptor rings
  - Media-independent interface (MII)
- Universal serial bus (USB) module
  - 12 Mbps (full-speed)
  - Fully compatible with USB 1.1 specifications
  - Eight endpoints (control, bulk, interrupt Rx, isochronous)
  - Endpoint FIFOs
  - Selectable on-chip analog interface
- External memory interface
  - External glueless 8, 16, and 32-bit SRAM and ROM interface bus
  - SDRAM controller supports 16–256 Mbit devices
  - External bus configurable for 16 or 32 bits width for SDRAM
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfer
  - Up to four chip selects available
  - Master operation
  - Programmable master bit rates
  - Up to 16 preprogrammed transfers
- Timer module
  - 4x16-bit general-purpose multi-mode timer
    - Input capture and output compare pins for timers 1 and 2
    - Programmable prescaler
  - 15-nS resolution at 66-MHz clock frequency
  - Software watchdog timer
  - Software watchdog can generate interrupt before reset
  - Processor interrupt for each timer
- Pulse width modulation (PWM) unit
  - Three identical channels
  - Independent prescaler TAP point
  - Period/duty range variable
- System integration module (SIM)
  - System configuration including internal and external address mapping
  - System protection by hardware watchdog

  - Versatile programmable chip select signals with wait state generation logic
  - Up to three 16-bit parallel input/output ports
  - Latchable interrupt inputs with programmable priority and edge triggering
  - Programmable interrupt vectors for on-chip peripherals
- Physical layer interface controller (PLIC)
  - Allows connection using general circuit interface (GCI) or interchip digital link (IDL) physical layer protocols for 2B + D data
  - Three physical interfaces
  - Four time-division multiplex (TDM) ports
- IEEE 1149.1 boundary-scan test access port (JTAG) for board-level testing
- Operating voltage: 3.3 V ±0.3 V
- Operating temperature: 0°–70°C
- Operating frequency: DC to 66 MHz, from external CMOS oscillator
- Compact ultra low-profile 196 ball-molded plastic ball-grid array package (PGBA)

1.2 MCF5272 Architecture

This section briefly describes the MCF5272 core, SIM, UART, and timer modules, and test access port.

1.2.1 Version 2 ColdFire Core

Based on the concept of variable-length RISC technology, ColdFire combines the simplicity of conventional 32-bit RISC architectures with a memory-saving, variable-length instruction set. The main features of the MCF5272 core are as follows:

- 32-bit address bus directly addresses up to 4 Gbytes of address space
- 32-bit data bus
- Variable-length RISC
- Optimized instruction set for high-level language constructs
- Sixteen general-purpose 32-bit data and address registers
- MAC unit for DSP applications
- Supervisor/user modes for system protection
- Vector base register to relocate exception-vector table
- Special core interfacing signals for integrated memories
- Full debug support

The Version 2 ColdFire core has a 32-bit address bus and a 32-bit data bus. The address bus allows direct addressing of up to 4 Gbytes. It supports misaligned data accesses and a bus arbitration unit for multiple bus masters.

The Version 2 ColdFire supports an enhanced subset of the 68000 instruction set. The MAC provides new instructions for DSP applications; otherwise, Version 2 ColdFire user code runs unchanged on 68020, 68030, 68040, and 68060 processors. The removed instructions include BCD, bit field, logical rotate,

decrement and branch, integer division, and integer multiply with a 64-bit result. Also, four indirect addressing modes have been eliminated.

The ColdFire 2 core incorporates a complete debug module that provides real-time trace, background debug mode, and real-time debug support.

1.2.2 System Integration Module (SIM)

The MCF5272 SIM provides the external bus interface for the ColdFire 2 architecture. It also eliminates most or all of the glue logic that typically supports the microprocessor and its interface with the peripheral and memory system. The SIM provides programmable circuits to perform address-decoding and chip selects, wait-state insertion, interrupt handling, clock generation, discrete I/O, and power management features.

1.2.2.1 External Bus Interface

The external bus interface (EBI) handles the transfer of information between the internal core and memory, peripherals, or other processing elements in the external address space.

1.2.2.2 Chip Select and Wait State Generation

Programmable chip select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select is general purpose; however, any one of the chip selects can be programmed to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

1.2.2.3 System Configuration and Protection

The SIM provides configuration registers that allow general system functions to be controlled and monitored. For example, all on-chip registers can be relocated as a block by programming a module base address, power management modes can be selected, and the source of the most recent RESET or BERR can be checked. The hardware watchdog features can be enabled or disabled, and the bus time-out period can be programmed.

A software watchdog timer is also provided for system protection. If programmed, the timer causes a reset to the MCF5272 if it is not refreshed periodically by software.

1.2.2.4 Power Management

The sleep and stop power management modes reduce power consumption by allowing software to shut down the core, peripherals, or the whole device during inactive periods. To reduce power consumption further, software can individually disable internal clocks to the on-chip peripheral modules. The power-saving modes are described as follows:

- Sleep mode uses interrupt control logic to allow any interrupt condition to wake the processor. As the MCF5272 is fully static, sleep mode is simply the disabling of the core's clock after the current instruction completes. An interrupt from any internal or external source causes on-chip power

management logic to reenable the core's clock; execution resumes with the next instruction. This allows rapid return from power-down state as compared to a dynamic implementation that must perform power-on reset processing before software can handle the interrupt request. If interrupts are enabled at the appropriate priority level, program control passes to the relevant interrupt service routine.

- Stop mode is entered by the disabling of the external clock input and is achieved by software setting a bit in a control register. Program execution stops after the current instruction. In stop mode, neither the core nor peripherals are active. The MCF5272 consumes very little power in this mode. To resume normal operation, the external interrupts cause the power management logic to re-enable the external clock input. The MCF5272 resumes program execution from where it entered stop mode (if no interrupt are pending), or starts interrupt exception processing if interrupts are pending.

1.2.2.5 Parallel Input/Output Ports

The MCF5272 has up to three 16-bit general-purpose parallel ports, each line of which can be programmed as either an input or output. Some port lines have dedicated pins and others are shared with other MCF5272 functions. Some outputs have high drive current capability.

1.2.2.6 Interrupt Inputs

The MCF5272 has flexible latched interrupt inputs each of which can generate a separate, maskable interrupt with programmable interrupt priority level and triggering edge (falling or rising). Each interrupt has its own interrupt vector.

1.2.3 UART Module

The MCF5272 has two full-duplex UART modules with an on-chip baud rate generator providing both standard and non-standard baud rates up to 5 Mbps. The module is functionally equivalent to the MC68681 DUART with enhanced features including 24-byte Tx and Rx FIFOs. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity and up to 2 stop bits in 1/16-bit increments. Receive and transmit FIFOs minimize CPU service calls. A wide variety of error detection and maskable interrupt capability is provided.

Using a programmable prescaler or an external source, the MCF5272 system clock supports various baud rates. Modem support is provided with request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines available externally. Full-duplex autoecho loopback, local loopback, and remote loopback modes can be selected.

The UART can be programmed to interrupt or wake-up the CPU on various normal or abnormal events. To reduce power consumption, the UART can be disabled by software if not in use.

1.2.4 Timer Module

The timer module contains five timers arranged in two submodules. One submodule contains a programmable software watchdog timer. The other contains four independent, identical general-purpose timer units, each containing a free-running 16-bit timer for use in various modes, including capturing the timer value with an external event, counting external events, or triggering an external signal or interrupting the CPU when the timer reaches a set value. Each unit has an 8-bit prescaler for deriving the clock input frequency from the system clock or external clock input. The output pin associated with each timer has programmable modes.

To reduce power consumption, the timer module can be disabled by software.

1.2.5 Test Access Port

For system diagnostics and manufacturing testing, the MCF5272 includes user-accessible test logic that complies with the IEEE 1149.1 standard for boundary scan testing, often referred to as JTAG (Joint Test Action Group). The IEEE 1149.1 Standard provides more information.

1.3 System Design

This section presents issues to consider when designing with the MCF5272. It describes differences between the MCF5272 (core and peripherals) and various other standard components that are replaced by moving to an integrated device like the MCF5272.

1.3.1 System Bus Configuration

The MCF5272 has flexibility in its system bus interfacing due to the dynamic bus sizing feature in which 32-,16-, and 8-bit data bus sizes are programmable on a per-chip select basis. The programmable nature of the strobe signals (including $\overline{OE}/\overline{RD}$, R/$\overline{W}$, $\overline{BS}$[3:0], and $\overline{CS}n$) should ensure that external decode logic is minimal or nonexistent. Configuration software is required upon power-on reset before chip-selected devices can be used, except for chip select 0 ($\overline{CS0}$), which is active after power-on reset until programmed otherwise. BUSW1 and BUSW0 select the initial data bus width for $\overline{CS0}$ only. A wake-up from sleep mode or a restart from stop mode does not require reconfiguration of the chip select registers or other system configuration registers.

1.4 MCF5272-Specific Features

This section describes features peculiar to the MCF5272.

1.4.1 Physical Layer Interface Controller (PLIC)

The physical layer interface controller (PLIC) allows the MCF5272 to connect at a physical level with external CODECs and other peripheral devices that use either the general circuit interface (GCI), or interchip digital link (IDL), physical layer protocols. This module is primarily intended to facilitate designs that include ISDN interfaces.

1.4.2 Pulse-Width Modulation (PWM) Unit

The PWM unit is intended for use in control applications. With a suitable low-pass filter, it can be used as a digital-to-analog converter. This module generates a synchronous series of pulses. The duty cycle of the pulses is under software control.

Its main features include the following:

- Double-buffered width register
- Variable-divide prescale
- Three identical, independent PWM modules
- Byte-wide width register provides programmable control of duty cycle.

The PWM implements a simple free-running counter with a width register and comparator such that the output is cleared when the counter exceeds the value of the width register. When the counter wraps around,

its value is not greater than the width register value, and the output is set high. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter.

1.4.3 Queued Serial Peripheral Interface (QSPI)

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfer RAMs in the QSPI are indirectly accessible using address and data registers. Functionality is similar to the QSPI portion of the QSM (queued serial module) implemented in the MC68332.

The QSPI has the following features:

- Programmable queue to support up to 16 transfers without user intervention
- Supports transfer sizes of 8 to 16 bits in 1-bit increments
- Four peripheral chip-select lines for control of up to 15 devices
- Baud rates from 129.4 Kbps to 33 Mbps at 66 MHz.
- Programmable delays before and after transfers
- Programmable clock phase and polarity
- Supports wrap-around mode for continuous transfers

1.4.4 Universal Serial Bus (USB) Module

The USB controller on the MCF5272 supports device mode data communications with a USB host (typically a PC). One host and up to 127 attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. The USB uses a tiered star topology with a hub at the center of each star. Each wire segment is a point-to-point connection between the host connector and a peripheral connector.

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