Signal Controllers

56F8355

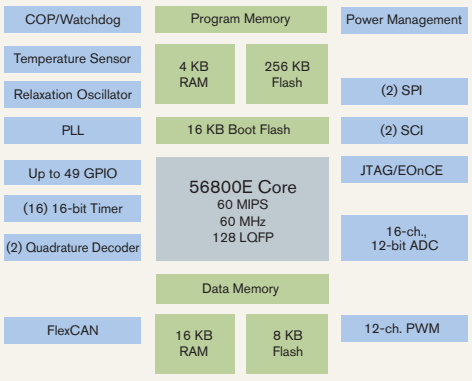
Target Applications

- > Automotive control
- > Industrial control/connectivity
- > Advanced motion control
- > Home appliances
- > General-purpose inverters
- > Smart relays
- > Fire and security systems
- > Power management
- > Medical monitoring
- > Multiphase inverters

Overview

Are features being added to your design as you get ready to begin production? Ever dream of the day you would have an easy solution for this dilemma? Dream no more!

The 56F8355 offers twice as much Program Flash, Data RAM and Boot Flash as the 56F8345, while providing full pin-for-pin compatibility. Doubling your applications memory has never been so easy! Continue to enjoy all the benefits of using a hybrid architecture and sophisticated peripherals with the additional memory you require to expand the capabilities of your product.



56800E Core Features	Benefits
> Up to 60 MIPS at 60 MHz execution frequency	> Hybrid architecture facilitates implementation of both control and signal processing functions in a single device
> DSP and microcontroller (MCU) functionality in a unified, C-efficient architecture	> High-performance, secured Flash memory helps eliminate the need for external storage devices
> JTAG/enhanced on-chip emulation (EOnCE™) for unobtrusive, real-time debugging	> Extended temperature range allows for operation of nonvolatile memory in harsh environments
> Four 36-bit accumulators	> Flash memory emulation of EEPROM helps eliminate the need for external nonvolatile memory
> 16- and 32-bit bidirectional barrel shifter	> 32-bit performance with 16-bit code density
> Parallel instruction set with unique addressing modes	> On-chip voltage regulator and power management help reduce overall system cost
> Hardware DO and REP loops available	> Diversity of peripheral configuration facilitates the elimination of external components, improving system integration and reliability
> Three internal address buses	> This device boots directly from Flash, providing additional application flexibility
> Four internal data buses	> High-performance pulse-width modulation (PWM) with programmable fault capability helps to simplify design and to promote compliance with safety regulations
> Architectural support for 8-, 16- and 32-bit single-cycle data fetches	> PWM and analog-to-digital converter (ADC) modules are tightly coupled to reduce processing overhead
> MCU-style software stack support	> Low-voltage interrupts (LVIs) help protect the system from brownout or power failure
> Controller-style addressing modes and instructions	> Simple in-application Flash memory programming via EOnCE or serial communication
> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)	
> Proven to deliver more control functionality with a smaller memory footprint than competing architectures	

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56F8355 Memory Features

> Architecture permits as many as three simultaneous accesses to program and data memory

> On-chip memory includes high-speed volatile and nonvolatile components:

- 280 KB On-chip Flash
  - 256 KB of Program Flash
  - 8 KB of Data Flash
  - 16 KB of Boot Flash
- 4 KB of Program RAM
- 16 KB of Data RAM

> Memories operate at 60 MHz (zero wait states) over temperature range (-40°C to +125°C) with no software tricks or hardware accelerators required

> Flash security feature prevents unauthorized accesses to its content

56F8355 Peripheral Circuit Features

> Two PWM modules with 12 outputs and eight programmable fault inputs

> Two serial peripheral interfaces (SPIs)

> Two serial communications interfaces (SCIs)

> I^2C communications master mode (emulated)

> Sixteen 16-bit timers with input and output compare capability

> Two four-input quadrature decoders

> FlexCAN module, 2.0 A/B compatible

> Temperature sense diode to monitor the on-chip temperature

> On-chip 3.3V to 2.6V voltage regulator

> Software-programmable Phase-Lock Loop (PLL)

> On-chip relaxation oscillator

> 12-bit ADCs with 16 inputs, self-calibration and current injection capability

> Up to 49 general-purpose input/output (GPIO) pins

> External reset input pin for hardware reset

> Computer operating properly (COP)

> Integrated power-on reset and LVI module

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

56F8300 Peripheral User Manual	Detailed peripheral descriptions of the 56F8300 family of devices ***Order Number:*** MC56F8300UM
56F8355/56F8155 Technical Data Sheet	Electrical and timing specifications, pin descriptions and package descriptions ***Order Number:*** MC56F8355
56F8355 Product Brief	Summary description and block diagram of the 56F8355 core, memory, peripherals and interfaces ***Order Number:*** MC56F8355PB
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit core processor and the instruction set ***Order Number:*** DSP56800ERM

Ordering Information

Part	MC56F8355
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	128
Temperature Range	-40°C to +105°C
Order Number	MC56F8355VFG60

Part	MC56F8355
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	128
Temperature Range	-40°C to +125°C
Order Number	MC56F8355MFG60

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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