

QUICC Engine Microcode Errata

This document describes all known QUICC Engine microcode errata for microcode package versions released in the General Release 3.1 (January 2009) and subsequent releases. For a description of each package and the devices for which the packages apply, please refer to the specific package release notes.

[Table 1](#) provides a revision history for this document.

Table 1. Document Revision History

Revision	Date	Significant Changes
4	Jan 22, 2010	<ul style="list-style-type: none"> • Added PPIW1, HC1, IPSec1, POS1, POS2, IWF5, IWF6, ETHBT1, ETH4, and AE TypeB 2.1.1 to ATM2 • In Table 2, added HC, IPSEC1, and POS. • In Table 3 <ul style="list-style-type: none"> – Changed package version of TypeF and TypeC to “all versions” for errata ATM6. – Changed package version of TypeC to “all versions” for errata IWF3, IWF4. – Changed package version of TypeC from 1.4.0 to 1.4.1 for errata MCC4.
3	Dec 1, 2009	<ul style="list-style-type: none"> • Added ETHIW5, MCC3 and MCC4. • In Table 3 <ul style="list-style-type: none"> – Changed package version from “E2E Type D 1.0.0” to “E2E Type D 1.1.0” for the all the relevant errata. – Changed microcode package column for ETHIW4 and ATM1.
2	Oct 28, 2009	<ul style="list-style-type: none"> • Added ATM7, ATMIW2, ETHIW4, HM4, MCC2 • In Table 3, added EE POS microcode package • In Table 3, changed package version to “all versions” for E2E Type D for the errata: IWF2, IWF3, IWF4
1.1	Oct 2009	<ul style="list-style-type: none"> • Added PE TypeI microcode package to applicable errata in summary table • Removed AET TypeF 0.0.0, AE TypeG all versions from errata IWF3
1	Sept 2009	<ul style="list-style-type: none"> • Initial release

Table 3 summarizes the errata and lists the corresponding microcode package with revision numbers as applicable. The erratas are categorized according to the general features. Table 2 lists the category IDs and their meaning.

Table 2. Errata Categories

ID	Description
ATM	ATM
ATMIW	ATM Interworking
ETH	Ethernet
ETHBT	Ethernet Burst Tolerance
ETHIW	Ethernet Interworking
HC	Header Compression
HM	Header Manipulation
IPSec	IPSec
IWF	Interworking Function
MCC	MCC
POS	POS MPHY/SPHY
PPP	PPP
PPPIW	PPP Interworking
QMC	QMC
VP	Virtual Port

Unless otherwise stated, the errata apply to the indicated revision number and all older revisions. The errata is fixed in the revision following the indicated revision number and all newer revisions. Packages that are not listed are not affected by the errata.

Table 3. Summary of QUICC Engine Microcode Errata

Errata	Description	Microcode Package
ATM1	IMA microcode event queue allocation.	AET TypeF all versions AE TypeB all versions AE TypeG all versions PAE TypeC all versions
ATM2	AAL2 Timer CU mode channel deletion for last cell.	AET TypeF all versions PAE TypeC all versions AE TypeB 2.1.1
ATM3	Cell duplication when using AAL2 with Switch WFQ.	AET TypeF all versions AE TypeB all versions AE TypeG all versions PAE TypeC all versions
ATM4	Wrong VBR contract calculation in APC scheduler of IMA system.	AE TypeB all versions

Table 3. Summary of QUICC Engine Microcode Errata (continued)

Errata	Description	Microcode Package
ATM5	Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command.	AET TypeF 0.0.0 AE TypeB 2.3.0 AE TypeG 0.0.0 PAE TypeC 1.4.0
ATM6	For APC flux compensation mode half of the time the TX will not transmit any ATM cells.	AET TypeF all versions AE TypeB all versions AE TypeG all versions PAE TypeC all versions
ATM7	AAL5 Auto-VC-Off with GBR may abort legal frames.	AET TypeF all versions AE TypeB 2.4.0 AE TypeG 0.0.1 PAE TypeC all versions 8569 IRAM v166
ATMIW1	ATM IW threads/buffer pool might be stuck under heavy traffic.	AE TypeB 2.3.0 AE TypeG 0.0.0
ATMIW2	AAL5 frame based with GBR IW AVCON/AVCF might not work.	AE TypeB 2.4.0 AE TypeG 0.0.1 8569 IRAM v166
ETH1	Ethernet transmitter scheduler on-the-fly rate changes.	PE TypeE All versions PE TypeB All versions PE TypeI All versions
ETH2	Ethernet transmitter scheduler rate limiting inaccuracy.	PE TypeE All versions PE TypeB All versions PE TypeI All versions
ETH3	Changing the rate limiter dynamically may cause the Ethernet transmitter to pause.	PE TypeE All versions PE TypeB All versions PE TypeI All versions
ETHBT1	BD ring of VP may be corrupted when it is used in Burst Tolerance setup.	8569 IRAM v169 (Burst Tolerance does not exist in earlier versions)
ETHIW1	Possible SDMA error and/or cache coherency problem for Tx when an enqueue busy or FBP busy condition is encountered.	EE TypeD 1.1.0 AE TypeB 2.3.0 PE TypeA 2.5.1 PE TypeB 2.8.1 PE TypeE 0.0.3 AE TypeG 0.0.0
ETHIW2	Possible SDMA error and/or cache coherency problem for Tx BD with length equal to zero.	EE TypeD 1.1.0 AE TypeB 2.3.0 PE TypeA 2.5.1 PE TypeB 2.8.1 PE TypeE 0.0.3 AE TypeG 0.0.0 PE TypeI 0.0.0

Table 3. Summary of QUICC Engine Microcode Errata (continued)

Errata	Description	Microcode Package
ETHIW3	Policer and PW codes are not invoked when CPU busy condition happened for Copy2CPU frames.	EE TypeD 1.1.0 AE TypeB 2.4.0 AE TypeG 0.0.1 PE TypeA 2.5.1 PE TypeB 2.8.1 PE TypeE 0.0.3 AET TypeF 0.0.0 8569 IRAM v166
ETHIW4	Interworking connection statistics TCI counters are not working correctly.	EE TypeD 1.1.0 AE TypeB 2.4.0 AE TypeG 0.0.1 PAE TypeC all versions PE TypeA all versions PE TypeB 2.8.1 PE TypeE 0.0.3 PE TypeI 0.0.0 AET TypeF all versions EE POS 0.0.0 8569 IRAM v166
ETHIW5	Ethernet Short frames (length<MINFLR) cannot be interworked.	PE TypeA 2.5.1
HC1	HC Generation Violation is not supported.	8569 IRAM v169 PE TypeA 2.5.1 PE TypeB 2.8.1 EE TypeD 1.1.0 PE TypeI 0.0.0
HM1	External Header Insert HMCD failure.	EE TypeD 1.1.0 AE TypeB all versions AE TypeG all versions
HM2	Header Removal followed by External Header Replace HMCD.	EE TypeD 1.1.0 AE TypeB all versions AE TypeG all versions
HM3	Header Insert HMCD with dynamic length insertion.	EE TypeD 1.1.0 AE TypeB all versions AE TypeG all versions
HM4	Header Insert HMCD using dynamic length insertion mode and a non zero insertion offset.	All IW versions 8569 IRAM all versions
IPSec1	IPSec synchronization bug + major changes in the interrupts structure	8569 IRAM v169
IWF1	PPP and Ethernet receivers cannot interwork to the same Ethernet TX queue.	PE TypeE 0.0.3 PE TypeI 0.0.0
IWF2	CAM emulation lookup host command.	EE TypeD all versions EE POS all versions AE TypeB all versions AE TypeG all versions

Table 3. Summary of QUICC Engine Microcode Errata (continued)

Errata	Description	Microcode Package
IWF3	Possible SDMA error and/or cache coherency problem while using aging mechanism on external hash tables.	AE TypeB all versions EE TypeD all versions EE POS all versions PAE TypeC all versions
IWF4	Possible SDMA error and/or cache coherency problem when using external indexed lookup table.	EE TypeD all versions EE POS all versions AE TypeB all versions PE TypeA 2.5.1 PE TypeB 2.8.1 PE TypeE 0.0.3 AE TypeG all versions PAE TypeC all versions PE TypeI 0.0.0
IWF5	Add/Remove and Remove commands for External 8-Ways Hash can induce the removal of a valid entry.	8569 IRAM v169
IWF6	noDHCP expect flag in GenerateLookupKey_IP PCD is not working correctly.	8569 IRAM v169
MCC1	CSP mixed mode (both standard and extended CSP used in the same time) not working.	PAE TypeC 1.4.0 ESS7 256 2.0.0
MCC2	Reset SU fil host command (MCC SS7) is not functional in MPC8569 device.	8569 IRAM v166
MCC3	OCT and SUERM/EIM interrupts may not be issued in certain cases.	PAE Type C 1.4.0 8569 IRAM v166
MCC4	HDLC ABORT character not detected by the HDLC framer in certain cases.	PAE Type C 1.4.1 8569 IRAM v169 8569Rev2_IRAM_1.0.0
POS1	Miss ordering between ACK1 and ACK2 in POS TX IDLE/TBNR flow.	EE POS 0.0.0 POS 0.0.4 8569 IRAM v169
POS2	The Protocol Error bit (PRE) is not signaled in the RxBD.	EE POS 0.0.0 POS 0.0.4 8569 IRAM v169
PPP1	ML/MC PPP transmitter Weighted Fair Queueing—Mixed Mode.	PE TypeB 2.8.1
PPPIW1	Possible SDMA error when using PPP IW to CPU.	8569 IRAM v169 PE TypeA 2.6.0 PE TypeB 2.8.1 PE TypeE 0.0.3 PE TypeI 0.0.0
QMC1	QMC Stop Receive command.	8569 IRAM v165
VP1	General Timer always triggered when in Virtual Port Polling mode.	EE TypeD 1.1.0 EE POS 0.0.0 AE TypeB all versions AE TypeG all versions PE TypeE 0.0.3 PE TypeI 0.0.0
VP2	Possible SDMA error and/or cache coherency problem when using the Virtual Port Fast Swap Queue operation mode.	EE TypeD 1.1.0

ATM1 **IMA microcode event queue allocation.****Description and Impact on Functionality:**

Placing the IMA microcode event queue in a cacheable memory area does not work.

Reference Manual:

QEIWRM, Rev 3, Section 27.4.7 “IMA Events”

Work Arounds:

Place the IMA microcode event queue in a non-cacheable memory area.

ATM2**AAL2 Timer CU mode channel deletion for last cell.****Description and Impact on Functionality:**

When AAL2 Timer CU mode is enabled and TCT[AVCF] mode is set, the channel may be deleted from the APC table even though the cell is partially full.

Reference Manual:

QEIWRM, Rev 3, Chapter 12, “ATM Adaptation Layer 2 (AAL2)”

Work Arounds:

None

ATM3**Cell duplication when using AAL2 with Switch WFQ.****Description and Impact on Functionality:**

When using AAL2 with Switch WFQ mode and IMA enabled and overload limit feature enabled, there can be cell duplication.

Reference Manual:

QEIWRM, Rev 3, Chapter 12, “ATM Adaptation Layer 2 (AAL2)”

Work Arounds:

None

ATM4**Wrong VBR contract calculation in APC scheduler of IMA system.****Description and Impact on Functionality:**

In an IMA system that uses the APC scheduler, the VBR contract calculation is wrong when the number of active IMA links in the IMA group is more than 1 link. As a result, ATM shaping will not enforce the VBR contract as described in ATM standard.

Reference Manual:

QEIWRM, Rev 3, Section 27.4.8, “APC Programming for IMA”

Work Arounds:

None

ATM5**Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command.****Description and Impact on Functionality:**

Possible Channel loss for ATM APC scheduler when issuing ATM transmit Host Command.

Reference Manual:

QEIWRM, Rev 3, Section 11.4.1.1, “ATM Transmit Command”

Work Arounds:

Use alternative ATM scheduler such as GCRA.

Use Auto AVCON/AVCOFF mechanism (for example for IW).

ATM6

For APC flux compensation mode half of the time the TX will not transmit any ATM cells.

Description and Impact on Functionality:

In APC flux compensation mode half of the time the TX will not transmit any ATM cells.

Reference Manual:

QEIWRM, Rev 3, Section 11.2.8, “APC Flux Compensation”

Work Arounds:

None

ATM7**AAL5 Auto-VC-Off with GBR may abort legal frames.****Description and Impact on Functionality:**

AAL5 Auto-VC-Off with GBR may abort legal frames.

Reference Manual:

QEIWRM, Rev 3, Section 11.3.5.4, “GBR Programming Model”

Work Arounds:

None

ATMIW1 **ATM IW threads/buffer pool might be stuck under heavy traffic.****Description and Impact on Functionality:**

ATM AAL5/AAL2 Interworking Rx Thread management and synchronization mechanism might fail under heavy traffic load conditions. This can lead to MURAM corruption, packet loss, loss of buffers from the buffer pool and/or thread halt

Reference Manual:

QEIWRM, Rev 3, Table 11-21, “Common MTH Parameters Table”

Work Arounds:

None

ATMIW2 **AAL5 frame based with GBR IW AVCON/AVCF might not work.****Description and Impact on Functionality:**

When working in AAL5 frame-based with V-TCT in GBR type and IW AVCON/AVCF mode, then frame may be not transmitted (MPC8360) or frames could be corrupted (MPC8569).

Reference Manual:

QEIWRM, Rev 3, Section 11.3.5.4, “GBR Programming Model”

Work Arounds:

None

ETH1**Ethernet transmitter scheduler on-the-fly rate changes.****Description and Impact on Functionality:**

The Ethernet transmitter scheduler may get stuck when changing rates on the fly.

Reference Manual:

QEIWRM, Rev 3, Section 8.4.16, “Ethernet Scheduler Theory of Operation”

Work Arounds:

None

ETH2 **Ethernet transmitter scheduler rate limiting inaccuracy.****Description and Impact on Functionality:**

There is a rate limiting inaccuracy when FCS and/or padding is added by the Ethernet Transmitter.

Reference Manual:

QEIWRM, Rev 3, Section 8.5.1.5, "MAC Configuration 2 Register (MACCFG2)"

Work Arounuds:

Set PAD/CRC and CRE bits in MAC Configuration 2 Register (MACCFG2) to zero.

ETH3

Changing the rate limiter dynamically may cause the Ethernet transmitter to pause.

Description and Impact on Functionality:

Changing the rate limiter dynamically may cause the Ethernet Transmitter to pause.

Reference Manual:

QEIWRM, Rev 3, Section 8.4.16.1.5, “Rate Limiting”

Work Arounds:

None

ETHBT1 **BD ring of VP may be corrupted when it is used in Burst Tolerance setup****Description and Impact on Functionality:**

The bug occurs when all the following conditions are met:

- Burst Tolerance setup
- Frame which requires multiple BDs in VP queue is received
- Some of the BDs of the frame were sent to VP queue.
- Last BD which was used for the frame has wrap bit set
- Busy condition occurs for subsequent BD of the same frame

In the above scenario the Ethernet controller should indicate to VP to drop the partial frame (BDs, which were already sent to VP) silently.

Due to a bug the wrap bit in the last BD is corrupted (cleared) and thus the whole BD ring structure is corrupted.

Reference Manual:

QEIWRM, Rev 3, Section 8.7 “Burst Tolerance Mode”.

Work Arounds:

The bug can be worked around by using only single BD when working in Burst Tolerance mode. Alternatively the user can avoid using Burst Tolerance mode (use regular Ethernet instead).

ETHIW1 **Possible SDMA error and/or cache coherency problem for Tx when an enqueue busy or FBP busy condition is encountered.**

Description and Impact on Functionality:

When enqueue busy or FBP busy conditions are encountered on destination Tx protocol and appropriate interrupts are unmasked, an SDMA and/or cache coherency problem may occur.

Reference Manual:

QEIWRM, Rev 3 Sections:

31.1.15.4.4, “Interworking Interrupt Queue Entry for Enqueue Busy Error for Ethernet and ATM”

31.1.15.4.5, “Interworking Interrupt Queue Entry for Free Buffer Pool (FBP) Busy Error for Ethernet and ATM”

Work Arounds:

Disable Enqueue Busy and FBP Busy interworking interrupts by negating bits 24 and 27 in IWMODER register described in QEIWRM, Rev 3 Section 31.1.1.1, “Interworking Mode Register (IWMODER).”

ETHIW2 Possible SDMA error and/or cache coherency problem for Tx BD with length equal to zero.

Description and Impact on Functionality:

Possible SDMA error and/or cache coherency problem for Tx BD with length equal to zero. BD with length equal to zero can occur if a Trailer Removal HMCD is applied to a frame for which the removed portion alone is contained within the last BD.

Reference Manual:

QEIWRM, Rev 3, Part IV, “Multiprotocol Interworking”

Work Arounds:

None

ETHIW3 **Policer and PW codes are not invoked when CPU busy condition happened for Copy2CPU frames.**

Description and Impact on Functionality:

Policer and PW codes are not invoked when CPU busy condition happened for Copy2CPU frames. Therefore, the Policer and PW codes can be skipped by mistake.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.3.3 “InterWorking Action Descriptor (IWAD)” and Section 29.2.6.1.4 “Policer Functional Description”

Work Arounds:

Do not use Copy2CPU mode together with Policer and/or PW.

ETHIW4 Interworking connection statistics TCI counters are not working correctly.

Description and Impact on Functionality:

The Interworking Statistics Counters (IWCS) TCI1 and TCI2 counters can have an erroneous values.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.14.2 “InterWorking Connection Statistics Table (IWCS)”.

Work Arounuds:

Do not use the TCI1 and TCI2 counters.

ETHIW5 Ethernet Short frames (length<MINFLR) cannot be interworked**Description and Impact on Functionality:**

If the interworking (IW) function is enabled (REMODR[IWEn==1]), RSH (receive short frames) is not functional. (RSH has to be set to zero).

Reference Manual:

QEIWRM, Rev 3, Section 8.5.1.1 “UCC Protocol Specific Ethernet Mode Register (UPSMR)”.

Work Arounds:

Use discard short frames (UPSMR[RSH]==0) in IW mode (REMODR[IWEn==1]).

HC1 **HC Generation Violation is not supported****Description and Impact on Functionality:**

Header Compression generation violation is not supported.

Reference Manual:

QEIWRM, Rev 3, Section 32.5.2, “Queue Operation Modes”

Work Arounds:

None.

HMI1 External Header Insert HMCD failure.**Description and Impact on Functionality:**

The External Header Insert HMCD command may fail if inserting data (not just length) to an offset greater than 0.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.11, “Header Manipulation Command Descriptors (HMCDs)”

Work Arounuds:

Use Internal Header Insert or Local Header Insert HMCD.

HM2 Header Removal followed by External Header Replace HMCD.**Description and Impact on Functionality:**

Header Removal with a non-zero offset which is followed by External Header Replace/Insert may cause data corruption.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.11, “Header Manipulation Command Descriptors (HMCDs)”

Work Arounds:

None

HM3 Header Insert HMCD with dynamic length insertion.**Description and Impact on Functionality:**

Local Header Insert HMCD and Internal Header Insert HMCD which use an internal IWCT and perform a dynamic length insertion when working with more than one Rx thread will cause the inserted frame length value to be corrupted.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.11, “Header Manipulation Command Descriptors (HMCDs)”

Work Arounds:

Use External Header Insert HMCD or use Local Header Insert with an external IWCT.

HM4 **Header Insert HMCD using dynamic length insertion mode and a non zero insertion offset.**

Description and Impact on Functionality:

When using Header Insert HMCD, which performs a dynamic length insertion and uses a non zero insertion offset, the insertion offset will not be subtracted from the calculated length.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.11, “Header Manipulation Command Descriptors (HMCDs)”

Work Arounds:

Use the dynamic length with zero insertion offset.

IPSec1 **IPSec synchronization bug + major changes in the interrupts structure****Description and Impact on Functionality:**

IPSec synchronization bug was found + major changes in the interrupts structure were made

Reference Manual:

IPsec_ - __Bump_in_the_Wire”

Work Arounds:

IPSec is not supported

IWF1**PPP and Ethernet receivers cannot interwork to the same Ethernet TX queue.****Description and Impact on Functionality:**

PPP and Ethernet receivers cannot interwork to the same Ethernet TX queue.

Reference Manual:

QEIWRM, Rev 3, Section 31.1.3.3.3, “Transmit Queue Descriptor Index (TQD Index)”, “TQD Index for Unicast Ethernet Destination Queue”

Work Arounuds:

PPP and Ethernet receivers interworking flows should be programmed to enqueue to different Ethernet transmitter queues.

IWF2 **CAM emulation lookup host command.****Description and Impact on Functionality:**

When issuing a host command "Add/Remove Entry in CAM Emulation Lookup Table" with ADDE equal to 00 (table lookup, no change in the table), the LookupTableOffset value might be invalid even though the V bit (valid LookupTableOffset) is asserted.

Reference Manual:

QEIWRM, Rev 3, Section 30.6.1.2, "Add/Remove Entry in CAM Emulation Lookup Table"

Work Arounds:

In case the V bit is asserted on the returned LookupTableOffset, the user should read the first byte of the Action Descriptor (AD) which is pointed to by the LookupTableOffset and verify that the V (valid) bit on the AD is asserted. In case the V (valid) bit on the AD is negated, the table lookup result should be considered as invalid, i.e. no entry was found.

IWF3 **Possible SDMA error and/or cache coherency problem while using aging mechanism on external hash tables.**

Description and Impact on Functionality:

Using aging mechanism on external hash tables might introduce a SDMA error and/or a cache coherency problem.

Reference Manual:

QEIWRM, Rev 3 Sections:

30.5.4, “Aging and Automatic Learning”

30.5.3.3.1, “TableLookup_FourWayHash PCD”

30.5.3.3.2, “TableLookup_EightWayHash PCD”

Work Arounds:

None

IWF4 **Possible SDMA error and/or cache coherency problem when using external indexed lookup table.**

Description and Impact on Functionality:

Possible SDMA error and/or cache coherency problem when using external indexed lookup table.

Reference Manual:

QEIWRM, Rev 3, Section 30.5.3.2, “TableLookup_Indexed PCD”

Work ArounDs:

Method 1:

Do not use external indexed lookup table PCD.

Method 2:

When using external indexed lookup table PCD, use only the primary bus and set the BMR to 0x1 to get BMR[GBL]=0 or to 0x3 to get BMT[GBL]=1. Secondary bus can be used in case the dynamic bus selection is enabled in QUICC Engine block's DMA, as described in the QEIWRM, Rev 3, Section 3.1.6, “Bus Selection Mechanisms.”

IWF5

Add/Remove and Remove commands for External 8-Ways Hash can induce the removal of a valid entry.

Description and Impact on Functionality:

Add/Remove and Remove commands for External 8-Ways Hash can induce the removal of a valid entry.

Reference Manual:

QEIWRM, Rev 3, Section 30.5.3.3 “Hash Table Lookup PCDs”

Work Arounds:

Use 4-ways Hash or internal 8 ways-Hash

Interworking Function

IWF6 **noDHCP expect flag in GenerateLookupKey_IP PCD is not working correctly.**

Description and Impact on Functionality:

The noDHCP expect flag in GenerateLookupKey_IP PCD not to work correctly.

Reference Manual:

QEIWRM, Rev 3, Section 30.5.2.6 “GenerateLookupKey_IP PCD”

Work Arounds:

Do not use noDHCP flag in GenerateLookupKey_IP PCD.

MCC1

CSP mixed mode (both standard and extended CSP used in the same time) not working.

Description and Impact on Functionality:

When using both CSP tables (standard and extended), MCPBASE gets corrupted in MCCTSTOP, MCCRSTOP and Reset_Su_Fil host commands for channels using the standard CSP table.

This may cause corruption of CSP table and GUN/GOV events.

Reference Manual:

QEIWRM, Rev 3, Section 22.2.1, “Global MCC Parameters”

Work Arounuds:

Do not use CSP mixed mode. Allocate all channels in only one of the CSP tables (standard or extended).

MCC2 **Reset SU fil host command (MCC SS7) is not functional in MPC8569 device.****Description and Impact on Functionality:**

Reset SU fil host command (is used for MCC SS7) is not functional in MPC8569 device.

Reference Manual:

QEIWRM, Rev 3, Section 22.2.2.4.15, “Resetting the SU Filtering Mechanism”

Work Arounuds:

None

MCC3 **OCT and SUERM/EIM interrupts may not be issued in certain cases.****Description and Impact on Functionality:**

OCM (octet counting mode) is left incorrectly based on IDLE / NON-IDLE line state transition. Due to this, OCT (and thus also SUERM/EIM) interrupts are not issued for certain data patterns.

Reference Manual:

QEIWRM, Rev 3, Section 22.2.2.4.16, “Octet Counting Mode - SS7 Mode”

Work Arounds:

None

MCC4 **HDLC ABORT character not detected by the HDLC framer in certain cases.****Description and Impact on Functionality:**

HDLC ABORT character is not detected for certain data patterns. Loss of flag is not detected in these cases and thus OCM is not entered or current interval is not marked as errored.

Reference Manual:

QEIWRM, Rev 3, Section 22.1.3.2, “HDLC”

Work Arounds:

None

POS1 **Miss ordering between ACK1 and ACK2 in POS TX IDLE/TBNR flow.****Description and Impact on Functionality:**

In case that more then one Risc or in case that different Riscs associated to POS TX distributor and POS TX terminator tasks, UCC TX port may stuck and no new requests will be served (TX port stop transmit).

Reference Manual:

QEIWRM, Rev 3, Chapter 13 “UCC POS Controller (UPOS)”

Work Arounds:

None

POS2 **The Protocol Error bit (PRE) is not signaled in the RxBD.****Description and Impact on Functionality:**

The global error bit in the Rx attribute is not set if the Protocol Error bit is set. As a result The Protocol Error bit (PRE) is not signaled in the RxBD.

Reference Manual:

QEIWRM, Rev 3, Chapter 13 “UCC POS Controller (UPOS)”

Work Arounds:

None

PPPI**ML/MC PPP transmitter Weighted Fair Queueing—Mixed Mode.****Description and Impact on Functionality:**

ML/MC PPP transmitter Weighted Fair Queueing mechanism operating in Mixed Mode (strict priority queues mixed with queues scheduled with WFQs) skips strict priority queues for a few frames.

Reference Manual:

QEIWRM, Rev 3, Section 25.7.3.4, “Mixed Mode”

Work Arounds:

Use Precise Weighted Fair Queueing if available.

See QEIWRM, Rev 3 Sections:

Section 25.12, “Bundle Parameter Table (BPT)”, Table 25-11, “Bundle Parameter Table Fields”, Transmit class weighted fair queue mode (Tx_CWFQ_Mode).

Section 25.11 Link Parameter Table (LPT), Table 25-8, “Link Parameter Table (LPT)”, Transmit Link Weighted Fair Queue mode (Tx_LWFQ_Mode).

PPPIW1 **Possible SDMA error when using PPP IW to CPU.****Description and Impact on Functionality:**

Possible SDMA error when using PPP IW to CPU.

Reference Manual:

QEIWRM, Rev 3, Section 32.5.2, “Queue Operation Modes”

Work Arounds:

None.

QMC1 **QMC Stop Receive command.****Description and Impact on Functionality:**

When QMC Stop Receive command is issued, it is not guaranteed that all closed BDs are introduced with an interrupt.

Reference Manual:

QEIWRM, Rev 3, Section 24.4.2, "Receive Commands"

Work Arounds:

After issuing a Stop Receive host command to a specific channel, the RX BD ring should be checked for leftover BD's with E=0.

VP1 **General Timer always triggered when in Virtual Port Polling mode.****Description and Impact on Functionality:**

When working with Virtual Port Polling mode, the General Timer is always triggered, even if no General Timer has been enabled by the user.

Reference Manual:

QEIWRM, Rev 3, Section 32.5.1, “Triggering Modes”

Work Arounuds:

Configure a “dummy” general timer as described in QEIWRM, Rev 3, Section 4.4, “RISC Timer Tables”

VP2 **Possible SDMA error and/or cache coherency problem when using the Virtual Port Fast Swap Queue operation mode.**

Description and Impact on Functionality:

Possible SDMA error and/or cache coherency problem when using the Virtual Port Fast Swap Queue operation mode. Therefore, the Virtual Port Fast swap queue operation mode is not functional.

Reference Manual:

QEIWRM, Rev 3, Section 32.5.2, “Queue Operation Modes”

Work Arounuds:

Use the Swap BD’s mode.

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