Mask Set Errata

MSE908QY1_3L69J
12/2002

Mask Set Errata for MC68HC908QY1, Mask 3L69J

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Introduction

This mask set errata applies to this MC68HC908QY1 MCU mask set:

- 3L69J

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3L69J. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “0201” indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Page Erase Can Cause Unexpected Erase of a Another FLASH Page

SE26-PAGE_ERASE

Detailed Description:

There are two blocks of FLASH memory in the MCU which are selected (internally) by array select signals. Address values are protected against changes after a page erase sequence has started. Any attempt to write a new address after HVEN=1 is blocked. However, due to a logic error, the latching of the array select signals is not blocked so it is possible that one page in one array could be unintentionally erased when a page erase is performed on a page in the other array.

For example, suppose you started a page erase of the $EE00–EE3F page and during this erase (while HVEN=1) you wrote to $FFFF to clear the COP watchdog timer. Since $FFFF is a valid address in the second array, its array select would erroneously get latched. The address latches are blocked from changes so the address that was written to start the original page erase would determine which page in the upper array ($FFB0–FFBF or $FFC0–FFFF) would begin to be page erased. The upper array only decodes latched address line A6 to decide which of the two possible pages to erase. This address line was latched as a 0 when the original page erase operation was initiated, so in this example the $FFB0–FFBF page in the upper array would begin a page erase operation. Since all other controls needed for page erase were latched based on the original page erase request, block protection was taken into account at that time. When the new write to $FFFF was executed, only the array select was latched (independent of the block protect logic). Therefore, even if the $FFB0–FFBF page was block protected, it would still be page erased.

Workaround:

Do not write to any other FLASH address while a page erase sequence is in progress. This would include avoiding writes to $FFFF which is both a valid FLASH address and the address you write to to service the COP watchdog.

Disable the COP watchdog, or use a timeout period that is longer than the page erase time (4 ms) and write to $FFFF immediately before and after doing any page erase.

PTA3 Data Bit Cannot Be Read When PTA3 Pin Configured as an Output

SE27-PTA3

Detailed Description:

When the PTA3 pin is configured as an output (DDRA3=1), writes to port A work correctly, but reads of port A return an indeterminate value in bit 3 rather than the value last written to the PTA3 data register. Any attempt to use a read-modify-write instruction (ASL, ASR, BCLR, BSET, COM, DEC, INC, LSL, LSR, NEG, ROL, or ROR) to modify any bit in port A while PTA3 is configured as an output can result in an unexpected change to PTA3.

While PTA3 could be used as an output in an application where read-modify-write instructions are avoided, debugging with monitor mode is complicated by a BCLR #0,PTA instruction in the MON08 monitor ROM. When V_{tst} is applied to PTA2/$\overline{IRQ}$ to force traditional monitor mode, PTA3 functions correctly but PTA2/$\overline{IRQ}$ is not available for user applications. In the case of the user mode monitor access program described in AN2305/D, V_{tst} is not present so it is not practical to use the monitor program in the MON08 ROM to debug a system that uses PTA3 as an output.

Workarounds:

- Design your application so PTA3/$\overline{RST}$/KBI3 is used as a general-purpose input, reset, or a keyboard interrupt input and use other port pins for general-purpose output functions.
- If PTA3 must be used as an output, do not use read-modify-write instructions to change any port A data values. In this case, debugging would need to be done with traditional monitor mode where PTA2/$\overline{IRQ}$ is connected to a higher-than-V_{DD} level called V_{tst}. The user mode monitor access program described in AN2305/D should not be used in this case because PTA3 could be changed unexpectedly whenever the monitor executed a breakpoint or traced a single instruction.

Excess Power Supply Current on A/D Input Pins

SE28-EXCESS

Detailed Description:

The four A/D pins (PTA0/AD0/TCH0/KBI0, PTA1/AD1/THC1/KBI1, PTA4/OSC2/AD2/KBI4, and PTA5/OSC1/AD3/KBI5) are internally connected to hysteresis input buffers which do not include logic to disable these buffers. When these pins are used as A/D inputs and a static analog level near mid-supply is applied, both the N-channel and P-channel transistors in the hysteresis buffer are partially on, causing a leakage path from V_{DD} to V_{SS}. Typical extra current when the analog level is at the worst case mid-supply level is on the order of 0.5 mA per pin at room temperature and 1.3 mA at cold temperature. This extra current is present in run or stop modes and does not prevent normal operation.

Workaround:

Where possible, design your system so analog levels are only present on the A/D inputs when an A/D reading is actually being performed. For example, in the case of a potentiometer or resistor ladder, rather than connect the top of the resistor to V_{DD}, connect it to a general-purpose output pin. When you are about to take an A/D reading, change the output to one (V_{DD} minus a small drop across the output transistor) and when the reading is finished, switch the output to 0 (V_{SS}). This will eliminate the extra leakage from this errata and will also eliminate the current through the potentiometer or resistor ladder.

In other systems it may be possible to disable the power supply to analog components before entering stop mode. This would force A/D inputs to V_{SS} and there is no extra leakage when these inputs are at V_{DD} or V_{SS}.

Any other workaround that forces the pin level to V_{SS} or V_{DD} during idle periods would eliminate this extra supply current.

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