FREESCALE SEMICONDUCTOR, MICROCONTROLLER DIVISION
CUSTOMER ERRATA AND INFORMATION SHEET
Part: MPC565.C
General Business Use
Report Generated: Wed Oct 27, 2010, 13:46:04

MPC565.C

ERRATA AND INFORMATION SUMMARY

AR_917 PADS: Connect VDDRTC to VDDSRAM1, VDDSRAM2 to VDDSRAM3
AR_1082 TPU ROM: Channels with the COMM ROM function affect other channels
AR_848 PADS: Negative current injection causes QADC conversion errors
AR_899 MPC565: Masknum is 0x11
AR_912 Bit 15 of the Reset Configuration Word is not documented
AR_904 BBC2: Branch targets must be 4 sequential instructions before MTSPR BBC SPR.
AR_905 BBC2: Disable BTB, or disable data show cycles and restrict store addresses.
AR_983 BBC2: Disable instruction show cycles while BTB is in use
AR_1078 BBC2: Do not enable BTB and Instruction Show Cycles at the same time
AR_870 BBC2: Do not use debug mode with BTB enabled, if code has 0x2F30 branch target.
AR_1079 BBC2: Flush the BTB if instructions in a region are changed during execution
AR_1121 BBC2: Do not run software from the DECRAM that modifies the DECRAM contents
AR_793 BBC2 Compression: No Compressed Code in Addresses $FFF00000 to $FFFFFFFF
AR_838 BBC2: Set BCMEE bit in the BBCMCR to 0
AR_1057 UC3F: censorship can be overridden in certain cases
AR_1146 UC3F: Contents of 0x00-0x1F may be invalid after HRESET if using RCW from flash
AR_1150 UC3F: Flash may not operate correctly with certain conditions at high frequency
AR_914 UC3F: Set censor operation requires a Reset to read Censor bits
AR_973 UC3F: Frequent Suspend/Resume Operations may cause Program or Erase Timeouts
AR_974 UC3F: FLASHID field in the UC3FMCRE is 0x01
AR_1132 UC3F: UC3F registers can only be accessed when in supervisor mode
AR_1057 UC3F: censorship can be overridden in certain cases
AR_1146 UC3F: Contents of 0x00-0x1F may be invalid after HRESET if using RCW from flash
AR_1150 UC3F: Flash may not operate correctly with certain conditions at high frequency
AR_914 UC3F: Set censor operation requires a Reset to read Censor bits
AR_973 UC3F: Frequent Suspend/Resume Operations may cause Program or Erase Timeouts
AR_974 UC3F: FLASHID field in the UC3FMCRE is 0x01
AR_1132 UC3F: UC3F registers can only be accessed when in supervisor mode
AR_1011 UC3FBIU: CENSOR bits cannot be cleared even if UC3FCFIG[IWS] is 0
AR_815 UC3F: Set small and remainder blocks to same access attributes
AR_1073 CALRAM: Aborted overlay accesses could halt processor
AR_1087 DLCMD2: do not allow RxFIFO to overflow or read using a high priority interrupt
AR_1126 DLCMD2: Transmitter may need to be reset after losing arbitration
AR_755 DLCMD2 switching into 1x-4x mode
AR_772 DLCMD2 Equating Parameter Values
AR_785 DLCMD2 RFIFO Polling
AR_771 DLCMD2 SEL bit is not lockable.
AR_1143 L2U: Care required when changing a slave MCU’s mode in multi-master systems
AR_841 MIOS14: Match value intermittently ignored in OC mode when writing a new value
AR_1127 MIOS: MDASMSCR polarity bit has no effect when open-drain mode selected
AR_911 Pads: Leakage May Affect Required Pull Up/Downs
AR_1025 PADRING_565: QSMCM_B wired-or mode affects vfls1_mpio32b4
AR_1027 PADRING_565: C_T2CLK does not have hysteresis
AR_1028 PADRING_565: TEXP pin will not output when VDD is turned off
AR_1029 PADRING_565: Selecting wired-or in toucan_c affects mpio32b13
AR_1049 PADS: No pull down on JCOMP
AR_1099 Padring: HRESET and SRESET require external pullup resistors
AR_1123 PADRING_565: Oscillator may overdrive some 20Mhz cyrstals
AR_1131 PADS: The weak internal pull device remains enabled on RSTCONF/TEXP
AR_922 PADS: VOH2.6 Spec changed to -1 mA
AR_940 JTAG: Do Not Switch All Pads Simultaneously When JTAG Enabled
AR_1018 Execute memory write prior to slave read for slave predischarge

AR_1019 RCPU: Don’t execute overflow type before update type MUL/DIV instruction
AR_1077 RCPU: Do not run multi-master compressed application with Show Cycles and BTB
AR_1138 RCPU: Data breakpoint exception may occur even if conditions are not met
AR_1076 RCPU: Treat VF queue flush information value of 6 as 2
AR_907 RCPU: Issue ISYNC command when entering debug mode
AR_440 RCPU: Execute any IMUL/DIV instruction prior to entering low power modes.
AR_211 Do not set breakpoint on mtspr ICTRL instruction
AR_214 Only negate interrupts while the MSR[EE] disables interrupts (MSR[EE]=0)
AR_949 QADC64E: Write CCW[EOQ] to 0x3F for the End of Queue
AR_915 QADC64E: Conversion Clock cannot be shared between Master/Slave Modules
AR_1125 QADC64: Don’t change both BQ2 and MQ2 while Q2 is running
AR_420 QADC64: Don’t change BQ2 with a set of SSE2 without a mode change.
AR_1048 QADC64E: Sample Time is 8 QCLKs instead of 16 when CCW[IST]=1 in Enhanced Mode
AR_1151 SCI: TXD pin reverts to output immediately when SCCxR1[TE] is cleared
AR_1041 READI: Trace may show incorrect Addresses When Exception Relocation is used
AR_1050 READI: Unexpected READI Overflow Error Messages
AR_1051 READI: Trace can’t handle multiple change of flow without a show cycle
AR_1118 READI: Program Flow Tracking Error Under Rare Condition
AR_1061 READI: New Feature added to allow queue mode to empty instead of flush
AR_1060 READI: Program Trace Sync Messages do not include sequential instruction count
AR_846 READI: Synchronize the MCKI input clock to the MCKO output clock.
AR_924 READI: Communication lost when clock freq is changed via Nexus with BDM enabled
AR_698 READI Input message requires 2 MCKI idle after READI Enabled.
AR_1021 READI: Manufacturer ID in Device ID register is incorrect
AR_1059 READI: 8-bit and some 16-bit data trace messages can’t be differentiated
AR_1065 READI: Queue entries to change from 16 to 32 on future revisions
AR_1066 READI: Program trace requires all change of flow show cycles
AR_783 READI input messages must be 4 MCKI apart.
AR_1144 TouCAN: Transmit buffers may freeze or indicate missing frame
AR_1045 CAN: Bus Off recovery not ISO compliant
AR_1142 TouCAN: Writing to an active receive MB may corrupt MB contents
AR_627 TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase
AR_985 USIU: Do not use ORx[EHTR] with Dual Mapping
AR_925 USIU: TEXP feature does not function when VDD supply is off
AR_909 USIU: Do not assert cr_b to abort pending store reservation access
AR_910 USIU: PITRTC Clock may not work when SCCR[RTDIV] is 0
AR_984 USIU: Setting of SCCR[EBDF] may slow execution of code
AR_1134 USIU: RTC, DEC, TB and PIT counters may not count after PORESET or HRESET
AR_1158 USIU: Stop Time Base to write new value
AR_287 USIU: System to Time Base frequency ratio must be greater than 4
AR_479 USIU: The MEMC does not support external master burst cycles
AR_868 USIU: Do not rely on censorship to prevent access on parts with internal Flash
AR_1135 USIU: Disable USIU burst in debug mode if READI R/W feature is used
AR_1152 USIU: PORESET must always be asserted before the 2.6V supplies reach 0.5V
AR_1154 SIU: RTSEC register not documented; May affect the initial increment of the RTC
AR_865 USIU: Do not rely on the VDDSRAM Low Voltage Detect Circuit
AR_1113 USIU: Ensure HRESET/SRESET negation time is longer than 3 CLKOUT periods
AR_833 USIU: Do not TEA data showcycles or enable data show cycles in single chip mode
AR_869 USIU: Do not enable BRx[SST] with SCCR[EBDF]>0
AR_1153 USIU: Sleep and Deep-Sleep modes require power to all 2.6V supplies
AR_389 Little Endian modes are not supported
AR_1109 USIU: Do not write zero value to the SYPCR[BMT]
AR_1120 USIU: Interrupt Controller may generate vector 0x0 or has no request indication
AR_1137 USIU: RSR[LLRS] can be set even though no loss of lock reset has occurred
AR_1155 SIU: TEA for external access must be negated within 1 system bus clock

DETAILED ERRATA DESCRIPTIONS

CDR_AR_917 Customer Erratum MPC565.C

PADS: Connect VDDRTC to VDDSRAM1, VDDSRAM2 to VDDSRAM3

DESCRIPTION:
The VDDRTC power supply was shorted internally to VDDSRAM1, VDDSRAM2 has been shorted internally to VDDSRAM3.

WORKAROUND:
Always connect the VDDRTC supply to VDDSRAM1 and VDDSRAM2 to VDDSRAM3.

CDR_AR_1082 Customer Erratum MPC565.C

TPU ROM: Channels with the COMM ROM function affect other channels

DESCRIPTION:
The TPU COMM ROM Function causes problems in other channels. When the Host Service request is set to 0b11, all channels that do not use the COMM function will be forced to outputs and a random state will be selected.

WORKAROUND:
Either: 1) Re-initialize all other channels after the COMM function has been initialized; or 2) If a fixed COMM TPU function is required, download an updated TPU ROM image into the DPTRAM and use the TPU in emulation mode.

CDR_AR_848 Customer Information MPC565.C

PADS: Negative current injection causes QADC conversion errors

DESCRIPTION:
Injection current of more than 1 mA flowing out of the part (negative current) can cause conversion errors on QADC analog input channels at room temperature. During high temperature operation (150 C), this worsens to 0.5 mA flowing out of the part. Negative current injection implies that current is flowing out of the part to the system. To get this condition, a voltage lower than VSS must exist on the channel for current to flow in this manner. Positive injection current is not an issue.

WORKAROUND:
Do not inject current greater than 1 mA out of the part. The QADC64 disruptive input current minimum specification was changed from -3 mA to -1 mA. The maximum disruptive Input current is still +3 mA.

CDR_AR_899 Customer Information MPC565.C

MPC565: Masknum is 0x11

DESCRIPTION:
The Masknum field of the IMMR register was updated from 0x10 to 0x11 to indicate a minor revision of the device mask set.

WORKAROUND:
Update software that reads the IMMR register to read 0x3311 instead of 0x3310 for the PARTNUM:MASKNUM.

CDR_AR_912 Customer Information MPC565.C

Bit 15 of the Reset Configuration Word is not documented

DESCRIPTION:
Bit 15 of the Reset Configuration Word is not documented in the Reference Manual. Bit 15 is the Interlock Write Select (IWS). This bit determines which interlock write operation should be used during the clear censorship operation. 0 = Interlock write is defined as a write to any UC3F array location. 1 = Interlock write is a write to the UC3FMCR register. This bit always comes from the shadow row of the flash module being accessed and never comes from the External Reset Configuration Word.

WORKAROUND:
Consult the latest version of the Reference Manual (dated June 29,2001 or later). The net affect is that if bit 15 is cleared (0), then the censor bits can only be cleared while running in an uncensored mode. If bit 15 is set (1), then the censor bits can also be cleared in censored mode by performing a clear censorship operation, which erases the flash module. Refer to manual dated after June 2001.

CDR_AR_904 Customer Erratum BBC2.CDR3UBUS_04_0

BBC2: Branch targets must be 4 sequential instructions before MTSPR BBC SPR.

DESCRIPTION:
A user application may crash when a BBC SPR is written in a program loop, if the MTSPR is within 4 instructions of a branch target.

WORKAROUND:
1) Make sure that a "mtspr" instruction writing to any BBC SPR register is preceded by four instructions that are not the target of any branch and followed by "isync" instruction, or 2) Disable BTB. Refer to manual dated on or after May 2003.

CDR_AR_905 Customer Erratum BBC2.CDR3UBUS_04_0

BBC2: Disable BTB, or disable data show cycles and restrict store addresses.

DESCRIPTION:
A memory write access on the UBUS with address bits [18:27] that match the following patterns: 0b10 0001 0000 xxxx (0x210X), 0b10 0001 0001 xxxx (0x211X), 0b10 0001 1001 xxxx (0x219X), 0b10 0001 1000 xxxx (0x218X), 0b10 0011 0000 xxxx (0x230X), 0b10 0011 0101 (0x235X), 0b10 0011 1000 (0x238X), 0b10 0101 1000 (0x258X), 0b10 0101 1001 (0x259X), 0b10 0111 1000 (0x278X), or 0b10 0111 1001 (0x279X) or the BBC SPRs representation on the UBUS will wrongly invalidate BTB entries. Note that the "X" - don’t care bits and first hex number may also be "6/a/e". This will cause user application performance degradation and crash in some cases.

WORKAROUND:
1) Avoid writing to external memory locations or memory mapped registers at addresses that match the problematic addresses and disable data show cycles on the CALRAM memory range, or 2) Disable the BTB.

CDR_AR_983 Customer Erratum **BBC2.CDR3UBUS_04_0**

BBC2: Disable instruction show cycles while BTB is in use

DESCRIPTION:
If the BBCMCR[BTEE] is set and instruction show cycles are enabled (ICTRL[ISCT_SER] not equal to 0x7), the RCPU may execute incorrect code.

WORKAROUND:
Disable show cycles (set ICTRL[ISCT_SER] to 0bX11) while the BBCMCR[BTEE] is set, or disable the BTB while instruction show cycles are enabled. Note this workaround is also required for AR_1078.

CDR_AR_1078 Customer Erratum **BBC2.CDR3UBUS_04_0**

BBC2: Do not enable BTB and Instruction Show Cycles at the same time

DESCRIPTION:
If the BTB is enabled together with instruction show cycles (ICTRL[ISCT_SER] not equal to 0x7), the RCPU may execute incorrect instructions.

WORKAROUND:
Do not enable instruction show cycles when the BTB is enabled; or disable the BTB if instruction show cycles are required.

CDR_AR_870 Customer Erratum **BBC2.CDR3UBUS_04_0**

BBC2: Do not use debug mode with BTB enabled, if code has 0x2F30 branch target.

DESCRIPTION:
The BTB (Branch Target Buffer) incorrectly matches in debug mode if there was a change of flow address of 0x2F30 and code from the address resides in the valid BTB buffer when the part enters debug mode. The address 0x2F30 is the debug port instruction register (SPR) address that the core issues to the BBC in debug mode for instruction fetches. The debug tool may lose communication with the part since the debug port will not assert the "ready" status (DSDO pin "low") until reset.

WORKAROUND:
Do not use debug mode on applications running with the BTB enabled if there is a branch with a target address of 0x2F30. Alternatively, either do not enable the BTB in debug mode or do not put any code at 0x2F30.

CDR_AR_1079 Customer Erratum **BBC2.CDR3UBUS_04_0**

BBC2: Flush the BTB if instructions in a region are changed during execution

DESCRIPTION:
If an IMPU region register has the BTB inhibit bit set (MI_RAx[BTBINH] = 1), the BTB inhibit function does not work for the first branch pointing into the region. These instructions will be stored in a vacant BTB table entry. Any following branches in the same region will NOT be stored in the BTB. This is the correct operation. In addition, the instructions following a branch out of the region will not be stored in the BTB table. This issue will only cause problems if there is a possibility that the instructions at a cached address are changed after they have been executed once.

WORKAROUND:
1) Disable the BTB if the caching from a memory region is undesirable; or 2) Flush the BTB by disabling and then re-enabling the BBCMCR[BTEE] any time the contents of a memory changes, prior to executing from that memory.

CDR_AR_1121 Customer Erratum **BBC2.CDR3UBUS_04_0**

BBC2: Do not run software from the DECRAM that modifies the DECRAM contents

DESCRIPTION:
When executing code from the DECRAM, a store instruction with destination address in the DECRAM may result in an overwrite of that code area.

WORKAROUND:
Do not perform data writes to the DECRAM while also executing code from DECRAM. The DECRAM should only be loaded while executing from a different memory.

CDR_AR_793 Customer Information **BBC2.CDR3UBUS_04_0**

BBC2 Compression: No Compressed Code in Addresses $FFF00000 to $FFFFFFFF

DESCRIPTION:
IMPU translates addresses in compression mode regardless of address form. Note that this may have a minor application impact. It will cause a failure ONLY if the compressed address space covers $FFF00000 to $FFFFFFFF and the BBCMCR[ETRE] and BBCMCR[EIR] are set, enabling Exception Table Relocation and Enhanced External Interrupt Relocation.

WORKAROUND:
Do not put compressed code at addresses $FFF00000 to $FFFFFFFF if Exception Table Relocation or Enhanced External Interrupt Relocation are enabled by BBCMCR[ETRE] and BBCMCR[EIR]. Refer to manual dated on or after May 2003.

CDR_AR_838 Customer Information BBC2.CDR3UBUS_04_0

BBC2: Set BCMEE bit in the BBCMCR to 0

DESCRIPTION:
No performance improvement is expected for the branch instructions BC and BL when setting BCMEE bit in BBCMCR.

WORKAROUND:
BBCMCR[BCMEE] (bit 27) should be written to 0. Refer to Reference Manuals dated after 29 June, 2001 that have references to this bit deleted.

CDR_AR_1057 Customer Erratum C3FARRAY_A.512KCDR3_02_0

UC3F: censorship can be overridden in certain cases

DESCRIPTION:
It is possible that Censorship can be overwritten under certain conditions. These conditions will not be documented.

WORKAROUND:
Program RCW[IWS] to 0 when censorship is enabled. This will provide an additional layer of protection by preventing access to the array except when executing from the array.

CDR_AR_1146 Customer Erratum C3FARRAY_A.512KCDR3_02_0

UC3F: Contents of 0x00-0x1F may be invalid after HRESET if using RCW from flash

DESCRIPTION:
When using the Reset Configuration Word (RCW) located in internal flash, addreses 0x00-0x1F of the UC3F may be incorrectly read from the shadow row instead of the data array after HRESET. This will continue to occur until an instruction is fetched from an address outside the 0x00-0x1F range. For example, when the internal flash RCW is programmed with exception table relocation enabled (IP = 1 and ETRE = 1) and the vector table base address is 0x0 (OERC = 0b00), the reset vector absolute branch may not be correctly fetched and the application may not start properly.

WORKAROUND:
Option 1) Use the external RCW or the default internal RCW. Option 2) When using the internal flash RCW: A) Ensure the first instruction fetch from the flash is outside of 0x00-0x1F by locating the reset vector outside of 0x00-0x1F. This can be done by setting IP = 0 or ETRE = 0 (reset vector at 0x100), or by setting IP = 1, ETRE = 1, and OERC != 0b00 (reset vector at 0x10008, 0x80008 or 0x3FE008). The vector table can be relocated later in the application if required. OR B) Program the same data/instructions to addresses 0x00-0x1F of both the shadow row and the data array.

CDR_AR_1150 Customer Erratum C3FARRAY_A.512KCDR3_02_0

UC3F: Flash may not operate correctly with certain conditions at high frequency

DESCRIPTION:
Data may be fetched or instructions may be executed incorrectly from the internal flash memory when the system frequency is greater than 40MHz under certain conditions. This is most likely to occur under extreme conditions such as a noisy system, poor board layout, extreme temperatures etc. For example programming one array while running the algorithm from the other array at temperatures less than 0C may cause incorrect instruction execution. Or branching repeatedly between arrays within a few instructions at 56MHz below 0C may cause incorrect data or instruction fetches.

WORKAROUND:
Run at a maximum system frequency of 40MHz. For applications that require a system frequency higher than 40MHz, use a newer version MPC565. For applications that require in-field flash programming, execute the program / erase code from any other memory such as the internal RAM or an external memory device.

CDR_AR_914 Customer Erratum C3FARRAY_A.512KCDR3_02_0

UC3F: Set censor operation requires a Reset to read Censor bits

DESCRIPTION:
During the internal verify read of a Censor Set operation, the internally unselected censor wordline are not driven to the appropriate voltage. Subsequently, the verify read may update the Censor registers with invalid data and may inadvertently place the UC3F into Information Censorship mode. Only registers bits that should be read as as zero may incorrectly be read as a one. Accesses to the array may also produce invalid data.

WORKAROUND:
The UC3F module requires a Reset Operation after any Program or Erase Operation to the Censor[0:1] bits in the UC3FMCR register.

CDR_AR_973 Customer Information C3FARRAY_A.512KCDR3_02_0

UC3F: Frequent Suspend/Resume Operations may cause Program or Erase Timeouts

DESCRIPTION:
Frequent use of the suspend or resume feature can cause a premature timeout of the program or erase time. The internal program and erase state machine has a counter for the maximum allowable program or erase time. This counter is incremented prior to the actual program or erase pulse. If the operation is suspended at a high frequency, it is possible that the upper count will be reached prior to completion of the program or erase operation. This will primarily be seen during erase operations.

WORKAROUND:
Do not suspend a program or erase at a high frequency (more than approximately once per millisecond). Refer to manual dated on or after May 2003.

CDR_AR_974 Customer Information C3FARRAY_A.512KCDR3_02_0

UC3F: FLASHID field in the UC3FMCRE is 0x01

DESCRIPTION:
The Flash ID field in the UC3FMCRE register is defined to be 0x01

WORKAROUND:
Ensure that software can use future values of the flash ID field.

CDR_AR_1132 Customer Information C3FARRAY_A.512KCDR3_02_0

UC3F: UC3F registers can only be accessed when in supervisor mode

DESCRIPTION:
All UC3F registers are accessible only when the device is in supervisor mode. Any attempt to access the UC3F registers in user mode will terminate the cycle with a data error exception.

WORKAROUND:
Ensure all UC3F registers are accessed only when in supervisor mode. Refer to manual dated after September 2003.

CDR_AR_1057 Customer Erratum C3FARRAY_B.512KCDR3_02_0

UC3F: censorship can be overridden in certain cases

DESCRIPTION:
It is possible that Censorship can be overwritten under certain conditions. These conditions will not be documented.

WORKAROUND:
Program RCW[IWS] to 0 when censorship is enabled. This will provide an additional layer of protection by preventing access to the array except when executing from the array.

CDR_AR_1146 Customer Erratum C3FARRAY_B.512KCDR3_02_0

UC3F: Contents of 0x00-0x1F may be invalid after HRESET if using RCW from flash

DESCRIPTION:
When using the Reset Configuration Word (RCW) located in internal flash, addreses 0x00-0x1F of the UC3F may be incorrectly read from the shadow row instead of the data array after HRESET. This will continue to occur until an instruction is fetched from an address outside the 0x00-0x1F range. For example, when the internal flash RCW is programmed with exception table relocation enabled (IP = 1 and ETRE = 1) and the vector table base address is 0x0 (OERC = 0b00), the reset vector absolute branch may not be correctly fetched and the application may not start properly.

WORKAROUND:
Option 1) Use the external RCW or the default internal RCW. Option 2) When using the internal flash RCW: A) Ensure the first instruction fetch from the flash is outside of 0x00-0x1F by locating the reset vector outside of 0x00-0x1F. This can be done by setting IP = 0 or ETRE = 0 (reset vector at 0x100), or by setting IP = 1, ETRE = 1, and OERC != 0b00 (reset vector at 0x10008, 0x80008 or 0x3FE008). The vector table can be relocated later in the application if required. OR B) Program the same data/instructions to addresses 0x00-0x1F of both the shadow row and the data array.

CDR_AR_1150 Customer Erratum C3FARRAY_B.512KCDR3_02_0

UC3F: Flash may not operate correctly with certain conditions at high frequency

DESCRIPTION:
Data may be fetched or instructions may be executed incorrectly from the internal flash memory when the system frequency is greater than 40MHz under certain conditions. This is most likely to occur under extreme conditions such as a noisy system, poor board layout, extreme temperatures etc. For example programming one array while running the algorithm from the other array at temperatures less than 0C may cause incorrect instruction execution. Or branching repeatedly between arrays within a few instructions at 56MHz below 0C may cause incorrect data or instruction fetches.

WORKAROUND:
Run at a maximum system frequency of 40MHz. For applications that require a system frequency higher than 40MHz, use a newer version MPC565. For applications that require in-field flash programming, execute the program / erase code from any other memory such as the internal RAM or an external memory device.

CDR_AR_914 Customer Erratum C3FARRAY_B.512KCDR3_02_0

UC3F: Set censor operation requires a Reset to read Censor bits

DESCRIPTION:
During the internal verify read of a Censor Set operation, the internally unselected censor wordline are not driven to the appropriate voltage. Subsequently, the verify read may update the Censor registers with invalid data and may inadvertently place the UC3F into Information Censorship mode. Only registers bits that should be read as as zero may incorrectly be read as a one. Accesses to the array may also produce invalid data.

WORKAROUND:
The UC3F module requires a Reset Operation after any Program or Erase Operation to the Censor[0:1] bits in the UC3FMCR register.

CDR_AR_973 Customer Information C3FARRAY_B.512KCDR3_02_0

UC3F: Frequent Suspend/Resume Operations may cause Program or Erase Timeouts

DESCRIPTION:
Frequent use of the suspend or resume feature can cause a premature timeout of the program or erase time. The internal program and erase state machine has a counter for the maximum allowable program or erase time. This counter is incremented prior to the actual program or erase pulse. If the operation is suspended at a high frequency, it is possible that the upper count will be reached prior to completion of the program or erase operation. This will primarily be seen during erase operations.

WORKAROUND:
Do not suspend a program or erase at a high frequency (more than approximately once per millisecond). Refer to manual dated on or after May 2003.

CDR_AR_974 Customer Information C3FARRAY_B.512KCDR3_02_0

UC3F: FLASHID field in the UC3FMCRE is 0x01

DESCRIPTION:
The Flash ID field in the UC3FMCRE register is defined to be 0x01

WORKAROUND:
Ensure that software can use future values of the flash ID field.

CDR_AR_1132 Customer Information C3FARRAY_B.512KCDR3_02_0

UC3F: UC3F registers can only be accessed when in supervisor mode

DESCRIPTION:
All UC3F registers are accessible only when the device is in supervisor mode. Any attempt to access the UC3F registers in user mode will terminate the cycle with a data error exception.

WORKAROUND:
Ensure all UC3F registers are accessed only when in supervisor mode. Refer to manual dated after September 2003.

CDR_AR_1011 Customer Erratum C3FBIU.CDR3UBUS_02_0

UC3FBIU: CENSOR bits cannot be cleared even if UC3FCFIG[IWS] is 0

DESCRIPTION:
The UC3FCFIG[IWS] bit may get cleared inadvertently at the deassertion of system reset. This means that only a write to a valid array location will serve as the erase interlock write for clearing CENSOR bits. If the array is already censored then it is not possible to clear the CENSOR bits at all.

WORKAROUND:
Do not censor the array (CENSOR=11) before production, as it may not be possible to clear the CENSOR bits if the array is censored.

CDR_AR_815 Customer Erratum C3FBIU.CDR3UBUS_02_0

UC3F: Set small and remainder blocks to same access attributes

DESCRIPTION:
Small blocks require the same attributes (supv/user and data/data&instr) as their remainder blocks. Failure to set this configuration may result in bus error on access to a remainder block.

WORKAROUND:
If the SBSUPV bit for a small block is set as supervisor, then the SUPV bit for the remainder of the block must also be set as supervisor. If the SBDATA bit for a small block is set as data only, then the DATA bit for the remainder of the block must also be set as data only.

CDR_AR_1073 Customer Erratum CALBIU32K.CDR3LBUS_02_0

CALRAM: Aborted overlay accesses could halt processor

DESCRIPTION:
If using the overlay feature of the CALRAM, aborted accesses could lock up the microcontroller if the second of two consecutive overlayed back-to-back data reads is aborted due to an exception and the exception writes to the same CALRAM module that is used for the overlay.

WORKAROUND:
Avoid consecutive overlayed CALRAM accesses in applications with interrupts or other exceptions. Specifically, avoid accessing the same CALRAM module (such as save registers to the stack) within an exception routine that is being used for flash overlay until a bus transaction is performed to a different data area (another CALRAM module, an IMB or USIU register or an SPR in the L2U or BBC). The easiest and least impact workaround is to perform a dummy write to any unused register through the L-bus in all exception handlers prior to any CALRAM access. Any SPR outside the RCPU could be used. An example is to use a write of any register to a L2U Region Attribute Register (mtspr 827, r0; L2U_RA3) that is disabled in the L2U Global region Attribute register (L2U_GRA[EN3]=0).

CDR_AR_1087 Customer Erratum DLCMD2.CDR3IMB3_04_0

DLCMD2: do not allow RxFIFO to overflow or read using a high priority interrupt

DESCRIPTION:
The DLCMD2 RxFIFO status register (STAT) bit 6 will become stuck high (1), indicating that there is a completion code in the RxFIFO. This occurs when a completion code is being read from the RxFIFO and a completion code is being written into the RxFIFO simultaneously. This occurance is highly unlikely, but may occur over time if the RxFIFO is allowed to repeatedly overflow, causing completion codes to be continually written to the RxFIFO.

WORKAROUND:
Implement a high priority service routine to insure that the DLCMD2 RxFIFO is read before another message completes and is put into the RxFIFO. This will prevent the possibility that completion codes will be written and read simultaneously.

CDR_AR_1126 Customer Erratum DLCMD2.CDR3IMB3_04_0

DLCMD2: Transmitter may need to be reset after losing arbitration

DESCRIPTION:
The DLCMD2 transmitter may incorrectly remain idle if it loses arbitration and an Incomplete Byte Received error or a Bit Timing Error is received before an End Of Frame is detected, and a Terminate Auto Retry (TAR) command was not previously issued. The Receiver Status Register (STAT) will indicate that the TxFIFO is full, but no transmission will occur until the transmitter is reset and a new message loaded into the TxFIFO.

WORKAROUND:
Reset the transmitter by issuing an Abort Transmission Now command (CMD[7:5] = 0b111) if either of the following cases occur when reading a valid completion code (CC[6] = 0). CASE 1: The completion code indicates a Transmitter Lost Arbitration status, and either an Incomplete Byte Received error or a Bit Timing Error (CC[7:0] = 0b1010xx01, or 0b1010xx10). CASE 2: STAT indicates the TxFIFO is full (STAT[1:0] = 0b11), and the completion code indicates Transmitter Not Involved for the transmitter action status (CC[5:4] = 0b00).

CDR_AR_755 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 switching into 1x-4x mode

DESCRIPTION:
If 4x mode is entered before the symbol counter value reaches the normal mode TIFS value but after the counter has passed the 4x mode TIFS value, the module will hang. Before a transmitter can send an SOF (which resets the symbol counter) it must wait for either of the two following conditions. One, TIFS must have been reached. Two, REOF and a rising edge from another module must have been detected. The second condition means that if another module tries to access the bus before TIFS and after REOF then we can also contend and try and gain access to the bus. If no other module is trying to access the bus then condition two won't occur. The symbol counter does not reset when the mode is changed. This means that if the module is put into 4x mode before the normal mode TIFS value has been detected (which would signal an SOF and reset the counter) the module will keep counting until it reaches its max value and holds. Since the counter is stuck at its max value the module can never detect any symbols on the bus so it will hang until reset.

WORKAROUND:
TIFS must be waited for before changing to 4x mode. To wait for TIFS the difference between the normal mode REOF and TIFS values must be found manually based on their values in the SDATA register. Once that value is determined, wait for bus_idle (REOF), which can be polled for, plus (TIFS - REOF) amount of time. Assuming all cycle counts for normal mode parameters are greater than or equal to the cycle counts for the 4x parameters, no delay (waiting for TIFS) is needed to transition from 4x to normal mode. Note that the bus should be idle when the transition takes place (regardless as to whether the DLCMD2 has detected idle or not) as it is always a bad idea to transition between modes during a message.

CDR_AR_772 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 Equating Parameter Values

DESCRIPTION:
If certain symbols are assigned the same counter value, one of the symbols might never be recognized. Instead the other symbol with the same value would be detected. For example, if RMIN=TSHA than an active RMIN will never be recognized. In the hardware implementation the parameter values are checked with a priority scheme. Once a parameter matches, no further checking is done until the next clock cycle when the counter value has changed. For an active pulse the following parameters are checked in order: TSOF, TSHA, TLNA, TBRK, RMIN, RSH, RLN, and REOF. In order for each parameter to be detectable they must all have unique values. Similarly, during a passive pulse the following parameters are checked in order: TSHP, TLNP, TIFR, TIFS, RMIN, RSH, RLN, REOF. Again, this set of passive parameters must be distinct. Keeping these parameters distinct is almost guaranteed due to the timing requirements of the J1850 specifications. Certain round trip delays in the transceiver may suggest that some parameters should be equated. In this case either parameter should be adjusted to make them unique. The real risk of equation parameters occurs in test mode when parameters are set as small as possible to accelerate testing.

WORKAROUND:
Parameters in the active set must all be distinct and parameters in the passive set must all be distinct.

CDR_AR_785 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 RFIFO Polling

DESCRIPTION:
Reads from the staus/rdata word result in valid data being popped from the RFIFO. If the FIFO is empty no pop occurs. This behavior is implemented as follows. First, the status and data at the head of the FIFO is returned. If the FIFO is currently empty, the status register will indicate this and the FIFO data returned will be invalid. After the read has completed, the FIFO will be popped if not empty. The problem occurs if data has been pushed since the status register read indicated an empty FIFO. In this case, when the pop is requested, the FIFO contains valid data which is then popped and lost.

WORKAROUND:
When polling for data, access the status register with a byte read access. Upon finding valid data present in the FIFO, access both the status and data with a word read access.

CDR_AR_771 Customer Information DLCMD2.CDR3IMB3_04_0

DLCMD2 SEL bit is not lockable.

DESCRIPTION:
The spec states that if LCK=1 writes to the SEL bit are disabled. This is not the case. The SEL bit can still be written when LCK=1. This allows the user to read both the 1x SDATA parameters and the 4x SDATA parameters. If writes to the SEL bit were not allowed, after the LCK bit was set it would only be possible to view one set of SDATA parameters depending on the state of the SEL bit wen the LCK bit was set.

WORKAROUND:
This is the desired operation of the DLCMD2. The reference manual will be updated to reflect this operation.

CDR_AR_1143 Customer Information L2U.CDR3LBUSUBUS_03_0

L2U: Care required when changing a slave MCU’s mode in multi-master systems

DESCRIPTION:
If an external master changes the mode of a slave MCU from slave to peripheral mode by setting EMCR[PRPM], and then accesses addresses on the slave MCU’s LBUS at the same time as the slave MCU’s RCPU accesses addresses over the UBUS for data, a deadlock may occur. The slave MCU may lock up until reset assertion.

WORKAROUND:
Ensure the slave MCU’s RCPU does not perform data accesses over the UBUS when an external master changes the slaves MCU mode from slave to peripheral mode, and then accesses the slave MCU’s LBUS (i .e. CALRAM). Use interrupts or other notification mechanisms to prevent the slave MCU’s RCPU from writing/reading data over UBUS.If the slave MCU changes its own mode, ensure any subsequent load/store instruction over the UBUS is at least 6 instructions after the write to EMCR[PRPM], or that they are separated by an ISYNC instruction.

CDR_AR_841 Customer Information MIOS14.CDR3IMB3_02_0

MIOS14: Match value intermittently ignored in OC mode when writing a new value

DESCRIPTION:
On B register update of an OC channel (B is NOT double-buffered) the update should enable the compare and match of the B register to the relevant Time Base. If the B register update is done in a time when a match (Not enabled) to the previous B value occurs, the compare and match mechanism will NOT be enabled for the new value.

WORKAROUND:
When updating the B register in OC mode write it twice.

CDR_AR_1127 Customer Information MIOS14.CDR3IMB3_02_0

MIOS: MDASMSCR polarity bit has no effect when open-drain mode selected

DESCRIPTION:
MDASMSCR[EDPOL] does not change the polarity of the MDA pin when MDASMSCR[WOR] = 1. This only applies to the MDASM output modes (OCB, OCAB and OPWM).

WORKAROUND:
Do not rely on MDASMSCR[EDPOL] to change the output polarity when open-drain mode is selected for an MDASM pin in output mode. Refer to the latest version of the Reference Manual (dated August 2003 or later).

CDR_AR_911 Customer Erratum PADRING.565_CDR3_02_1

Pads: Leakage May Affect Required Pull Up/Downs

DESCRIPTION:
During power up, there is an additional leakage path that must be overcome on pins that are used for configuring the initial device operation. Pull down devices may pull up initially. This may cause a problem on pins used to the configure the part. These pins include the data bus (if an external reset config word is used), MODCK[1:3], JCOMP, DSCK, and DSDI.

WORKAROUND:
For all pins with internal pull down devices that need to be low to configure the device, either add an external pull-down resistor (10K or less) or ensure there is a load of at least 50pF on the pin. On pins with internal pull up devices that need to be pulled low, lower the value of the external pull down resister to 3K ohms or less.

CDR_AR_1025 Customer Erratum PADRING.565_CDR3_02_1

PADRING_565: QSMCM_B wired-or mode affects vfls1_mpio32b4

DESCRIPTION:
Setting the QSMCM_B SPCR0[WOMQ] to select open drain mode on the QASCM_B QSPI, also sets the vfls1_mpio32b4 pin to an open-drain driver (wired-or) mode.

WORKAROUND:
1) Do not set QSMCM_B SPCR0[WOMQ]. 2) Select vfls1_mpio32b4 to be an input function in mpio mode, Or 3) Do not use vfls1 function on vfls1_mpio32b4 for debugging in this mode without an external pull up resistor.

CDR_AR_1027 Customer Erratum PADRING.565_CDR3_02_1

PADRING_565: C_T2CLK does not have hysteresis

DESCRIPTION:
The C_T2CLK pad does not have hysteresis enabled. This may cause additional edges of the T2CLK to be sampled for the TCR2 of the TPU3_C module.

WORKAROUND:
Use a filtered waveform to drive the T2CLK.

CDR_AR_1028 Customer Erratum PADRING.565_CDR3_02_1

PADRING_565: TEXP pin will not output when VDD is turned off

DESCRIPTION:
When turning off VDD in low power mode (Key-off), TEXP will not drive the output to indicate that the related timer has expired.

WORKAROUND:
Do not rely on TEXP to assert while in Low power mode while VDD is off.

CDR_AR_1029 Customer Erratum PADRING.565_CDR3_02_1

PADRING_565: Selecting wired-or in toucan_c affects mpio32b13

DESCRIPTION:
Setting open drain (wired-or) mode on the toucan_c module also sets open drain mode on the mpio32b13 pin, when the mpio32b13 is used as an output.

WORKAROUND:
The CANTX0_C pin is shared with the MPIO32B13 function. Do not set toucan_c open drain mode when the mpio32b13 output function is selected. Only set open drain mode when the toucan_c function is used on this pin.

CDR_AR_1049 Customer Erratum PADRING.565_CDR3_02_1

PADS: No pull down on JCOMP

DESCRIPTION:
JCOMP pin does not have a pull down resistor. If the pin floats and is sampled high, the part will be in JTAG compliant mode, instead of BDM or normal operation.

WORKAROUND:
Tie or drive the JCOMP pin using an external device.

CDR_AR_1099 Customer Erratum **PADRING.565_CDR3_02_1**

Padring: HRESET and SRESET require external pullup resistors

DESCRIPTION:
The MPC565 Reference Manual states that external pullups are required for SRESET and HRESET, but it also states that there are internal weak pullups. These internal pullups are not enabled.

WORKAROUND:
As the MPC565 Reference Manual states, external pullups are always required on the HRESET and SRESET signals. In future revisions, the pull up may be disabled by PDMCR[SPRDS] bit.

CDR_AR_1123 Customer Information **PADRING.565_CDR3_02_1**

PADRING_565: Oscillator may overdrive some 20Mhz cyrstals

DESCRIPTION:
The oscillator output may overdrive some low-power 20Mhz crystals, and over the lifetime of the crystal this may cause degredation

WORKAROUND:
Design the crystal circuit to withstand the oscillator output.

CDR_AR_1131 Customer Information **PADRING.565_CDR3_02_1**

PADS: The weak internal pull device remains enabled on RSTCONF/TEXP

DESCRIPTION:
If PDMCR[SPRDS] is set by software after reset negates, the weak internal pull device on RSTCONF/TEXP remains enabled. This has no impact on applications designed according to the specification.

WORKAROUND:
There is no workaround required for applications designed according to the specification. If PDMCR[SPRDS] is set, and the pin is set to input mode, the existing external pull device or driver will overdrive the weak internal pull device (maximum = 130uA) on RSTCONF/TEXP.

CDR_AR_922 Customer Information **PADRING.565_CDR3_02_1**

PADS: VOH2.6 Spec changed to -1 mA

DESCRIPTION:
The IOH specification for all 2.6 volt outputs has been changed from -2 mA to -1 mA to insure a VOH2.6 of 2.3 volts. An additional specification has been added for VOH2.6A for a -2.0 mA load with a minimum VOH of 2.1 volts.

WORKAROUND:
2.6 volt outputs will only drive -1.0 mA with a VOH of 2.3 volts and will drive -2.0 mA with an output voltage of 2.1 volts minimum. Refer to manual dated after June 2001.

CDR_AR_940 Customer Information PADRING.565_CDR3_02_1

JTAG: Do Not Switch All Pads Simultaneously When JTAG Enabled

DESCRIPTION:
JTAG mode puts all output pins in fast slew rate mode. The power supply pins of the device cannot supply enough current to allow all pins to be changed at the same time in fast slew rate mode. During normal operation, this is not an issue since all pins on the device do not switch at the same time.

WORKAROUND:
When using JTAG, all pins should not be switched simultaneously. Refer to manual dated on or after May 2003.

CDR_AR_1018 Customer Information PADRING.565_CDR3_02_1

Execute memory write prior to slave read for slave predischarge

DESCRIPTION:
When using multiple processors on a common bus with an external device that outputs voltages exceeding 3.1v, the predischarge cycle will not occur if the processor that initiated the read is different than the processor that initiated the write.

WORKAROUND:
Perform a write access to external memory to discharge the external bus, or read a value of 0x0 from the external device prior to accessing another MPC56x device on the same bus. Refer to manual dated on or after May 2003.

CDR_AR_1019 Customer Erratum RCPU.CDR3LBUSIBUS_16_1

RCPU: Don’t execute overflow type before update type MUL/DIV instruction

DESCRIPTION:
When an integer overflow type non multiply or divide instruction (designated by an ’o’ in the instruction mneumonic, such as addo) starts to execute before a previously started Condition Register 0 (CR0) update type integer multiply or divide instruction (designated by a ’.’ in the instruction mneumonic, such as divw.) completes, the CR0[SO] bit may be wrongly updated from the XER[SO] bit earlier changed by the overflow type instruction. For example, instruction sequence "divw. Rx,Ry,Rz , subfo Rt,Ru,Rv" may cause this problem. It does not happen if the overflow type instruction is also a CR0 update type instruction (designated by ’o.’ in the instruction mneumonic, such as addo.), or if register dependencies exist.

WORKAROUND:
Do any one of the following: 1) Keep a gap of at least 1 instruction between a CR0 update type integer multiply instruction and an overflow type instruction or a gap of 4 integer or 6 other instructions between a CR0 update integer divide instruction and an overflow type instruction; 2) Use the CR0 update type for both instructions; 3) Run the RCPU in serialized mode; 4) Place a "sync" instruction between the integer multiply/divide instruction and the overflow type instruction; 5) Don’t use the update form of integer multiply or divide instructions; or 6) Don’t use overflow type integer instructions. (Note: most compiler vendors do not generate the error case.)

CDR_AR_1077 Customer Erratum RCPU.CDR3LBUSIBUS_16_1

RCPU: Do not run multi-master compressed application with Show Cycles and BTB

DESCRIPTION:
If instruction show cycles (ICTRL[ISCT_SER] not equal to 0x7) and BTB are enabled in a compressed application with interrupts and another master (READI or External Bus master) initiates internal accesses on UBUS, the RCPU may execute incorrect instructions.

WORKAROUND:
Do not enable instruction show cycles together with BTB while running compressed application with interrupts if a UBUS master (READI or External Master) other than the RCPU or the L2U operated by the RCPU, accesses MCU internal resources through the UBUS.

CDR_AR_1138 Customer Erratum RCPU.CDR3LBUSIBUS_16_1

RCPU: Data breakpoint exception may occur even if conditions are not met

DESCRIPTION:
The RCPU may incorrectly take a second data breakpoint exception, if a data breakpoint occurs on a load/store instruction with a load following within five instructions in the RCPU program flow. This extra exception will only be taken if very specific internal bus timing occurs during the instruction sequence and the data breakpoint state remains set after the first data breakpoint exception is taken. In this condition, any load/store instruction executed with breakpoints enabled will cause the second data breakpoont exception.The additional exception sets SRR0 to the effective address of the instruction after the second load/store instruction, but the BAR register remains set to the effective address of the first load/store instruction that met the data breakpoint conditions.If the processor is in a non-recoverable state (MSR[RI] = 0) and breakpoints are not masked (LCTRL2[BRKNOMASK] = 1), the first load/store instruction within the data breakpoint exception handler (usually saving CPU context) will cause the second exception, handler re-entrance and loss of program tracking.

WORKAROUND:
1) Run RCPU in serialized mode. 2) Create conditions for an exception during the data breakpoint exception handler execution after saving SRR0/1 on the stack, for example, use ’SC’ instruction inside the handler, or a floating point instruction if the Floating Point Unit is disabled, or an unimplemented instruction. This exception will reset the internal data breakpoint state, eliminating the false data breakpoint exception.

CDR_AR_1076 Customer Erratum RCPU.CDR3LBUSIBUS_16_1

RCPU: Treat VF queue flush information value of 6 as 2

DESCRIPTION:
When the RCPU fetches instructions from zero wait state slaves on UBUS (Internal flash or SIU when in enhanced burst mode), the VF queue flush information may have the reserved value of 6.

WORKAROUND:
If a VF instruction queue flush value of 6 is shown on the VF pins, tools should treat this value as 2 for program tracking purposes.

CDR_AR_907 Customer Information RCPU.CDR3LBUSIBUS_16_1

RCPU: Issue ISYNC command when entering debug mode

DESCRIPTION:
If the ICTRL[29] bit is set (non-serialized mode) then the RCPU issues two instruction fetch requests into the instruction pipeline after entering debug mode. The debug port and the debug tool may get confused when processing an "mtspr DPDR,Rx" instruction. The debug tool loses synchronization with debug port and receives the wrong data for the "Rx" register. The typical case is when the debug tool tries to save scratch registers or read the debug mode cause.

WORKAROUND:
Issue an ISYNC instruction to the debug port prior to any other instructions when the RCPU enters debug mode after running code. Refer to manual dated on or after May 2003.

CDR_AR_440 Customer Information RCPU.CDR3LBUSIBUS_16_1

RCPU: Execute any IMUL/DIV instruction prior to entering low power modes.

DESCRIPTION:
There is a possibility of higher than desired currents during low power modes. This is caused by a possible contention in the IMUL/DIV control area. This contention may only exist prior to the execution of any IMUL/DIV instruction.

WORKAROUND:
Execute a MULLW instruction prior to entering into any low power mode (anytime after reset, and prior to entering the low power mode). Refer to manual dated on or after May 2003.

CDR_AR_211 Customer Information RCPU.CDR3LBUSIBUS_16_1

Do not set breakpoint on mtspr ICTRL instruction

DESCRIPTION:
When a breakpoint is set on an "mtspr ICTRL,Rx" instruction and ICTRL[IIFM] = 1, the result will be unpredictable. The breakpoint may or may not be taken on the instruction and value of the IIFM bit can be either 0 or 1.

WORKAROUND:
Do not put a break point on mtspr ICTRL, Rx instruction when ICTRL[IIFM] is set to 1. Refer to manual dated on or after May 2003.

CDR_AR_214 Customer Information RCPU.CDR3LBUSIBUS_16_1

Only negate interrupts while the MSR[EE] disables interrupts (MSR[EE]=0)

DESCRIPTION:
If the MSR[EE] bit is set and an external interrupt request to the RCPU is negated before the external interrupt vector is issued, the RCPU may become unpredictable until the device is reset. This interrupt event may be generated by software while managing peripheral modules in the MCU, or external devices connected to external interrupt request pins of the MCU or the MCU interrupt controller. This issue may occur when performing USIU operations like masking interrupt requests, clearing interrupt flags, masking or changing interrupt logic in the interrupt controller, or switching on/off enhanced interrupt control if available.

WORKAROUND:
Do not clear an interrupt that is not being serviced by software while MSR[EE]=1. Software should disable interrupts (MSR[EE]=0) in the RCPU before clearing or masking any interrupt source from the USIU, IMB or external pin. For external interrupt request pins, it is recommended that edge triggered interrupts be used. No delay time is required before re-enabling interrupts (MSR[EE]=1). Refer to manual dated on or after May 2003.

CDR_AR_949 Customer Erratum QADC64E.CDR3IMB3_03_0

QADC64E: Write CCW[EOQ] to 0x3F for the End of Queue

DESCRIPTION:
Using 0x7F as an EOQ (end of queue) causes a conversion of VRL to occur when the EOQ is reached. In single or continuous scan modes, this conversion is underway when the queue wraps back to the first word, and the first conversion is not performed. The result for the conversion of VRL gets written in the result space for the first conversion word. The queue and conversions then proceed on correctly.

WORKAROUND:
Always use 0x3F instead of 0x7F as an EOQ in the CCW for both Legacy and Enhanced modes of QADC64E operation. Refer to an updated Reference Manual dated after January 2003.

CDR_AR_915 Customer Erratum QADC64E.CDR3IMB3_03_0

QADC64E: Conversion Clock cannot be shared between Master/Slave Modules

DESCRIPTION:
In a multiple QADC64E module configuration it is not possible to operate the modules on synchronous conversion clocks. The conversion clock of a module configured as Master cannot be input to the Slave .

WORKAROUND:
If simultaneous conversions are required, the customer can trigger both QADC64E modules SIMULTANEOUSLY using the external trigger inputs (ETRIG1 or 2), however, the conversions will not be performed SYNCHRONOUSLY. There is no workaround to allow synchronous QADC64E module operation. Do not set EXTCLK of the QADCMCR register to use the conversion clock of a master QADC (don’t set to 1). References to this feature are removed in updated Reference Manuals dated after January 2003.

CDR_AR_1125 Customer Erratum QADC64E.CDR3IMB3_03_0

QADC64: Don’t change both BQ2 and MQ2 while Q2 is running

DESCRIPTION:
There exists a window of 2 system clocks in the conversion cycle during which a change to the Queue2 trigger mode (QACR2[MQ2]) along with a change to the Queue2 start location (QACR2[BQ2]) while Queue2 is active will cause the new value for BQ2 to be ignored. The new trigger mode takes place and conversions continue to be stored in Q2 as defined by the previous BQ2. Hence the locations following the new BQ2 will not contain results.

WORKAROUND:
Before changing the Queue2 mode, disable Q2 (MQ2=0b0000), then update MQ2 and BQ2.

CDR_AR_420 Customer Information QADC64E.CDR3IMB3_03_0

QADC64: Don’t change BQ2 with a set of SSE2 without a mode change.

DESCRIPTION:
Changing BQ2 and setting SSE2 with no mode change will cause Q2 to begin but not recognize the change in BQ2. Further, changes of BQ2 after SSE2 is set, but before Q2 is triggered are also not recognized. All other sequences involving a change in BQ2 are recognized.

WORKAROUND:
Be sure to do mode change when changing BQ2 and setting SSE2. Recommend setting BQ2 first then setting SSE2. Refer to manual dated on or after May 2003.

CDR_AR_1048 Customer Information QADC64E.CDR3IMB3_03_0

QADC64E: Sample Time is 8 QCLKs instead of 16 when CCW[IST]=1 in Enhanced Mode

DESCRIPTION:
If the QADC64E is in enhanced mode, the documentation says that the Input sample time is 16 QCLKs when CCW[IST]=1. Actually the Input sample time is 8 QCLKs. On the MPC561-564, enhanced mode is enabled by setting QADCMCR[FLIP]=1. The MPC565 is always in enhanced mode.

WORKAROUND:
Always expect the Input Sample time to be 8 QCLKs when CCW[IST]=1 when operating in enhanced mode. Refer to manual dated after January 2003.

CDR_AR_1151 Customer Erratum QSMCM.CDR3IMB3_03_2

SCI: TXD pin reverts to output immediately when SCCxR1[TE] is cleared

DESCRIPTION:
When the Transmiter Enable bit of the SCI Control Register 1 is cleared (SCCxR1[TE]=0), the Transmit Data pin, TXD, reverts immediately to general purpose output mode, and the pin will be driven high or low as determined by the PortQS Data Register, PORTQS. If the transmitter is not idle when SCCxR1[TE] is cleared, any data still being output on the TXD pin will be lost.

WORKAROUND:
Ensure SCCxR1[TE] is only cleared after the Transmit Complete bit of the SCI status Register is set (SCxSR[TC]=1).

CDR_AR_1041 Customer Erratum READI.CDR3LBUSUBUS_02_0

READI: Trace may show incorrect Addresses When Exception Relocation is used

DESCRIPTION:
When the BBC2 Exception relocation feature is used, the READI (Nexus) may report the incorrect addresses for exceptions that are relocated.

WORKAROUND:
Tools should expect either the relocated exception address or the non-relocated address for flow reconstruction. The following READI Nexus trace message may use either of these addresses as its base for next relative address. i.e. when the non relocated address was transmitted via Nexus, the correct relocated address could be used in calculating the relative address. In the case of the Enhanced External Interrupt Relocation feature, the tool may need to know the EEIR base address (EIBADR) and additional information to fully reconstruct the flow of instructions.The tool can either "fingerprint" each exception vector routine to identify the exact exception or require users to set a watchpoint at the non-relocated address (0xFFF0_0500).

CDR_AR_1050 Customer Erratum READI.CDR3LBUSUBUS_02_0

READI: Unexpected READI Overflow Error Messages

DESCRIPTION:
Under certain internal bus conditions the READI program trace may generate an overrun condition regardless of the state of the queue. This has been seen on miss-predicted branches that follow multi-cycle instructions and generate a branch message and a correction message in consecutive cycles. No incorrect information is generated by the READI, information currently in the queue is lost and this is indicated. Examples of multi-cycle instructions are reads and writes to IMB/USIU registers, floating point operations, integer multiply/divide, etc. It can also be seen when an exception message causes a correction message (cancels a previous branch) on the bus. This causes back-to-back U-bus transactions. If this occurs and the READI module was not ready for the first transaction it will also cause the trace overrun message. Either of these trace overrun conditions cause the Nexus message queue to be flushed.

WORKAROUND:
Either run the PPC in serialized mode or add 3 nop instructions between the instruction that sets the condition code flags and the branch. Eliminating U-bus and internal READI bus traffic will help minimize the occurrence of this issue. An additional option is to accept gaps in the reconstruction flow trace.

CDR_AR_1051 Customer Erratum READI.CDR3LBUSUBUS_02_0

READI: Trace can’t handle multiple change of flow without a show cycle

DESCRIPTION:
The READI program trace state machine can not handle multiple VF change of flow indications before the corresponding show cycle for the first change of flow appears on the U-bus. The READI matches change of flow indications to the show cycles and can only store one of each at a time. If two of either occur before the other, then incorrect information is sent in the Nexus trace packet.

WORKAROUND:
Run the PPC in serialized mode. If code cannot be run serialized (due to performance impact), reducing U-bus traffic will help in minimize the occurrence of this issue. Turn on SIUMCR[NOSHOW] and turn off L-bus data show cycles.

CDR_AR_1118 Customer Erratum READI.CDR3LBUSUBUS_02_0

READI: Program Flow Tracking Error Under Rare Condition

DESCRIPTION:
Under certain conditions, the program trace information output by the READI module may not accurately reflect the actual program flow. This condition requires ALL of the following conditions: 1) Either the BTB or code compression is enabled. 2) A double branch instruction sequence must occur where: the first branch is indirect and its condition is already determined or is non-conditional, the second branch is conditional and is miss-predicted and then corrected due to a long (execution time) instruction. And 3) the BBC must be held off the U-bus so that U-bus show cycle addresses are delayed.

WORKAROUND:
Either disable code compression and the BTB, or accept erroneous trace reconstruction under this rare condition.

CDR_AR_1061 Customer Erratum READI.CDR3LBUSUBUS_02_0

READI: New Feature added to allow queue mode to empty instead of flush

DESCRIPTION:
The READI flushes all information out of the queue on an overrun detection. The theory was trace could be restarted as soon as possible after the overrun. In practice, this information is valuable in determining the cause of the overrun for tuning what is getting traced.

WORKAROUND:
Tools may need to be modified to allow selection of the behavior of the READI queue being filled. A new register has been added to the Nexus memory map at address 0xB (11). See an updated Reference Manual (dated after November 2002) for a complete description.

CDR_AR_1060 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Program Trace Sync Messages do not include sequential instruction count

DESCRIPTION:
Program Trace Sync Messages do not include sequential instruction count which can cause a loss of synchronization in some cases. This operation is in compliance with the IEEE-ISTO 5001-1999 standard which can lead to the loss of trace information when the program sync message is sent.

WORKAROUND:
The development tool can analyze the trace information along with the disassembled code to determine the I-CNT value in most cases. The tool may not be able to determine the exact number of instructions that were executed if the Program Trace Sync Message is sent due to an exception or interrupt.

CDR_AR_846 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Synchronize the MCKI input clock to the MCKO output clock.

DESCRIPTION:
The READI module may not properly receive input messages if the input clock is not synchronous with the output clock.

WORKAROUND:
Synchronize the MCKI input clock to the MCKO output clock. Refer to manual dated on or after May 2003.

CDR_AR_924 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Communication lost when clock freq is changed via Nexus with BDM enabled

DESCRIPTION:
When the READI is enabled to use BDM accesses, a deadlock occurs when the development tool tries to enter a low-power mode or change the clock frequency (via the debug port). The internal clock will still run at the previous frequency. If code running on the target is changing the frequency then the following will occur: All READI MDI/MSEI traffic is ignored when this change is recognized; All MDO messages in the transmit FIFO will be sent; Then the MCKO will be stopped until the PLL has relocked at the new frequency.

WORKAROUND:
Do not change the system clock frequency from the Nexus debug port. Use code running on the target to change the clock speed. Reset the system by asserting sreset_b or hreset_b to continue debugging after unsuccessfully changing the clock frequency.

CDR_AR_698 Customer Information READI.CDR3LBUSUBUS_02_0

READI Input message requires 2 MCKI idle after READI Enabled.

DESCRIPTION:
If an input message is sent to the READI immediately after deassertion of RSTI_B (enabling READI) the READI may not recognize the start of the message and will ignore it. This behavior could cause the tool to get out of sync with the READI.

WORKAROUND:
Do not send an input message until at least 2 MCKI after READI is enabled, or better, until the DID message is received from the READI. Refer to manual dated on or after May 2003.

CDR_AR_1021 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Manufacturer ID in Device ID register is incorrect

DESCRIPTION:
The manufacturer ID number in the READI Device Identification (DID) register is incorrect for Motorola’s assigned JEDEC value.

WORKAROUND:
Nexus Tools should not expect the JEDEC defined Motorola ID (0x0E), but instead should expect the documented value of 0x1C for the MID field in the READI Device ID Register.

CDR_AR_1059 Customer Information READI.CDR3LBUSUBUS_02_0

READI: 8-bit and some 16-bit data trace messages can’t be differentiated

DESCRIPTION:
8-bit data trace messages transmit the same message as 16-bit data trace messages with a most significant byte of 0. This is a result of a shortcoming in the IEEE-ISTO 5001-1999 standard.

WORKAROUND:
Any Trace Tool that supports data trace via an 8-bit wide Nexus port must determine the data size from the source code or code disassembly and not rely on the number of bits transmitted.

CDR_AR_1065 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Queue entries to change from 16 to 32 on future revisions

DESCRIPTION:
The number of entries in the READI queue will increase from 16 to 32 on future revisions of READI. This change will not affect external tools, but should allow more information to be traced at the same time without queue overflows.

WORKAROUND:
None required.

CDR_AR_1066 Customer Information READI.CDR3LBUSUBUS_02_0

READI: Program trace requires all change of flow show cycles

DESCRIPTION:
A mode may be added to a future revision of the READI module to allow program trace to be done with the ICTRL field ISCTL equal to anything except 0b11 (no show cycles). Currently this field must equal 0b01 (show all change of flows). Operating with ISCTL==0b10 increases performance of the system. The only effect is that synchronization messages will no longer be transmitted with direct branch messages, so the sync request is held until the next indirect branch.

WORKAROUND:
Set ICTRL[ISCT_SER] to 0x5. Tools will need to be updated to support ICTRL[ISCT_SER]=0x6 mode of operation in the future.

CDR_AR_783 Customer Information READI.CDR3LBUSUBUS_02_0

READI input messages must be 4 MCKI apart.

DESCRIPTION:
READI input messages must be spaced by at least 4 MCKI input clocks.

WORKAROUND:
Wait for an output message response before sending in another input message.

CDR_AR_1144 Customer Erratum TOUCAN.CDR3IMB3_05_1

TouCAN: Transmit buffers may freeze or indicate missing frame

DESCRIPTION:
If a received frame is serviced during reception of a second frame identified for the same MB (message buffer) and a new Tx frame is also initiated during this time, the Tx MB can become frozen and will not transmit while the bus is idle. The MB remains frozen until a new frame appears on the bus. If the new frame is a received frame, the frozen MB is released and will arbitrate for external transmission. If the new frame is a transmitted frame from another Tx MB, the frozen MB changes its C/S (control status word) and IFLAG to indicate that transmission has occurred, although no frame was actually transmitted. The frozen MB occurs if lock, unlock and initiate Tx events all occur at specific times during reception of two frames. The timing of the lock event affects the timing window of the unlock event as follows: Situation A) Rx MB is locked during the second frame. A frozen Tx MB occurs if: 1) Both of these events occur in either a-then-b or b-then-a order: a) A new transmission is initiated by writing its C/S between CRC6 (sixth bit of CRC field) and EOF7 (seventh bit of end of frame) of the second frame. b) The Rx MB is locked by reading its C/S after EOF6 of first frame and before EOF6 of second frame. 2) The Rx MB is unlocked between EOF7 and intermission at end of the second frame. Notice in this situation that if the lock/unlock combination happens close together, the lock must have been just before EOF6 of the second frame, and therefore the system is very close to having an overrun condition due to delayed handling of received frames. Situation B) Rx MB was locked before EOF6 of the first frame; in other words, before its IFLAG is set. This is a less likely situation but provides a larger window for the unlock event. A frozen Tx MB occurs if: 1) The Rx MB is locked by reading its C/S word before EOF6 of the first frame. 2) Both of these events occur in either a-then-b or b-then-a order: a) A new transmission is initiated by writing its C/S word sometime between CRC6 and EOF7 of the second frame. b) The Rx MB is unlocked between CRC6 and intermission at end of the second frame. Notice in this situation that if the unlock event occurs after EOF6, the first frame would be lost and the second frame would be moved to the Rx MB due to the delayed handling of received frames. Situation C) Rx unlocked during bus idle. A frozen/missing Tx occurs if: 1) An Rx MB is locked before EOF6 of an incoming frame with matching ID and remains locked at least until intermission. This situation would usually occur only if the received frame was serviced after reception of a second frame. 2) An internal arbitration period is triggered by writing a C/S field of an MB. 3) The locked Rx MB is unlocked within two internal arbitration periods (defined below) before or after step 2). 4) 0xC is written to the C/S of a Tx MB within these same two arbitration periods. This step is optional if 0xC was writin in step 2) above. Two internal arbitration periods are calculated as ((2 * number of MBs) + 16) IMB clocks. Additional Notes: 1) The received frames can be transmitted from the same node, but they must be received into an Rx MB. 2) When the frozen Tx MB’s IFLAG becomes set, an interrupt will occur if enabled. 3) The timestamp of the missing Tx will be set to the same timestamp value as the last reception before it was frozen. 4) If the user software locks the Rx MB before a frame is received, situation A can occur with a single received frame. 5) The issue does not occur if there were any additional pending Tx MBs before CRC6. 6) If multiple Tx MBs are initiated within the CRC6/EOF7 window (situation A and B) or two internal arbitration windows (situation C), they all become frozen.

WORKAROUND:
If received frames can be handled (lock/unlocked) before EOF6 of the next frame, situations A and C are avoided. If they are handled before CRC6, or lock times are below 23 CAN bit times, situation B is avoided. If these conditions cannot be guaranteed, situation A and B are avoided by inserting a delay of at least 28 CAN

bit times between initiating a tranmission and unlocking an Rx MB, and vice versa. Typically a system would use a mechanism to selectively add the necessary delay. For example, software might use a global variable to record an external timer value (the TouCAN timer can't be used as that would unlock) when initiating a new Tx or unlocking an Rx, and then add the required delay before performing second action. Situation C can be avoided by inserting a delay of at least two internal arbitration periods between writing 0xC and unlocking the locked Rx MB.

CDR_AR_1045 Customer Information TOUCAN.CDR3IMB3_05_1

CAN: Bus Off recovery not ISO compliant

DESCRIPTION:
The Bus Off recovery is not ISO compliant on the FlexCAN and TouCAN modules. The ISO specification indicates that the CAN node should remain inactive until user intervention restarts it. The FlexCAN and TouCAN modules both include an automatic recovery mechanism for the Bus Off condition.

WORKAROUND:
The Bus Off condition interrupt should be enabled and an interrupt service routine implemented to disable the CAN. The user's software should then determine when the CAN should be re-activated.

CDR_AR_1142 Customer Information TOUCAN.CDR3IMB3_05_1

TouCAN: Writing to an active receive MB may corrupt MB contents

DESCRIPTION:
Deactivating a TouCAN receive message buffer (MB) may cause corruption of another active receive MB, including the ID field, if the following sequence occurs. 1) A receive MB is locked via reading the Control/Status word, and has a pending message in the temporary receive serial message buffer (SMB). 2) A second frame is received that matches a second receive MB, and is queued in the second SMB. 3) The first MB is unlocked during the time between the CRC field and the 6th bit of end of frame (EOF) of the second frame. 4) The second MB is deactivated within 20 IMB clock cycles of the 6th bit of EOF, resulting in corruption of the first MB.

WORKAROUND:
Do not write to the Control/Status word after initializing a receive MB. If a write (deactivation) is required to the Control/Status field of an active receive MB, either FREEZE the TouCAN module or insert a delay of at least 27 CAN bit times plus 21 IMB clock cycles between unlocking one MB and deactivating another MB. This will avoid MB corruption, however frames may still be lost.

CDR_AR_627 Customer Information TPU3.CDR3IMB3_03_0

TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase

DESCRIPTION:
Incorrect generation of 50% duty cycle is caused by the command combination "write_mer, end". If the write_mer is the last instruction together with the end, this may create an additional match using the old contents of the match register (which are in the past now and therefore handled as an immediate match)

WORKAROUND:
Add neg_mrl together with the last write_mer and with end-of-phase. The negation of the flag overrides the false match which is enabled by write_mer and postpones the match effect by one micro-instruction. In the following micro-instruction the NEW MER value is already compared to the selected TCR and no false match is generated. The neg_mrl command has priority over the match event recognition, separating the write_mer and the end command. This gives enough time for the new MER to update before the channel transition re-enables match events.

CDR_AR_985 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Do not use ORx[EHTR] with Dual Mapping

DESCRIPTION:
When an access is matched through the Dual Mapping registers (DMBR/DMOR), extended hold time (from a previous access region) or Burst length (from the new access region) may cause execution of wrong code.

WORKAROUND:
1) Do not set ORx[EHTR] while a dual mapping region is enabled. Or: 2) Do not enable dual mapping if an extended hold time is required for any memory in the system.

CDR_AR_925 Customer Erratum USIU.CDR3UBUS_10_1

USIU: TEXP feature does not function when VDD supply is off

DESCRIPTION:
The TEXP function does not work if the main power supplies are powered down. Whenever VDD (low voltage supplies other than KAPWR and VDDSRAM) is powered down, hreset_b will be asserted by the chip and low power mode exited. The TEXP pin will never be asserted.

WORKAROUND:
The TEXP pin will never be asserted if VDD is powered down. Use an external counter to indicate the length of power down. As an alternate solution, put the part into Deep Sleep mode to reduce power consumption and leave the power supplies powered.

CDR_AR_909 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Do not assert cr_b to abort pending store reservation access

DESCRIPTION:
If an external cancel reservation (cr_b) is asserted then a pending store reservation may show on the external bus. This may occur with or without transfer start (ts_b), and will terminate after 1 clock. If the region is in the memory controller of the chip generating the store with reservation, then no chip-select or other memory controller attributes will assert on the bus, and the memory will not be altered.

WORKAROUND:
1) Do not assert cr_b; or 2) following assertion of cr_b, external logic must prevent the erroneous store with reservation bus cycle from altering memory, and must not assert ta_b to terminate the erroneous store with reservation bus cycle.

CDR_AR_910 Customer Erratum USIU.CDR3UBUS_10_1

USIU: PITRTC Clock may not work when SCCR[RTDIV] is 0

DESCRIPTION:
The RCPU RTC/PIT may not count in all operating conditions if the ratio of System clock to the PITRTC Clock is less than or equal to 4. This may happen if the SCCR[RTDIV] is set to 0 and either 1) the part is running on the limp clock, or 2) the PLPRCR[MF] = 0 and both the System PLL and the PITRTC Clock use the same clock source (EXTCLK or the crystal oscillator).

WORKAROUND:
Keep the System Clock to PITRTC clock frequency ratio greater than 4. This can be done the easiest by setting the SCCR[RTDIV] to a value of 1 (reset value).

CDR_AR_984 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Setting of SCCR[EBDF] may slow execution of code

DESCRIPTION:
If the SCCR[EBDF] is greater than 0 and the RCPU is running not serialized, the USIU may issue external read bus cycles that are not complete. The TS_B will assert with an address, but without a chip select or STS_B assertion. These cycles may cause a delay in execution of application code. These cycles will self terminate in 1 to 3 clocks, depending on the TS_B signal negation rate, defined by the external pull up strength and board capacitance.

WORKAROUND:
There are two possible workarounds: 1) In a program with critical timing, do not run from external memory with the SCCR[EBDF] set to a value greater than 0. Or 2) If external logic is used as a memory controller, define the logic to disregard these extra bus cycles.

CDR_AR_1134 Customer Erratum USIU.CDR3UBUS_10_1

USIU: RTC, DEC, TB and PIT counters may not count after PORESET or HRESET

DESCRIPTION:
The Real-Time Clock (RTC), Timebase (TB), Decrementer (DEC) and Periodic Interrupt Timer (PIT) may not count during the time between PORESET or HRESET negation and the time at which the PLL is programmed by application software and becomes locked to the target frequency.

WORKAROUND:
Always program the PLL to the target operating frequency (by changing the PLPRCR[MF] or PLPRCR[DIVF] bits) before referencing the TB, RTC, DEC, or PIT in an application after a PORESET or a HRESET.

CDR_AR_1158 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Stop Time Base to write new value

DESCRIPTION:
The RCPU Time Base registers may become corrupted if a new value is written (with a mttbl or mttbu instruction) to the Time Base Upper (TBU) or Time Base Lower (TBL) registers while the Time Base clock is enabled in the Time Base Control and Status Register (TBSCR[TBE]=1).

WORKAROUND:
Disable the Time Base clock by clearing the Time Base Enable bit in the TBLSCR (TBSCR[TBE]=0) prior to any write to the TBU or TBL registers.

CDR_AR_287 Customer Erratum USIU.CDR3UBUS_10_1

USIU: System to Time Base frequency ratio must be greater than 4

DESCRIPTION:
The Time Base and Decrementer may not count properly if the ratio of the System clock to Time Base Clock is 4 or less.

WORKAROUND:
Keep the ratio of the System Clock to the Time Base clock above 4. Always set SCCR[TBS] = 1 when running on the limp clock. Refer to manual dated on or after May 2003.

CDR_AR_479 Customer Erratum USIU.CDR3UBUS_10_1

USIU: The MEMC does not support external master burst cycles

DESCRIPTION:
The MTS function of the Memory Controller (MEMC) will not work properly to control external devices when an external master initiates a burst.

WORKAROUND:
Use external logic to control devices which can have burst accesses from multiple masters. Refer to manual dated on or after May 2003.

CDR_AR_868 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Do not rely on censorship to prevent access on parts with internal Flash

DESCRIPTION:
Under certain conditions, the flash censorship mechanism can be over-ridden (i.e. loads from flash will return the correct data). This does not apply to parts that do not have internal flash memory.

WORKAROUND:
Do not depend on censorship mechanism to prevent access to the internal flash.

CDR_AR_1135 Customer Erratum USIU.CDR3UBUS_10_1

USIU: Disable USIU burst in debug mode if READI R/W feature is used

DESCRIPTION:
If the RCPU is in debug mode and USIU burst mode is enabled (SIUMCR[BURST_EN]=1), READI R/W accesses may cause the RCPU to stop fetching instructions. The device must be reset before the RCPU will fetch and execute instructions.

WORKAROUND:
Use a BDM debugger or when using a Nexus debugger, disable the USIU burst when debugging (SIUMCR[BURST_EN]=0). Alternately, debuggers could disable the USIU burst when entering debug mode (and re-enable upon exiting debug mode) before using READI R/W accesses (i.e. with BDM messages), or the debugger could use BDM messages to perform all read/write accesses instead of using READI R/W accesses.

CDR_AR_1152 Customer Erratum USIU.CDR3UBUS_10_1

USIU: PORESET must always be asserted before the 2.6V supplies reach 0.5V

DESCRIPTION:
When exiting low power modes where the 2.6V supplies (VDD, QVDDL, NVDDL and VDDSYN) are off (Power-down and SRAM Standby modes), correct operation cannot be guaranteed if the 2.6V supplies are above 0.5V before PORESET is asserted. For example, the CALRAM or flash contents may be corrupted.

WORKAROUND:
Ensure PORESET is asserted before ramping the 2.6V supplies above 0.5V in any power-up sequence.

CDR_AR_1154 Customer Erratum USIU.CDR3UBUS_10_1

SIU: RTSEC register not documented; May affect the initial increment of the RTC

DESCRIPTION:
The Reference Manuals have an incomplete statement in the description of the Real-Time Clock register (RTC). In addition, the reserved Real-Time Clock Predivider Register (RTSEC) is not documented and may affect the initial increment of the RTC (seconds) counter. In the Reference Manual, the statement "A write to the RTC resets the seconds timer to zero." is incorrectly worded. A better statement that fully describes the this action would be: "A write of 0 to the RTC must be performed to reset the RTC (seconds) timer to zero." The RTSEC register is the predivider to the RTC (seconds) timer. The RTC, the RTSEC, and the Real Time Clock Alarm (RTCAL) registers, as well as the Real-Time Clock Enable [RTE] and the Real-Time Clock Source [4M] bits of the Real Time Clock Control and Status Register (RTCSC), are not affected by any reset (unchanged) and power up in a random state. This will cause the initial increment of the RTC to be between one system clock and 26143 PITRTCLK clocks. All of these bits and registers must be initialized the first time they are used or if known start points are required. RTSEC is implemented as an 18-bit counter that is left justified in a 32-bit word at address 0x2F_C228. The RTC Alarm itself is always disabled by reset, but RTCAL should be initialized to the desired alarm time, if required, before the Alarm Interrupt Enable (ALE) in the RTCSC is enabled (RTCSC[ALE]=0b1).

WORKAROUND:
To properly initialize the RTC timer to a completely known state with the most accurate startup, the following sequence must be used. 1) The Real-Time Clock Enable [RTE] and the Real-Time Clock Source [4M] bits must be configured in the Real-Time Clock Control and Status Register (RTCSC) after any true power on reset (if KAPWR is powered up) prior use of the RTC. The bits must be initialized since they are not affected by any reset and can be in a random state after the power up. For the most accuracy in the start value of the RTC, RTE should be cleared during this step. For the most accuracy in the start value of the RTC, RTE should be cleared during this step. 2) In order to guarantee that the first increment of the RTC register occurs in approximately 1 second (depending on whether a 4 MHz or 20 MHz crystal is being used), the reserved register RTSEC must also be initialized by writing either 0x0F42_4000 (if using a 4 MHz crystal) or 0x4C4B_4000 (if using a 20 MHz crystal). Alternately, RTSEC could be written to 0 and RTSEC will be updated automatically to these values, but will then immediately (within one PITRTCLK clock) increment the RTC when the RTC is enabled. 3) If a known starting point is desired (like 0), a value must be written to the Real-Time Clock register (RTC). 4) RTE bit should be then be set in the RTCSC register to enable RTC operationNote that the RTCSC, the RTC, and the RTSEC registers are locked following all resets and must be unlocked. The RTSEC can be unlocked by writing 0x55CC_AA33 to address 0x2F_C328.

CDR_AR_865 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not rely on the VDDSRAM Low Voltage Detect Circuit

DESCRIPTION:
At temperatures above room ambient (25C), the VDDSRAM low voltage detect circuit may not always indicate that the VDDSRAM voltage has dropped below the minimum data retention level for the SRAM.

WORKAROUND:
Utilize an external mechanism for detecting when the voltage supplied to the VDDSRAM pin(s) is below the minimum data retention voltage. Refer to manual dated on or after May 2003.

CDR_AR_1113 Customer Information USIU.CDR3UBUS_10_1

USIU: Ensure HRESET/SRESET negation time is longer than 3 CLKOUT periods

DESCRIPTION:
If either HRESET or SRESET are externally re-asserted after a negation time of less than 3 CLKOUT clocks, and after an initial assertion of more than 512 CLKOUT periods, the MCU will remain in that reset until PORESET is applied. In the case of SRESET being the cause, then HRESET can also clear the locked condition. In the case of HRESET being the cause then SRESET will be held asserted internally by the MCU. The SWT (Software Watchdog Timer) will not clear the locked condition.

WORKAROUND:
Do not re-assert HRESET/SRESET within 3 CLKOUT periods of the previous HRESET/SRESET negation; Or apply PORESET.

CDR_AR_833 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not TEA data showcycles or enable data show cycles in single chip mode

DESCRIPTION:
The chip may stop fetching instructions until Reset is asserted if TEA is asserted in data show cycles. This can also occur if the chip is in single chip mode (no databus) since the chip will assert TEA.

WORKAROUND:
Do not assert TEA on data showcycle accesses. Do not program data show cycles when in single chip mode (i.e. no databus is available).

CDR_AR_869 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not enable BRx[SST] with SCCR[EBDF]>0

DESCRIPTION:
When EBDF>0 an external burst access with short setup timing will corrupt any USIU register load/store

WORKAROUND:
Do not enable BRx[SST] while EBDF>0. Refer to manual dated on or after MAy 2003.

CDR_AR_1153 Customer Information USIU.CDR3UBUS_10_1

USIU: Sleep and Deep-Sleep modes require power to all 2.6V supplies

DESCRIPTION:
The reference manual table 8-5 Power Mode Descriptions has incorrect votlage requirements for Sleep and Deep-Sleep modes. Sleep and Deep-Sleep modes require that VDD, QVDDL, NVDDL and VDDSYN all remain powered-up.

WORKAROUND:
Maintain power to all 2.6V supplies during Sleep or Deep-Sleep low power mode.

CDR_AR_389 Customer Information USIU.CDR3UBUS_10_1

Little Endian modes are not supported

DESCRIPTION:
The little Endian modes are not functional.

WORKAROUND:
Do not activate little endian modes. The reference manual will be updated to remove all little endian mode references.

CDR_AR_1109 Customer Information USIU.CDR3UBUS_10_1

USIU: Do not write zero value to the SYPCR[BMT]

DESCRIPTION:
If the BMT (Bus Monitor Timing) field of the SYPCR register is written as zero, the external bus activity may not be available after SRESET assertion even if the bus monitor is disabled by BME bit. The MCU will assert TEA which will terminate any external bus cycle with a data error.

WORKAROUND:
Always write a non-zero value to the BMT field of the SYPCR register.

CDR_AR_1120 Customer Information USIU.CDR3UBUS_10_1

USIU: Interrupt Controller may generate vector 0x0 or has no request indication

DESCRIPTION:
When software masks interrupt requests, clears interrupt flags, stops or disables a module, or masks or changes interrupt logic in the UIMB or the USIU interrupt controller while MSR[EE] = 1, the interrupt request may disappear during or after the RCPU has acknowledged the external interrupt exception. It may also occur after re-enabling interrupts in the RCPU. This may cause the following: 1. When external interrupt relocation is enabled, the BBC may issue a vector offset of 0x0. 2. The SIPEND registers will not contain set bits, and if the service routine polls for a set bit it may hang. 3. The SIVEC register may contain a value of zero which could cause software to branch to an unmapped location.

WORKAROUND:
Follow the workarounds in AR_214, however, note that a time delay is required prior to re-enabling interrupts. Before clearing an interrupt related register, ensure that MSR[EE] = 0. Expect a vector offset of 0x0 if an interrupt is cleared or disabled while MSR[EE] = 1. This vector should be handled as if no interrupt has occurred, i.e. perform an RFI. After clearing an interrupt source, sufficient time must occur before re-enabling interrupts in the RCPU. This time should take longer than the time needed for a load of the same register that was just cleared. If unsure, include this load instruction before the instruction that re-enables interrupts in the RCPU. Refer to manual dated on or after May 2003.

CDR_AR_1137 Customer Information USIU.CDR3UBUS_10_1

USIU: RSR[LLRS] can be set even though no loss of lock reset has occurred

DESCRIPTION:
If the Loss of Lock Reset Enable bit in the PLPRCR register is set when the PLL Multiplication or Division Factor value is changed (PLPRCR[MF] or PLPRCR[DIVF]), the Loss of Lock Reset Status bit in the RSR register will be set (RSR[LLRS] = 1), even though a reset does not occur.

WORKAROUND:
Enable PLPRCR[LOLRE] after setting PLPRCR[MF] and PLPRCR[DIVF] values, or if PLPRCR[LOLRE] is already enabled, clear RSR[LLRS] after changing the value of PLPRCR[MF] or PLPRCR[DIVF].

CDR_AR_1155 Customer Information USIU.CDR3UBUS_10_1

SIU: TEA for external access must be negated within 1 system bus clock

DESCRIPTION:
When accessing external memory and the SIU bus monitor terminates the cycle with a Transfer Error Acknowledge (TEA), the SIU may produce unexpected results on subsequent accesses to the SIU address space, including SIU internal registers reads. This condition occurs when the TEA signal (pin) is not negated within 1 system clock of the time that the MCU stops asserting the TEA signal. While TEA is asserted by the MCU, it must be negated by the required external pull-up resistor. While the TEA negation requirement (1 clock) is documented in the Reference Manual, it may not be obvious that internally terminated accesses of an external memory space require the use of the external pull-up resistor. The value of the resistor should be small enough to pull the TEA line up to VIH level faster than one system clock and depends on the TEA line/board wire capacitance. Circuitry inside the MCU generates an actively driven TEA for accesses to internal non-existent memory spaces and does not rely on the external pull-up resistor to negate the cycle.

WORKAROUND:
Insure that the external pull-up resistor on the TEA pin is sufficient to negate TEA within one system clock. A value of 1K is recommended.