TRANSPORTATION SYSTEMS GROUP
CUSTOMER ERRATA AND INFORMATION SHEET
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MPC555.A

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DETAILED ERRATA DESCRIPTIONS

CDR_AR_252 Customer Erratum MPC555.A

Censorship has been disabled within the CMF

DESCRIPTION:
The censorship mode for the CMF modules has been disabled. The value of the CMF Censor bits will not provide any protection of the contents of the CMF memory array.

WORKAROUND:
To ensure similar behavior on future revisions with censorship enabled, boot code residing within the CMF flash module should set the ACCESS bit.

CDR_AR_313 Customer Erratum MPC555.A

Reduce temperature, frequency, and/or increase voltage to ensure D8/D24 on IMB

DESCRIPTION:
IMB data bits 8 and 24 may be erroneously be set to 0, when they should be 1, when the part is run at 40 Mhz, at certain temperature and voltage combinations. This failure only occurs when accessing data across the IMB, with specific data patterns (where adjacent bits are 0, and bit 8/24 should be 1).

WORKAROUND:
Increase the supply voltage vddi, reduce the operating temperature, and / or drop frequency. For a 40MHz part, the IMB should be operated athalf frequency.

CDR_AR_226 Customer Erratum MPC555.A

Part number in IMMR is 0x04, and will change to 0x30. Mask number is 0.

DESCRIPTION:
Part Number in IMMR is incorrectly 0x04 and will be changed in a future revision to 0x30. The mask number for this revision is 0.

WORKAROUND:
Write software so that both part number values are identified as the MPC555 device.

CDR_AR_1082 **Customer Erratum** **MPC555.A**

TPU ROM: Channels with the COMM ROM function affect other channels

DESCRIPTION:
The TPU COMM ROM Function causes problems in other channels. When the Host Service request is set to 0b11, all channels that do not use the COMM function will be forced to outputs and a random state will be selected.

WORKAROUND:
Either: 1) Re-initialize all other channels after the COMM function has been initialized; or 2) If a fixed COMM TPU function is required, download an updated TPU ROM image into the DPTRAM and use the TPU in emulation mode.

CDR_AR_382 **Customer Information** **MPC555.A**

AC timing changes

DESCRIPTION:
The AC timing specifications used for production screening have been relaxed. Some of these changes will be made permanent. AC specifications: 7, 7a, 7b are 5ns (were 7ns). AC specifications: 8, 8a, 8b, 11 are 15ns (were 13ns). AC specification 15 is 10ns (was 9.75ns). AC specification 19 max is 15ns (was 14ns). AC specification 20 max is 9ns (was 8ns). AC specification 22 is 9ns (was 8ns). AC specifications 28, 29 are 14ns (were 7ns). AC specification 23 is 1ns minimum (was 2ns).

WORKAROUND:
Ensure external devices are matched to these specifications.

CDR_AR_441 **Customer Information** **MPC555.A**

Updated Operating Current Projections

DESCRIPTION:
The operating current specification is listed as TBD in version 2.1 of the electrical specification. The estimated currents in Addendum 2 are outdated. The currents listed below are the design targets, and will be updated and become part of the specification when final silicon is fully characterized.

WORKAROUND:
Projected Average Operating Current at 40MHz, 3.6V, 150C, expanded mode for each power supply: VDDI+VDDL 230mA, KAPWR 5.0mA, VDDSRAM 5.0 mA, VDDSYN 10mA, VDDF 22mA, VDDA 5.0mA, VDDH(5V IO) 25.0mA, VPP 30.0mA/module being programmed/erased. NOTE: In the above projections, some of the current allocated to VDDSRAM and VDDF may be consumed via VDDI, causing IDDI to be larger than the above projection. NOTE: As shown in the above numbers, VDDSRAM should be capable of supplying operating current -- a suggested connection is shown in Figure 8-11 External Power Supply Scheme of the MPC555 User’s Manual.

CDR_AR_851 Customer Information **MPC555.A**

Documentation: COLIE is bit 10 of COLIR Register

DESCRIPTION:
The COLIE (Change of Lock Interupt Enable) bit was incorrectly listed as bit 9 of the COLIR register. The correct location is bit 10.

WORKAROUND:
Software should be updated to reflect the proper bit location. Refer to Reference Manuals dated October 15,2000 or later for the correct bit location.

CDR_AR_1067 Customer Information **MPC555.A**

MPC555: Errata Lists for discontinued revisions no longer updated

DESCRIPTION:
As of October 2002, Errata lists for discontinued versions of the MPC555 will no longer be updated. All revisions 0, A, C, G, and K have been out of production for more than 2 years. New errata that affect these revisions will no longer be updated.

WORKAROUND:
Convert to later versions of the MPC555, either K2, K3 or M.

CDR_AR_212 Customer Erratum **BBC.CDR1UBUS_01_0**

Do not assert SRESET pin without asserting HRESET first

DESCRIPTION:
BBC samples reset configuration using SRESET. If only SRESET is asserted, reset configuration bits in BBC may be corrupted. Reset configuration bits in BBC include reserve bits, and also the exception table relocation feature. Improper initialization can cause not fetching code out of reset.

WORKAROUND:
Never assert SRESET without first asserting HRESET.

CDR_AR_213 Customer Erratum **BBC.CDR1UBUS_01_0**

Ignore redundant instruction show cycles

DESCRIPTION:
Instruction Show cycle may be repeated several times.

WORKAROUND:
Ignore the extra show cycles. This is a rare situation.

CDR_AR_215 Customer Erratum **BBC.CDR1UBUS_01_0**

Use same IMPU protection for external and internal regions with same offset

DESCRIPTION:
When accessing any address in the MPC555 address space, the protection attribute will be determined as if address[7:9] were replaced by IMMR[ISB]. It is not possible to alter protection attributes (User/supervisor, access, and guarded) where address[7:9] is not the same as IMMR[ISB]. When accessing external address to MPC555 space region then the protection attributes are matched as if the address was in the internal range.

WORKAROUND:
Use the same IMPU protection for all address spaces.

CDR_AR_261 Customer Erratum **CMF.192KB_CDR1UBUS_01_1**

Boot from internal flash at low frequency (~ 10 MHz or less)

DESCRIPTION:
The CMF does not negate the data error signal quickly enough. As a result, the CMF may inadvertently data error accesses. This makes it difficult to boot from flash except at low frequencies. In addition, access to the CMF immediately following data errored accesses may result in a data error. When the error occurs, the core should take a machine check exception. If the machine check is also fetched from flash, the part may require reset to recover.

WORKAROUND:
Boot from the CMF using a low frequency clock. Avoid accessing the CMF immediately after a data errored bus cycle. Avoid software watchdog resets when running at full frequency and booting from the CMF module.

CDR_AR_636 Customer Erratum **CMF.192KB_CDR1UBUS_01_1**

CMF: Program at reduced temperature and voltage ranges

DESCRIPTION:
There may be insufficient program margin to be able to correctly read all bits of the array at cold with 3.0Vdd if the part was programmed at hot.

WORKAROUND:
Workarounds in order of effectiveness: First, reduce temperature while programming. Second, reduce Vpp while programming. Third, increase VDD while programming and reading. During programming, limit the maximum ambient temperature to 85C, and Vdd to 3.3V +/- 5%. This allows sufficient margin to read flash cells over the entire specified temperature and voltage ranges. By further restricting Vdd to 3V +/- 5% during all operations (including flash read), the maximum programming temperature may be increased to 90C with sufficient program margin to operate over the entire temperature range.

CDR_AR_249 Customer Erratum **CMF.192KB_CDR1UBUS_01_1**

Do not use reset configuration word from the internal flash

DESCRIPTION:
The device cannot boot using the reset configuration word from the internal flash register (CMFCFIG). If the internal value is used, the device will be unable to boot, and will be unable to accessed via the development port.

WORKAROUND:
Do not program CMFCFIG[20] (HC) to 0. Either(1) Use external data bus pins for reset configuration: Hold rstconf_b low during reset, and supply the configuration word on the data bus. To boot from internal flash (CMF) hold d[20] high during reset to enable the CMF.or (2) Use internal default constant reset configuration word; note that this prevents booting from CMF.

CDR_AR_250 Customer Erratum **CMF.192KB_CDR1UBUS_01_1**

Ensure multiple pulses in program/erase sequence

DESCRIPTION:
On the 1st program/erase pulse, HVS may not set.

WORKAROUND:
Follow the specified program/erase sequence in the user manual. This will result in one additional program/erase pulse.

CDR_AR_279 Customer Information **CMF.192KB_CDR1UBUS_01_1**

CMFCTL register field, CLKPE, definition is changing

DESCRIPTION:
The CLKPE field in the CMFCTL register now has a new definition for PE=0 beginning with CMF_02_0_MODULES revision of the CMF module:CLKPE[0:1]=00 Exponent = 5, CLKPE[0:1]=01 Exponent = 6,CLKPE[0:1]=10 Exponent = 7, CLKPE[0:1]=11 Exponent = 8

WORKAROUND:
Software requires update for the new CLKPE definition.

CDR_AR_101 Customer Information **CMF.192KB_CDR1UBUS_01_1**

Be cautious when terminating flash programming early -- follow users manual

DESCRIPTION:
If the program/erase pulse is terminated early by writing EHV = 0, the programmed/erased data may be corrupted.

WORKAROUND:
Don’t terminate the program or erase cycle early and then immediately read the array. No problem will occur if program/erase sequence as defined in the spec is followed.

CDR_AR_102 Customer Information **CMF.192KB_CDR1UBUS_01_1**

Avoid margin read of flash at wrong time -- follow users manual

DESCRIPTION:
If the first array interlock write is followed on the next clock by an array margin read, the contents in the CMF program page buffer will be corrupted resulting in an unsuccessful program

WORKAROUND:
Follow the program/erase sequence as defined in the spec.

CDR_AR_105 Customer Information **CMF.192KB_CDR1UBUS_01_1**

Avoid margin read of flash at wrong time -- follow users manual

DESCRIPTION:
If margin reads are done in between writes to the same page before a programming, only the first read will return the correct value. The data to be programmed is correct.

WORKAROUND:
Follow the specified program/erase sequence

CDR_AR_268 Customer Erratum **DPTRAM.6K_CDR1IMB3_01_0**

Do not access any DPTRAM control registers in TPU emulation mode

DESCRIPTION:
When the DPTRAM is in TPU emulation mode, the DPTRAM spuriously asserts the TEA signal if HOST tries to access any of its control registers.

WORKAROUND:
Set up all DPTRAM control registers before putting the device in emulation mode. Do not access them upon entering the emulation mode.

CDR_AR_485 Customer Information **DPTRAM.6K_CDR1IMB3_01_0**

Disable of TPU emulation mode while MISC enabled corrupts data in RAM

DESCRIPTION:
If the TPU emulation mode is negated while MISC is enabled, the DPTRAM data may be corrupted.

WORKAROUND:
In test mode / TPU development mode, disable the MISCEN (DPTMCR) before negation of TPEMEM in the TCR. In normal mode, disable MISCEN prior to performing a soft reset of the TPU (TPUMCR2).

CDR_AR_15 Customer Erratum **L2U.CDR1LBUSUBUS_01_0**

Only enter low power mode following a SYNC

DESCRIPTION:
During entry into low power mode, the device can be stalled in a deadlock situation. Only HRESET can cancel this situation.

WORKAROUND:
Write the low power mode command in serialized mode (issue a SYNC command). This will ensure that there are not any pending accesses in Lbus or in Ubus.

CDR_AR_142 Customer Erratum **L2U.CDR1LBUSUBUS_01_0**

Leave L-bus show cycles disabled

DESCRIPTION:
A data showcycle may be missed or the data from previous showcycle may be corrupted for U-bus pipelined showcycles. This may cause the device to hang. Instruction showcycle is not affected by this errata. Data showcycle cannot be done through L-bus. However, data showcycle through U-bus is not affected.

WORKAROUND:
Either (1) disable L-bus showcycle LSHOW[0:1](L2U_MCR)=00, or (2) operate in serialized mode by leaving SER (ICTRL[29]) as ’0’.

CDR_AR_91 Customer Erratum **LRAM.10KA_CDR1LBUS_01_0**

Insert additional machine check handler at h1400

DESCRIPTION:
The 10K RAM issues the wrong exception request for accesses which cause an exception. The processor will execute a dsi exception (vector to h1400) instead of a machine check exception (vector to h0200).

WORKAROUND:
Make sure that the code at vector h1400 will handle the exception.

CDR_AR_93 Customer Erratum **LRAM.10KA_CDR1LBUS_01_0**

Avoid accessing holes in the internal memory map

DESCRIPTION:
Accesses to the unimplemented 6K hole in the memory map left by the 10K RAM will not showcycle. The access will still cause an exception, but may not be seen by development hardware.

WORKAROUND:
None.

CDR_AR_445 Customer Erratum **MIOS1.CDR1IMB3_01_0**

Potential trap state in MIOS MDASM in OPWM mode.

DESCRIPTION:
A trap state is entered when a value of MDASMBR is written in OPWM mode, to a value which is out of the counter bus range. For example, if the modulus value of the MCSM driving the counter bus is $FF00 and if MDASMBR is written to a value less than $FF00, then a match is never made on channel B hence a B1 to B2 transfer never occurs. To get out of the trap, the MDASM mode should be reset back to idle.

WORKAROUND:
Ensure that the software never writes MDASMBR (in OPWM mode) to a value which is less than the MCSMMOD value.

CDR_AR_468 Customer Erratum **MIOS1.CDR1IMB3_01_0**

Configure MIOS/VF/VFLS pins as all MIOS or all VF/VFLS

DESCRIPTION:
The MIOS VF/VFLS multiplexer must not be individually programmed. These pins can be configured either as VF/VFLS or as all MIOS pins. Do not configure bit[0:1] of the MIOS1TPCR register as 2’b01 or 2’b10.

WORKAROUND:
Whenever the user wishes to configure the MIOS/VF/VFLS pins, software should write 2’b11 or 2’b00 to bit[0:1] of the MIOS1TPCR register. This will allow the pins to be either all MIOS functions or all development support functions. The pins should never be configured separately.

CDR_AR_295 Customer Erratum **MIOS1.CDR1IMB3_01_0**

Do not write data value to MIOS MDASMAR or MDASMBR when in input mode

DESCRIPTION:
The MDASMAR or MDASMBR registers can be loaded by a write with the data bus value or can be loaded with the counter bus value when a counter bus capture happens. Normally, software should not write data when in an input mode. However no hardware exists to prevent simultaneous loads to happen. As a result, during a simultaneous load, a driver conflict occurs and the register bit contents will be indeterminate. The specification does not define what happens in these cases.

WORKAROUND:
When in one of the input modes, do not write a data value to the MDASMAR or MDASMBR.

CDR_AR_296 Customer Erratum **MIOS1.CDR1IMB3_01_0**

Do not use the value in the MIOS DASM B register when in input capture mode

DESCRIPTION:
In DASM IC mode the captured data is not transferred to the B1 register, as it is in the IPM mode. This is contrary to the MIOS specification which says that DASM IC mode and IPM mode should be identical except for when the flag bit will be set. This issue does not affect standard single input captures.

WORKAROUND:
For a period measurement the IPM mode should be used. For a standard input capture function use the IC mode and ignore MDASMBR.

CDR_AR_443 Customer Erratum **MIOS1.CDR1IMB3_01_0**

MIOS: Do not write data into the MDASMBR when in an input mode.

DESCRIPTION:
The MDASMBR register can be loaded via a write from the IMB, from the counter bus OR from a transfer from the MDASMAR to the MDASMBR register. The transfer from MDASMAR to MDASMBR only happens in input modes, when the software should not normally write into MDASMBR. However, no hardware exists to prevent a simultaneous transfer from MDASMAR and write to MDASMBR. As a result, during a simultaneous transfer and write, the resulting data in MDASMBR will be undefined. The specification does not define what happens in this case.

WORKAROUND:
When in an input mode, do not write to MDASMBR.

CDR_AR_444 Customer Erratum **MIOS1.CDR1IMB3_01_0**

MIOS: Warning in MDASM OPWM mode when MDASMAR = MDASMBR.

DESCRIPTION:
In OPWM mode when a comparison occurs simultaneously on register A and B (i.e. they have the same value stored), the pin is reset or stays reset. The specification states that the transfer between B1 and B2 should occur when the pin is low. However this is not necessarily the case when a simultaneous A&B compare occurs. If the pin was previously low then the transfer would not happen until after the next compare.

WORKAROUND:
1): Avoid setting MDASMAR = MDASMBR when in OPWM mode. 2): To come out of MDASMAR = MDASMBR when in OPWM mode change the value of MDASMAR first. 3): Be aware that it may take an extra match to update MDASMBR B2 than expected, after a new value is written to MDASMBR B1.

CDR_AR_446 Customer Erratum **MIOS1.CDR1IMB3_01_0**

MIOS: Avoid 100% pulse in MDASM OPWM mode.

DESCRIPTION:
A two cycle system clock "glitch" (to logic "0") may occur when 100% output state is entered in MDASM OPWM mode. 100% pulse is entered by writing B register bit 15 high when using less than 16 bit resolution. The problem occurs only when B register bit 15 is set while the pin is high; the glitch occurs on the next match on the B register.This glitch is only seen the first time a match on B causes 100% mode to be entered. No glitches will be seen on subsequent matches.

WORKAROUND:
- Use the pads with the slow slew rate. Then at 40 Mhz no glitch will be seen on the output pin.- If B register bit 15 is only set while the pin is low then there will not be any glitch on the pad. The change to 100% will occur 2 cycles after the setting of B register bit 15.Invert the polarity of the output. Then setting A=B will cause a 100% pulse. A glitch free 0% pulse is now no longer possible.

CDR_AR_452 Customer Information **MIOS1.CDR1IMB3_01_0**

MIOS: "non-reset" registers are undefined after reset.

DESCRIPTION:
The specification states that many of the MIOS data registers are unaffected by reset. This should really be "undefined" after a reset. Note that after reset all the MIOS submodules are correctly in their idle state with the pads as inputs.

WORKAROUND:
After a reset of the MIOS a full initialization routine should be run, rather than assuming that the same values remain in the MIOS data registers.

CDR_AR_351 Customer Erratum **PKPADRING.CDR1_01_0**

Hreset and Sreset falsely change during poreset and powerdown

DESCRIPTION:
Hreset and Sreset falsely change during poreset and powerdown (KAPWR on and VDD off). Floating controls on the output buffers of the Hreset and Sreset pads cause excessive leakage current which in turn may cause the output value on the pin to change.

WORKAROUND:
Do not rely on the value of Hreset and Sreset when powered-down.

CDR_AR_182 Customer Erratum **PKPADRING.CDR1_01_0**

Minimize resistance between CLKOUT and any loads

DESCRIPTION:
The chips/peripherals which exists on a board with a large resistive paths may receive an inaccurate clock source. The CLKOUT and ENGCLK signals may not reach the full rail if it is driving an RC type load.

WORKAROUND:
Minimize series resistance between the CLKOUT pin and peripheral chips receiving this signal.

CDR_AR_298 Customer Erratum **PKPADRING.CDR1_01_0**

Latch address during address phase of write cycle

DESCRIPTION:
When the databus switches on a write cycle, address lines set to 0 may exceed Vol during the time in which the databus switches. This problem is more likely to occur if the databus is heavily loaded. The impact on a board may be measured by writing $ffffffff followed by $00000000 to an external device, and measuring the address lines.

WORKAROUND:
Reduce loading on the databus and/or latch address during address phase of write cycle or delay chip select/WE assertion until the data phase of the bus cycle.

CDR_AR_127 Customer Erratum **PKPADRING.CDR1_01_0**

Ignore data obtained from JTAG for IRQ6 pin

DESCRIPTION:
JTAG inputs cannot be captured for the IRQ6_b_modck pin.

WORKAROUND:
Ignore data obtained from JTAG for IRQ6_b_modck pin.

CDR_AR_128 Customer Erratum **PKPADRING.CDR1_01_0**

Configure MIOS/VF/VFLS pins as all MIOS or all VF/VFLS

DESCRIPTION:
The MIOS VF/VFLS multiplexer must not be individually programmed. These pins can be configured either as VF/VFLS or as all MIOS pins. Do not configure bit[1:0] of the MIOS1TPCR register as 2’b01 or 2’b10.

WORKAROUND:
Whenever the user wishes to configure the MIOS/VF/VFLS pins, software should write 2’b11 or 2’b00 to bit[1:0] of the MIOS1TPCR register. This will allow the pins to be either all mios functions or all development support functions. The pins should never be configured separately.

CDR_AR_209 Customer Erratum **PKPADRING.CDR1_01_0**

Hysteresis is unavailable on MIOS pins

DESCRIPTION:
Hysteresis is not enabled on the inputs of the MIOS gpio pins.

WORKAROUND:
None

CDR_AR_349 Customer Erratum PKPADRING.CDR1_01_0

Drive 3V inputs to the rail

DESCRIPTION:
The 3v input buffer design does not meet the specified values for VIL/VIH.

WORKAROUND:
Ensure that 3V input signals are greater than 2.2V. Preferably, drive them to the rail.

CDR_AR_454 Customer Erratum PKPADRING.CDR1_01_0

Use external resistors/drivers when using external reset configuration word

DESCRIPTION:
When asserting RSTCONF to direct the MPC555 to sample the reset configuration word from the external data pins, the weak pulldowns on the data pads may not fully discharge the pins during reset. If the data pins were driven high by the MPC555 just prior to the assertion of reset, the weak pulldowns will not be able to discharge the pins due to contention with the P-channel transistor of the output buffer. This transistor is not fully turned off by the pre-driver stage.

WORKAROUND:
Program the internal flash to provide the reset configuration word. Or, use external resistors/drivers to drive all of the configuration word during reset (including bits set to 0) when providing the reset configuration word from external. An external 10K resistor is sufficient to pull a data pin to 0 during reset.

CDR_AR_680 Customer Information PKPADRING.CDR1_01_0

CLKOUT and ENGCLK drive strengths will change

DESCRIPTION:
Beginning with Revision M, the CLKOUT pad driver will be sized to drive loads of 30pf or 90pf, selectable by software. The ENGCLK pad driver will be sized to drive loads of 25pf or 50pf, selectable by software.

WORKAROUND:
Designs with clkout loads between 30pf and 45pf should evaluate setting the clkout driver to the 90pf drive mode. Designs with ENGCLK loads above 25pf should evaluate setting the ENGCLK driver to the 50pf drive mode. Designs with ENGCLK loads above 50pf should reduce the ENGCLK frequency to 10Mhz or below.

CDR_AR_154 Customer Information PKPADRING.CDR1_01_0

0 in the PDMCR sets pads to slow slew rate -- see later versions of users manual

DESCRIPTION:
In the PDMCR register, a value of 0 defines the related pads to be slow slew rate.

WORKAROUND:
Follow the definition given in 3/1/98 or later versions of User’s Manual.

CDR_AR_292 Customer Information PKPADRING.CDR1_01_0

QADC64 Pins have active pull-ups

DESCRIPTION:
The QADC64 port related pads have pull-ups active during reset until PRDS is negated. This description is missing from some versions of the padring specification and the users manual.

WORKAROUND:
Update documentation.

CDR_AR_940 Customer Information PKPADRING.CDR1_01_0

JTAG: Do Not Switch All Pads Simultaneously When JTAG Enabled

DESCRIPTION:
JTAG mode puts all output pins in fast slew rate mode. The power supply pins of the device cannot supply enough current to allow all pins to be changed at the same time in fast slew rate mode. During normal operation, this is not an issue since all pins on the device do not switch at the same time.

WORKAROUND:
When using JTAG, all pins should not be switched simultaneously.

CDR_AR_219 Customer Erratum RCPU.CDR1LBUSIBUS_11_1

Avoid (or fix output from) compilers which generate specific branch sequence

DESCRIPTION:
In the following instance, an instruction may be issued multiple times: When there are three branches in a row in the program flow and the third branch is in a miss-predicted path of the second branch. Then although the third branch is part of predicted path it may be issued from the instruction queue. If this wrong issue happens at the same time that the condition is resolved [causing conditional instructions to be flushed from queue] then earlier instruction[s] are re-issued. Not all compilers can generate this sequence.

WORKAROUND:
Use compiler which does not generate this sequence, and/or inspect code for this sequence. If found: For every conditional branch preceded in program order by a branch: IF the first instruction in a predicted path is a branch AND the first instruction in the non predicted path is NOT branch, THEN change predicted policy [invert y bit in the branch op-code] IF the first instruction in the predicted path is a branch AND the first instruction in the non predicted path is ALSO branch, THEN insert a non branch instruction before the branch on the predicted path. Another alternative is to insert an ISYNC instruction between the instruction generating the condition and the conditional branch.

CDR_AR_1019 Customer Erratum RCPU.CDR1LBUSIBUS_11_1

RCPU: Don’t execute overflow type before update type MUL/DIV instruction

DESCRIPTION:
When an integer overflow type non multiply or divide instruction (designated by an ’o’ in the instruction mneumonic, such as addo) starts to execute before a previously started Condition Register 0 (CR0) update type integer multiply or divide instruction (designated by a ’.’ in the instruction mneumonic, such as divw.) completes, the CR0[SO] bit may be wrongly updated from the XER[SO] bit earlier changed by the overflow type instruction. For example, instruction sequence "divw. Rx,Ry,Rz , subfo Rt,Ru,Rv" may cause this problem. It does not happen if the overflow type instruction is also a CR0 update type instruction (designated by ’o.’ in the instruction mneumonic, such as addo.), or if register dependencies exist.

WORKAROUND:
Do any one of the following: 1) Keep a gap of at least 1 instruction between a CR0 update type integer multiply instruction and an overflow type instruction or a gap of 4 integer or 6 other instructions between a CR0 update integer divide instruction and an overflow type instruction; 2) Use the CR0 update type for both instructions; 3) Run the RCPU in serialized mode; 4) Place a "sync" instruction between the integer multiply/divide instruction and the overflow type instruction; 5) Don’t use the update form of integer multiply or divide instructions; or 6) Don’t use overflow type integer instructions. (Note: most compiler vendors do not generate the error case.)

CDR_AR_1077 Customer Erratum RCPU.CDR1LBUSIBUS_11_1

RCPU: Do not run multi-master compressed application with Show Cycles and BTB

DESCRIPTION:
If instruction show cycles (ICTRL[ISCT_SER] not equal to 0x7) and BTB are enabled in a compressed application with interrupts and another master (READI or External Bus master) initiates internal accesses on UBUS, the RCPU may execute incorrect instructions.

WORKAROUND:
Do not enable instruction show cycles together with BTB while running compressed application with interrupts if a UBUS master (READI or External Master) other than the RCPU or the L2U operated by the RCPU, accesses MCU internal resources through the UBUS.

CDR_AR_218 Customer Erratum RCPU.CDR1LBUSIBUS_11_1

Byte or half-word breakpointing of store instructions is unreliable

DESCRIPTION:
When breakpoint on data elements of size of byte or half word is programmed for store instructions, (1) Breakpoint might be detected when it should not. (2) Breakpoint might not be detected when it should. This might happen when either byte or half-word size of data are programmed to be detected, and this data matches some other portion of the register that is currently being stored in memory by store byte or half-word instruction. The fault occurs when the previous Load-Store instruction address’s LSB is different from the current one’s.

WORKAROUND:
None.

CDR_AR_1076 Customer Erratum RCPU.CDR1LBUSIBUS_11_1

RCPU: Treat VF queue flush information value of 6 as 2

DESCRIPTION:
When the RCPU fetches instructions from zero wait state slaves on UBUS (Internal flash or SIU when in enchanced burst mode), the VF queue flush information may have the reserved value of 6.

WORKAROUND:
If a VF instruction queue flush value of 6 is shown on the VF pins, tools should treat this value as 2 for program tracking purposes.

CDR_AR_907 Customer Information RCPU.CDR1LBUSIBUS_11_1

RCPU: Issue ISYNC command when entering debug mode

DESCRIPTION:
If the ICTRL[28] bit is set (non-serialized mode) then the RCPU issues two instruction fetch requests into the instruction pipeline after entering debug mode. The debug port and the debug tool may get confused when processing an "mtspr DPDR,Rx" instruction. The debug tool loses synchronization with debug port and receives the wrong data for the "Rx" register. The typical case is when the debug tool tries to save scratch registers or read the debug mode cause.

WORKAROUND:
Issue an ISYNC instruction to the debug port prior to any other instructions when the RCPU enters debug mode after running code.

CDR_AR_440 Customer Information RCPU.CDR1LBUSIBUS_11_1

RCPU: Execute any IMUL/DIV instruction prior to entering low power modes.

DESCRIPTION:
There is a possibility of higher than desired currents during low power modes. This is caused by a possible contention in the IMUL/DIV control area. This contention may only exist prior to the execution of any IMUL/DIV instruction.

WORKAROUND:
Execute a MULLW instruction prior to entering into any low power mode (anytime after reset, and prior to entering the low power mode).

CDR_AR_211 Customer Information RCPU.CDR1LBUSIBUS_11_1

Do not set breakpoint on mtspr ICTRL instruction

DESCRIPTION:
When a breakpoint is set on an "mtspr ICTRL,Rx" instruction and the value of bit 28 (IIFM) is 1, the result will be unpredictable. The breakpoint can be taken or not on the instruction and value of the IFM bit can be either 0 or 1.

WORKAROUND:
Do not put a break point on mtspr ICTRL, Rx instruction when bit 28 of Rx is set to a 1.

CDR_AR_214 **Customer Information** **RCPU.CDR1LBUSIBUS_11_1**

Only negate interrupts while the EE bit (MSR) disables interrupts

DESCRIPTION:
An IRQ to the core, which is negated before the core services it, may cause the core to stop fetching until reset.

WORKAROUND:
Interrupt request to the core should only be negated while interrupts are disabled by the EE bit in the MSR. Software should disable interrupts in the CPU core prior to masking or disabling any interrupt which might be currently pending at the CPU core. For external interrupts, it is recommended to use the edge triggered interrupt scheme. After disabling an interrupt, sufficient time should be allowed for the negated signal to propagate to the CPU core, prior to re-enabling interrupts. For an interrupt generated from an IMB module, 6 clocks is sufficient (for IMBCLK in 1:1 mode).

CDR_AR_563 **Customer Erratum** **QADC64.CDR1IMB3_01_0**

QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.

DESCRIPTION:
This problem does not affect parts that do not run IACK cycles (i.e. RISC CPUs). The Common BIU state machine, used by the QSM/QSMCM/QADC64, mis-tracks an IACK cycle if an interrupt is issued while an IACK cycle for the same level is in progress. In this case, the next access on the IMB3 will be corrupted by the QSM/QSMCM/QADC64. On CPU32 based parts (or CPU32X parts where the FASRAM is not used for the stack), the first access after an IACK cycles is the stacking of the vector offset The risk to the system by corrupting this stacked value is very low, since it is not used by the processor or most interrupt service routine software. On CPU32X based parts which have the stack located in the FASRAM, however, the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error.

WORKAROUND:
Workarounds exist for both CPU32 and CPU32X based parts. On CPU32 based parts the first access after an IACK cycles is the stacking of the vector offset The risk to the system by corrupting this stacked value is very low, it is not used by the processor. On CPU32X based parts which have the stack located in the FASRAM the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error. The suggested workarounds for the QSM/QSMCM/QADC64 are listed below. For CPU32 based parts: - assign the QSM/QSMCM/QADC64 it’s own interrupt levels separate from any other modules if the corruption of the vector offset in the stack frame is an issue. For CPU32X based parts: (a) assign the QSM/QSMCM/QADC64 its own interrupt levels separate from any other module in the system or (b) move the stack out of the FASRAM.

CDR_AR_271 Customer Erratum QADC64.CDR1IMB3_01_0

Loss of Accuracy upon current injection to analog pins

DESCRIPTION:
QADC64 conversion results are affected when the immediately following channel undergoes a current injection condition. When a channel being converted experiences current injection, the prior conversion will be affected (regardless of which channel was the prior conversion). Up to 7 counts of deviation are seen at 1 ma of injection. At ˜20 ua of current injection, there is a one count deviation.

WORKAROUND:
Convert the prior channel twice, ignoring the 2nd result.

CDR_AR_754 Customer Erratum QADC64.CDR1IMB3_01_0

QADC64:Do not use queue1 in external gated mode with queue2 in continuous mode.

DESCRIPTION:
When the gate for queue1 opens when queue2 is converting the last word in its queue, queue1 completion flag will immediately set and no conversions will occur. Queue1 will remain in a hung state for the duration of the gate (no conversions will occur regardless of how long the gate is open). This failure will only occur when the QADC64 is configured with queue1 in external gated mode (continuous or single scan) and queue2 is in continuous mode. The failure mode can be detected if it is known that the gate for queue 1 is shorter than the length of the queue, and the completion flag becomes set. The failure can also be detected as follows: software writes invalid results to the result register (3ff when it is known the input will never go to full scale); after the gate has closed if the invalid result is still in result space 0, then the failure has occured.

WORKAROUND:
There are 2 workarounds: (1) Do not use queue 2 if queue1 is set for external gated mode. Or, (2) SETUP: (a) queue 2 mode : ’Interval Timer Single-Scan Mode’ (MQ2 = 11000) so the interval is (1/(2MHz/2048)) = 1.024ms (b) Pause bit set in CCW60 (c) Pause bit set in CCW61. FUNCTIONALITY: SSE2 bit gets set, the timer starts, and the internal trigger comes after 1.024ms. queue2 will then start converting and will continue until it sees the pause bit in CCW60. So, a reset could occur every 2ms, and the SSE2 bit should be set allowing the queue to begin again never having reached an end of queue. If ’Task jitter’ does occur, and the queue does not get reset before another internal trigger is created, then it will do a one word conversion and immediately pause again due to the pause bit set in CCW61. Even if there is enough ’Task jitter’ to allow this sub-queue to begin, it will be paused after only one conversion and will not reach the end of queue. Finally, it is assumed that it would not be possible to have enough uncertainty for another level of sub-queues to be needed.

CDR_AR_89 Customer Erratum **QADC64.CDR1IMB3_01_0**

Mask off address field data during QADC port register reads in external mux mode

DESCRIPTION:
In external multiplexor mode, reads of the QADC64 port register may return indeterminate values for field MA[2:0]. This occurs when the converter fetches a new command control word at the same time the port register is read. The address has not stabilized for the read. Note: No adverse affect is seen on the external address pins.

WORKAROUND:
This minor problem can be avoided by the customer by masking off the address field data during the port register reads. To determine the current mux address, read the CCW.

CDR_AR_143 Customer Erratum **QADC64.CDR1IMB3_01_0**

Use software to disable QADC external gated single scan mode at end of queue

DESCRIPTION:
In the QADC, the SSE-bit is not cleared in external gated single scan mode when the gate closes before queue1 completes, allowing further gated triggers to occur. Pause flag correctly asserts indicating incomplete queue.

WORKAROUND:
Enable the PF1 flag assertion to interrupt software and disable the mode upon gate closure.

CDR_AR_144 Customer Erratum **QADC64.CDR1IMB3_01_0**

In external gated continuous scan mode of the QADC, avoid use of CCW-EOQ

DESCRIPTION:
In the QADC64, CCW-EOQ is not recognized in external gated continuous scan mode. The other 2 EOQ conditions, BQ2 encountered, and end of physical queue, operate correctly.

WORKAROUND:
Utilize 1 of the other 2 EOQ conditions: BQ2 encountered, or end of physical queue.

CDR_AR_145 Customer Erratum **QADC64.CDR1IMB3_01_0**

Do not program QADC64 QACR2 BQ2 field to a value greater than 63

DESCRIPTION:
Programming BQ2 pointer in QACR2 outside the implmented CCW table memory and starting Q2 results in a Q2 false start. It goes active and does not correctly process. It should not go active.

WORKAROUND:
Do not program BQ2 outside the implemented CCW table memory and start the Q2.

CDR_AR_307 Customer Erratum **QADC64.CDR1IMB3_01_0**

Program the QADC64 end of Q2 in software cont mode with CCW-EOQ

DESCRIPTION:
Programming Q2 for software continuous mode and using the end of the result table for the end of queue causes the Q2 to stall after the first pass.

WORKAROUND:
Program Q2 for software continuous mode using a CCW-EOQ condition to end the queue.

CDR_AR_421 Customer Erratum **QADC64.CDR1IMB3_01_0**

QADC64: Don’t switch to software triggered continuous scan after completing Q1.

DESCRIPTION:
In the case when application software switches Q1 to software triggered continuous scan mode after Q1 completes a single scan where BQ2 provides the end of queue, an indeterminate response results.

WORKAROUND:
Don’t select software triggered continuous scan after using Q1.

CDR_AR_422 Customer Erratum **QADC64.CDR1IMB3_01_0**

QADC64: Do not rely on set of TOR1 in external gated continuous scan mode

DESCRIPTION:
In External Gated Continuous Scan mode: If the external gate is negated during the last conversion (after the ccw has started, but before the result is converted) the TOR1 flag will not set.

WORKAROUND:
Control software needs to reflect the following: In external gated continuous scan mode, setting of TOR1 is guaranteed only if the gate remains open thru the completion of the last conversion in queue1.

CDR_AR_419 Customer Information **QADC64.CDR1IMB3_01_0**

QADC64: False trigger upon configuration (depends on chip configuration)

DESCRIPTION:
In some implementations, the QADC64 may have a false trigger upon entering an external trigger mode. The potential for a false trigger only exists on QADC64’s which are implemented with trigger pin(s) muxed through PortA[3 or 4]. If the triggers have dedicated pins, then no difference exists between the value on the pin and the value between the pad and the module.The false trigger can result when an edge triggered mode is enabled and the logic value at the pin and the previously latched value in the pad are not equal.

WORKAROUND:
A port data register read may be performed prior to entering an external trigger mode to ensure that the latched value between the pad and the module matches the value on the pin. This read ensures that an edge will not be caused by the latch in the pad becoming transparent when the external trigger mode is entered. This issue does not exist on the following parts: MPC555.

CDR_AR_420 Customer Information QADC64.CDR1IMB3_01_0

QADC64: Don’t change BQ2 with a set of SSE2 without a mode change.

DESCRIPTION:
Changing BQ2 and setting SSE2 with no mode change will cause Q2 to begin but not recognize the change in BQ2. Further, changes of BQ2 after SSE2 is set, but before Q2 is triggered are also not recognized. All other sequences involving a change in BQ2 are recognized.

WORKAROUND:
Be sure to do mode change when changing BQ2 and setting SSE2. Recommend setting BQ2 first then setting SSE2.

CDR_AR_435 Customer Information QADC64.CDR1IMB3_01_0

QADC64: TOR1 flag operates in both single and continuous external gated modes.

DESCRIPTION:
TOR1 response was added to QADC64 to provide an indication of more than 1 pass through queue1. It was described in the specification as a continuous mode only flag. The flag is however, operating in both single and continuous modes.

WORKAROUND:
None. Simply expect the flag to respond in both single scan and continuous scan modes.

CDR_AR_290 Customer Erratum QSMCM.CDR1IMB3_01_0

QSMCM Errata ONLY if QSMCM used on a CPU16/32/32X MCU

DESCRIPTION:
Wrong QSMCM interrupt source for IACK cycle may be returned on MODULAR parts. Bit 0 of the vector number is erroneously returned as a 1 for an SCI interrupt. It should be 0. (Same as CDR_AR:205)

WORKAROUND:
Interrupt handlers for QSMCM could poll status registers to determine actual source of the interrupt.

CDR_AR_294 Customer Erratum QSMCM.CDR1IMB3_01_0

Do not use QSMCM SCI1 Queue

DESCRIPTION:
The QSMCM RXTX queue decodes to multiple addresses. Writes to any location on the IMB which match A[8:0]=$02C:06A will also result in the corresponding location in the RXTX queue being written.

WORKAROUND:
Do not use the SCI queue for SCI transmission or reception. Alternatively, ensure that no IMB writes occur to locations $XXXXX02C:XXXXX06A, $XXXXX22C:XXXXX26A, $XXXXX42C:XXXXX46A, $XXXXX62C:XXXXX66A, $XXXXX82C:XXXXX86A, $XXXXXA2C:XXXXXA6A, $XXXXXC2C:XXXXXC6A, $XXXXXE2C:XXXXXE6A while the SCI1 RX or TX queue is in use. Refer to the full chip memory map to determine which IMB registers reside in the conflicting ranges.

CDR_AR_563 Customer Erratum QSMCM.CDR1IMB3_01_0

QSM/QSMCM/QADC64 corrupts data after an IACK cycle in CISC parts.

DESCRIPTION:
This problem does not affect parts that do not run IACK cycles (i.e. RISC CPUs). The Common BIU state machine, used by the QSM/QSMCM/QADC64, mis-tracks an IACK cycle if an interrupt is issued while an IACK cycle for the same level is in progress. In this case, the next access on the IMB3 will be corrupted by the QSM/QSMCM/QADC64. On CPU32 based parts (or CPU32X parts where the FASRAM is not used for the stack), the first access after an IACK cycles is the stacking of the vector offset The risk to the system by corrupting this stacked value is very low, since it is not used by the processor or most interrupt service routine software. On CPU32X based parts which have the stack located in the FASRAM, however, the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error.

WORKAROUND:
Workarounds exist for both CPU32 and CPU32X based parts. On CPU32 based parts the first access after an IACK cycles is the stacking of the vector offset The risk to the system by corrupting this stacked value is very low, it is not used by the processor. On CPU32X based parts which have the stack located in the FASRAM the first IMB3 access is the fetch from the vector table. Corruption of this value (handler address) causes the processor to jump to an incorrect location or to produce an address error. The suggested workarounds for the QSM/QSMCM/QADC64 are listed below. For CPU32 based parts: - assign the QSM/QSMCM/QADC64 it’s own interrupt levels separate from any other modules if the corruption of the vector offset in the stack frame is an issue. For CPU32X based parts: (a) assign the QSM/QSMCM/QADC64 its own interrupt levels separate from any other module in the system or (b) move the stack out of the FASRAM.

CDR_AR_584 Customer Information QSMCM.CDR1IMB3_01_0

QSMCM: Do not use link baud and ECK modes

DESCRIPTION:
Reads of the SCI control and status registers do not read correctly when using the link baud or the external clock source feature of the QSMCM. These modes are enabled by the SCCxR0 control register bits 0 and 1 (OTHR and LNKBD). These modes are not fully operational.

WORKAROUND:
Do not use the link baud or external clock modes of the QSMCM. The OTHR bit in the SCCxR0 control register 0 must be set = 0 to use normal mode operation only.

CDR_AR_16 Customer Information **TOUCAN.CDR1IMB3_03_0A**

Loop feature in the TOUCAN is not supported

DESCRIPTION:
Previous documentation indicated the capability in the TOUCAN to transmit back-to-back frames. A problem exists where a second frame in a sequence of two may be transmitted with its first IDENTIFIER bit corrupted. This function was enabled when the LOOP bit in CTRL1 was = 1.

WORKAROUND:
The loop feature is no longer supported. The previous LOOP bit in CTRL1 is now RESERVED and should never be set to 1. The TOUCAN specifications (revisions 3.1 or later) discuss this operation.

CDR_AR_1045 Customer Information **TOUCAN.CDR1IMB3_03_0A**

CAN: Bus Off recovery not ISO compliant

DESCRIPTION:
The Bus Off recovery is not ISO compliant on the FlexCAN and TouCAN modules. The ISO specification indicates that the CAN node should remain inactive until user intervention restarts it. The FlexCAN and TouCAN modules both include an automatic recovery mechanism for the Bus Off condition.

WORKAROUND:
The Bus Off condition interrupt should be enabled and an interrupt service routine implemented to disable the CAN. The user’s software should then determine when the CAN should be re-activated.

CDR_AR_627 Customer Information **TPU3.CDR1IMB3_01_0**

TPU: (Microcode) Add neg_mrl with write_mer and end_of_phase

DESCRIPTION:
Incorrect generation of 50% duty cycle is caused by the command combination "write_mer, end". If the write_mer is the last instruction together with the end, this may create an additional match using the old contents of the match register (which are in the past now and therefore handled as an immediate match)

WORKAROUND:
Add neg_mrl together with the last write_mer and with end-of-phase. The negation of the flag overrides the false match which is enabled by write_mer and postpones the match effect by one micro-instruction. In the following micro-instruction the NEW MER value is already compared to the selected TCR and no false match is generated. The neg_mrl command has priority over the match event recognition, separating the write_mer and the end command. This gives enough time for the new MER to update before the channel transition re-enables match events.

CDR_AR_577 Customer Information TPU3.CDR1IMB3_01_0

TPU3 - TCR2PSCK2 bit does not give TCR2 divide ratios specified.

DESCRIPTION:
The TCR2PSCK2 bit was originally specified to cause the TCR2 timebase to be divided by 2. Actually, it causes the TCR2 timebase to be divided as follows: The /16 of external clock and /128 of internal clock are eliminated and /3, /7, /15 of the external clock and /24, /56, /120 of the internal clock are added.

WORKAROUND:
When the TCR2PSCK2 is set, instead of the specified divides of /16, /32, /64, /128, expect the internal clock source to be /8, /24, /56 and /120 for TCR2 Prescaler values of 00, 01, 10 and 11, respectively. Likewise, for the external clock source expect /1, /3, /7, /15 instead of /2, /4, /8, /16.

CDR_AR_498 Customer Erratum UIMB.CDR1UBUSIMB3_01_0

UIMB: Read failures occur for IMB accesses when IMB clock is half speed

DESCRIPTION:
When the IMB clock is at half speed, a speed path occurs which prevents the proper data in the UIMB internal data latches from being observed by the user. Data is transferred from the latches before the latches are updated with data for the current cycle. This failure occurs when the part is heated (80-100C) and the frequency is at 40Mhz.

WORKAROUND:
There are 3 possible workarounds: (1). Since the internal latches are late in being updated with IMB data, it takes 2 consecutive reads from the same IMB location to observe the proper data from that location. The data from the first access should be disregarded when in half speed mode. (2). When running half speed on the IMB, keep the part as close to room temp. (25C) as possible. or (3). Only use full speed IMB mode. This workaround only applies to RevC or later.

CDR_AR_896 Customer Erratum UIMB.CDR1UBUSIMB3_01_0

UIMB: Avoid external code in addresses 0xZ[3,7,B,F]0_7F80 to 0xZ[3,7,B,F]0_7FFC

DESCRIPTION:
When two UBUS cycles are precisely pipelined, such that the first cycle is to an address within the IMB address range, (Internal memory map base address + 0x300000:0x307F7F), and the 2nd cycle is a fetch to an external address in which A[10:29] match A[10:29] of any unimplemented register of the UIMB module, then the IMB cycle will be tagged with an error resulting in a machine check exception. During operation, the pipelining of fetches relative to an IMB access will vary if an interrupt occurs between the last change of flow and the IMB access.

WORKAROUND:
1) Do not place instructions which might be fetched after an IMB access in external memory which matches A[10:24] = 0x60FF. In other words, the instruction address must not fall in the ranges: 0xZY0_7F80 to 0xZY0_7FFC, where ZY is in the external address space, Z=0x00 to 0xFF and Y is 3,7,B, or F. Or 2) Ensure that an external fetch is not pipelined with an IMB access by (a) running from internal memory, (b) running in serialized mode.

CDR_AR_90 Customer Erratum **UIMB.CDR1UBUSIMB3_01_0**

Poll TPU3 development status register to determine if TPU breakpoint occurs

DESCRIPTION:
A breakpoint requested by the TPU3 may not be recognized; hence, the FREEZE indication may not be asserted by the development port. The TPU3 will still halt. The device may draw up to 10mA more current when the breakpoint is requested by the TPU3.

WORKAROUND:
Development software should poll the Development Support Status Register to determine if TPU3 has encountered a breakpoint. If the TPU3 generates a breakpoint, the breakpoint status flag should be negated to reduce excessive current consumption.

CDR_AR_92 Customer Erratum **UIMB.CDR1UBUSIMB3_01_0**

Avoid instruction accesses from IMB regions

DESCRIPTION:
The uimb ignores aborts (for example, on cache hit or branch) for instruction accesses. This is applicable only when instructions are placed in the RAM of UIMB modules.

WORKAROUND:
Configure all regions controlled by the uimb as cache inhibited by configuring the IMPU, or prevent any instruction accesses to the uimb controlled regions.

CDR_AR_231 Customer Erratum **USIU.CDR1UBUS_01_0**

Avoid external master accesses to internal resources which result in data error

DESCRIPTION:
When an external master accesses the device and the access has a data error, the USIU asserts TEA externally but never releases bus request signals internally.

WORKAROUND:
1. Avoid slave accesses which cause data error.OR2.Initiate another access to internal valid address; this will release the internal dead lock

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CDR_AR_232 Customer Erratum **USIU.CDR1UBUS_01_0**

Do not configure IRQ1 and IRQ4 pins as AT2, RSV, or GPIO

DESCRIPTION:
IRQ1/RSV/SGPIOC[1] and IRQ4/AT[2]/SGPIOC[4] function as IRQ inputs only.

WORKAROUND:
Do not use these pins as GPIO/AT/RSV

CDR_AR_985 Customer Erratum USIU.CDR1UBUS_01_0

USIU: Do not use ORx[EHTR] with Dual Mapping

DESCRIPTION:
When an access is matched through the Dual Mapping registers (DMBR/DMOR), extended hold time (from a previous access region) or Burst length (from the new access region) may cause execution of wrong code.

WORKAROUND:
1) Do not set ORx[EHTR] while a dual mapping region is enabled. Or: 2) Do not enable dual mapping if an extended hold time is required for any memory in the system.

CDR_AR_235 Customer Erratum USIU.CDR1UBUS_01_0

Do not activate data show cycles when external master may access internal space

DESCRIPTION:
USIU slave does not check the state of internal bus request signal.

WORKAROUND:
Do not activate data show cycles in slave mode

CDR_AR_236 Customer Erratum USIU.CDR1UBUS_01_0

In slave mode, do not access another MPC55X

DESCRIPTION:
When the device is in SLAVE mode then the KR/RETRY pin is always an output.

WORKAROUND:
When the device is in SLAVE mode, do not access another MPC555.

CDR_AR_239 Customer Erratum USIU.CDR1UBUS_01_0

Reprogram RTCAL register for accurate real time clock interrupts

DESCRIPTION:
The Real Time Clock [RTC] counts a larger time than it should to give any of its interrupts

WORKAROUND:
For alarm interrupt required every XXX seconds RTCAL register should be programmed as follows: XXX / 2.6777 [20 MHz crystal] XXX / 9.3886 [4 MHz crystal].

CDR_AR_241 Customer Erratum USIU.CDR1UBUS_01_0

External write data may be corrupted during reset (SRESET or HRESET)

DESCRIPTION:
If reset [HRESET or SRESET] occurs during external write access the data may be corrupted due to wrong reset signal to pads.

WORKAROUND:
Use delay from the reset source to the HRESET [or SRESET] to ensure that the external access is completed before the device receives the reset. Also connect the reset signal source to IRQ0.

CDR_AR_267 Customer Erratum USIU.CDR1UBUS_01_0

When operating in slave mode, reduce the load on the RETRY pin

DESCRIPTION:
The pinout path for the RETRY pin is slow.

WORKAROUND:
Reduce the capacitive load on the RETRY pin connecting the master and slave.

CDR_AR_305 Customer Erratum USIU.CDR1UBUS_01_0

Do not use alternate masters on the external bus.

DESCRIPTION:
Address Pins 28:31 are corrupted when initiating an external bus access after another external master executed external bus transaction.

WORKAROUND:
Do not use alternate masters on the external bus.

CDR_AR_306 Customer Erratum USIU.CDR1UBUS_01_0

Asynchronous SRAMS with Byte Enables require glue logic

DESCRIPTION:
It is impossible to interface Static Ram memory devices which have Byte Enable signals to enable byte access.

WORKAROUND:
Use supported SRAMS or use glue logic to create the byte enables. A mode will be added in the future to support some of these devices.

CDR_AR_582 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU:Under certain conditions, XFC stuck at 0V on power-on

DESCRIPTION:
In some systems, the PLL does not lock on power-up. This issue occurs on some board designs, and not on others. On some boards, the not lock on startup occur if 3V VDD has a DC offset of ~150mV. This also happens when the VDDSYN ramps up much slower than the VDDL/VDDi. This can also be repeated if the XFC pin is temporarily shorted to ground. If the PLL does not lock and limp mode is disabled, the part will never negate HRESET, and CLKOUT will run at the backup clock frequency. If the PLL does not lock and limp mode is enabled, the part will exit reset clocked by the backup clock. For the sensitivities mentioned above, additional assertions of the PORESET pin will not cause the PLL to lock, only cycling the power (and avoiding the condition) will resolve the issue.Observation of the XFC pin (with a high impedance probe), can distinguish that XFC is "stuck" at 0.

WORKAROUND:
First, make sure that the PLL and reset circuitry is correct: see CDR_AR_598. If XFC is at 0V, add a circuit (VDDsyn voltage divider set at 1.1-1.3V over temp/voltage connected to small signal diode connected to XFC) to ensure XFC does not drop below ~0.8V. It has been reported that some boards may be able to avoid this issue by avoiding a DC offset on VDDL and controlling the ramp rate of VDDsyn and KAPWR. Injection into 3V only pins may result in an offset on VDDL -- refer to CDR_AR_595.

CDR_AR_595 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU: PLL will not lock on power-on, use limp mode and switch via software

DESCRIPTION:
In some systems, the PLL does not indicate lock on power-up. However, examination of the XFC with a high impedance, low capacitance probe indicates the VCO is at the correct frequency (20MHz XFC typically at ~1.6-1.8V). Additional assertions of the PORESET pin result in the PLL locking. This issue occurs on some board designs, and not on others. The PLL does seem to have some sensitivities related to power supplies. On some boards, the not lock on startup occur if 3V VDD has a DC offset of ~150mV. This also happens when the VDDSYN ramps up much slower than the VDDL/VDDi, or when KAPWR ramps faster. If the PLL does not lock and limp mode is disabled, the part will never negate HRESET, and CLKOUT will run at the backup clock frequency. If the PLL does not lock and limp mode is enabled, the part will exit reset clocked by the backup clock.

WORKAROUND:
Verify proper setup as noted in CDR_AR_598. To avoid system failure, always enable limp mode, allowing the system to boot using the backup clock even though lock is not yet indicated. After booting, switch from backup clock to PLL clock under software control. If EXTCLK is the clock input, use a higher frequency (15MHz or greater) and boot in 1:1 mode with limp mode enabled, or choose MODCK = 010, and overdrive the XTAL input from the oscillator output, and set EXTAL to a voltage of 0.5-0.6V. In this case, the oscillator output should be designed to meet an XTAL Vil of 300mv, with Iil= 1ma. Vih of 0.8v. To reduce fail to indicate lock, reduce the VDDL DC offset below 100mv by use of a discharge resistor. Ensure that current injected into 5V and 3V/5V pads is absorbed by circuitry attached to VDDH. While VDDL is off, avoid injecting current into 3V only pads since the PU3 circuit will cause an increase in VDDL.

CDR_AR_925 Customer Erratum USIU.CDR1UBUS_01_0

USIU: TEXP feature does not function when VDD supply is off

DESCRIPTION:
The TEXP function does not work if the main power supplies are powered down. Whenever VDD (low voltage supplies other than KAPWR and VDDSRAM) is powered down, hreset_b will be asserted by the chip and low power mode exited. The TEXP pin will never be asserted.

WORKAROUND:
The TEXP pin will never be asserted if VDD is powered down. Use an external counter to indicate the length of power down. As an alternate solution, put the part into Deep Sleep mode to reduce power consumption and leave the power supplies powered.

CDR_AR_223 Customer Erratum USIU.CDR1UBUS_01_0

Design system to allow additional address time on first external access

DESCRIPTION:
On the first external access after reset, the address valid time is ~2ns slower than specified due to 5V precharge of the address bus. This may cause wrong data to be read.

WORKAROUND:
Lower the frequency of the system if needed. If not booting from external device, discard the result from the first read.

CDR_AR_224 Customer Erratum USIU.CDR1UBUS_01_0

Run external bus in full frequency mode (not half frequency)

DESCRIPTION:
When operating as a bus master, the device may stop operating when the external bus is at half frequency (EBDF = 01) RCW[13:14]. Proper operation will resume upon reset. Slave operation at half frequency is still operational.

WORKAROUND:
Use full frequency external bus clocking. Lower the system frequency if required.

CDR_AR_234 Customer Erratum USIU.CDR1UBUS_01_0

Program must not change locked bits in the SIUMCR register

DESCRIPTION:
DLK bit locks only bits 8:15 in SIUMCR instead of all bits of the register. Bits 16:31 remain unlocked.

WORKAROUND:
be cautious when accessing the register.

CDR_AR_237 Customer Erratum USIU.CDR1UBUS_01_0

Read the USIU GPIO data register immediately after every data direction change

DESCRIPTION:
GPIO output data is not reflected on pins unless data register is read first.

WORKAROUND:
Read the GPIO data register immediately after every GPIO data direction change (input to output or vice versa).

CDR_AR_240 Customer Erratum USIU.CDR1UBUS_01_0

External master should not request burst from the MPC555

DESCRIPTION:
When the device is in slave mode/peripheral mode it will not assert the BI pin when accessed in burst mode.

WORKAROUND:
avoid activating burst cycles to the device by external master

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CDR_AR_242 Customer Erratum USIU.CDR1UBUS_01_0

Avoid 2 accesses in a row to non-existent external addresses

DESCRIPTION:
If two successive accesses are made to external non-existent addresses, the Bus Monitor may cause the device to hang.

WORKAROUND:
Avoid accessing external non-existent addresses-- in particular, two such accesses in a row.

CDR_AR_304 Customer Erratum USIU.CDR1UBUS_01_0

Factory test mode required to use TPU debug features

DESCRIPTION:
The TPU3 debug features can be activated only when factory test mode is set.

WORKAROUND:
Enter factory test mode, prior to using TPU3 debugger.

CDR_AR_380 Customer Erratum USIU.CDR1UBUS_01_0

Assert PORESET until all 3V supplies are in regulation

DESCRIPTION:
MODCK pins are not properly sampled while VDD is off. In addition, there is excessive KAPWR current consumption when VDD is off.

WORKAROUND:
Assert PORESET until all 3V supplies are in regulation. Allow for additional KAPWR current when VDDL is not powered.

CDR_AR_610 Customer Erratum **USIU.CDR1UBUS_01_0**

Additional current on KAPWR when power is not applied

DESCRIPTION:
There is a leakage path between KAPWR and VDDi/VDDL. This results in additional KAPWR current when VDDi/VDDL is not powered. The amount of current varies, partially based upon the MODCK setting.

WORKAROUND:
Design KAPWR supply to handle additional 15ma of current, if KAPWR is powered while VDDi and VDDL are not powered. For MODCK=011, expect up to 9ma of leakage current, for MODCK=010, expect up to 7ma of leakage current.

CDR_AR_909 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU: Do not assert cr_b to abort pending store reservation access

DESCRIPTION:
If an external cancel reservation (cr_b) is asserted then a pending store reservation may show on the external bus. This may occur with or without transfer start (ts_b), and will terminate after 1 clock. If the region is in the memory controller of the chip generating the store with reservation, then no chip-select or other memory controller attributes will assert on the bus, and the memory will not be altered.

WORKAROUND:
1) Do not assert cr_b; or 2) following assertion of cr_b, external logic must prevent the erroneous store with reservation bus cycle from altering memory, and must not assert ta_b to terminate the erroneous store with reservation bus cycle.

CDR_AR_910 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU: PITRTC Clock may not work when SCCR[RTDIV] is 0

DESCRIPTION:
The RCPU RTC/PIT may not count in all operating conditions if the ratio of System clock to the PITRTC Clock is less than or equal to 4. This may happen if the SCCR[RTDIV] is set to 0 and either 1) the part is running on the limp clock, or 2) the PLPRCR[MF] = 0 and both the System PLL and the PITRTC Clock use the same clock source (EXTCLK or the crystal oscillator).

WORKAROUND:
Keep the System Clock to PITRTC clock frequency ratio greater than 4. This can be done the easiest by setting the SCCR[RTDIV] to a value of 1 (reset value).

CDR_AR_984 Customer Erratum USIU.CDR1UBUS_01_0

USIU: Setting of SCCR[EBDF] may slow execution of code

DESCRIPTION:
If the SCCR[EBDF] is greater than 0 and the RCPU is running not serialized, the USIU may issue external read bus cycles that are not complete. The TS_B will assert with an address, but without a chip select or STS_B assertion. These cycles will cause a delay in execution of code, but will not cause the code to fail. These cycles will self terminate in 1 to 3 clocks (depending on the external pull up strength).

WORKAROUND:
There are two possible workarounds: 1) In a program with critical timing, do not run from external memory with the SCCR[EBDF] set to a value greater than 0. Or 2) If external logic is used as a memory controller, define the logic to disregard these extra bus cycles.

CDR_AR_221 Customer Erratum USIU.CDR1UBUS_01_0

Do not use LBDIP function of the memory controller

DESCRIPTION:
The LBDIP field (BR bit 28) of the memory controller is not functional.

WORKAROUND:
Do not use memories which require the LBDIP function.

CDR_AR_225 Customer Erratum USIU.CDR1UBUS_01_0

Latch RSV, AT, and PTR when TS or STS is asserted

DESCRIPTION:
The RSV_B AT[2] and PTR_B functions may be driven incorrectly during the data phase of an external bus cycle.

WORKAROUND:
Latch externally these signals using the CLKOUT rising edge when either TS or STS is asserted

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CDR_AR_227 Customer Erratum USIU.CDR1UBUS_01_0

Use MIOS PWM channel instead of ENGCLK to generate 1MHz clock

DESCRIPTION:
ENGCLK frequency range is CLKOUT/64 to CLKOUT/128. Hence, it is not possible to generate a 1Mhz or 4Mhz ENGCLK.

WORKAROUND:
Use MIOS PWM channel to generate 1Mhz clock.

CDR_AR_238 Customer Erratum **USIU.CDR1UBUS_01_0**

Avoid byte writes to PDMCR

DESCRIPTION:
When byte accesses is used to access PDMCR some bits may be corrupted.

WORKAROUND:
Use only full word access to PDMCR; if done so no problem will occur.

CDR_AR_270 Customer Erratum **USIU.CDR1UBUS_01_0**

Write either all 0s or all 1s to the reserved bits of SGPIOCR[8:15]

DESCRIPTION:
The output of the reserved bits in SGPIOCR (bits 8:15) register are shorted. Writing a different value will cause contention of the register output drivers.

WORKAROUND:
Write either all ‘0’ or all ‘1’ to these bits.

CDR_AR_287 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU: System to Time Base frequency ratio must be greater than 4

DESCRIPTION:
The Time Base and Decrementer may not count properly if the ratio of the System clock to Time Base Clock is 4 or less.

WORKAROUND:
Keep the ratio of the System Clock to the Time Base clock above 4. Always set SCCR[TBS] = 1 when running on the limp clock.

CDR_AR_288 Customer Erratum **USIU.CDR1UBUS_01_0**

Avoid unnecessary MF changes

DESCRIPTION:
The internal clock frequency may rise up to 100MHz upon MF bit field change. The internal clock frequency will rise for a few clocks before the clock stops (due to loss of lock detect). This may possibly cause a race. This may not have any effect; depends on chip activities.

WORKAROUND:
Avoid unnecessary MF changes.

CDR_AR_289 Customer Erratum **USIU.CDR1UBUS_01_0**

HRESET may be shorter than 70ns during SWT reset

DESCRIPTION:
The HRESET signal that is generated due to SWT (Software Watchdog) reset is sometimes shorter than 70ns.

WORKAROUND:
Ensure that external devices will be reset by this pulse or do not use the software watchdog reset. Ensure than no software watchdog reset occurs during flash programming.

CDR_AR_379 Customer Erratum **USIU.CDR1UBUS_01_0**

Don’t set MLRC=11 in multiple master configurations

DESCRIPTION:
In the case of MLRC=11 retry pad does NOT behave as retry in the "input" mode.

WORKAROUND:
Dont set MLRC=11 in multiple master configuration.

CDR_AR_483 Customer Erratum **USIU.CDR1UBUS_01_0**

USIU: BDIP may not assert for non-MEMC mapped accesses

DESCRIPTION:
in case of two memory accesses, the first is mapped through the MEMC, and the second is NOT, then the second will not assert BDIP.

WORKAROUND:
Do not use a mixture of MEMC mapped and non-mapped regions for doing external burst accesses.

CDR_AR_222 Customer Information **USIU.CDR1UBUS_01_0**

Program the memory controller base registers prior to enabling it

DESCRIPTION:
Memory controller base registers 1, 2, 3 reset value is the same as the reset value for base register 0.

WORKAROUND:
Change the BR1/2/3 values before enabling these Memory Controller regions.

CDR_AR_269 Customer Information **USIU.CDR1UBUS_01_0**

Load address signal is not provided when external master initiates cycles

DESCRIPTION:
When External master utilizes Memory Controller services to access external memory the CS will assert only at the 3rd clock of the access when TS is already negated.

WORKAROUND:
Do not use the MEMC to access external memory by external master if the memory uses TS to latch/load the address.

CDR_AR_228 Customer Information USIU.CDR1UBUS_01_0

In the USIU RSR, if both EHRS and ESRS are set, the reset source is internal.

DESCRIPTION:
EHRS and ESRS bits in RSR register are set for any internal reset source in addition to external HRESET and external SRESET events. If both internal and external indicator bits are set, then the reset source is internal.

WORKAROUND:
If both internal and external (EHRS/ESRS) indicator bits are set, then the reset source is internal. If only external (EHRS/ESRS) indicator bits are set, then the reset source is external.

CDR_AR_389 Customer Information USIU.CDR1UBUS_01_0

Little Endian modes are not supported

DESCRIPTION:
The little Endian modes are not functional.

WORKAROUND:
Do not activate little endian modes. The reference manual will be updated to remove all little endian mode references.

CDR_AR_442 Customer Information USIU.CDR1UBUS_01_0

Avoid loss of clock during HRESET

DESCRIPTION:
The chip may fail to switch to backup clock. This mode may occur if the input reference clock fails to toggle during hreset while switching from normal clock to backup clock. This condition may occur while switching from backup clock to normal clock (during hreset) if the PLL is not locked and there is no reference clock. In order to resume operation, the part may require the input reference clock to resume (for 1-2 more clocks) or for PORESET to be asserted.

WORKAROUND:
Avoid loss of the reference clock during hreset; ensure that the PLL is locked before switching to PLL clock. Do not enable reset upon loss of lock if limp mode is enabled, instead enable an change of lock interrupt by setting the COLIE bit (COLIR).

CDR_AR_594 Customer Information USIU.CDR1UBUS_01_0

USIU: Changing PLL MF to 1:1 mode can have 180 degree phase shift

DESCRIPTION:
After software changes MF from >1 to MF = 1, a 180 degree skew between EXTCLK and CLKOUT could occur.

WORKAROUND:
If synchronization between EXTCLK and CLKOUT is required, set MODCK to boot in 1:1 mode, and do not alter the MF bits to exit 1:1 mode.

CDR_AR_598 Customer Information USIU.CDR1UBUS_01_0

USIU: Ensure proper configuration for proper startup

DESCRIPTION:
In some systems, the PLL does not lock on power-up, or the system does not properly execute software out of reset. This issue occurs on some board designs, and not on others. Locking may be improved by board design and component selection, and can be resolved by paying attention to the design and setup, and ensuring that the PLL and Oscillator components are correct and as noise free as possible.

WORKAROUND:
First, make sure that the PLL and reset circuitry is correct: ensure that the PLL components are properly selected and that the PLL power (VDDSYN) is not noisy. Refer to appendix E of the users manual, "Clock and Board Guidelines". Verify that the XFC capacitor is connected to VDDSYN. Validate that the TRST pin is asserted upon power-up. Do not connect TRST to HRESET or SRESET. Validate that all power supplies are stable and all MODCK pins are at the correct levels in time for the PLL and Oscillator to be stable prior to PORESET rising above VIL. Verify that the proper reset configuration word is used. Validate the reset and post reset pin state for each pin controlled by the reset configuration word, and ensure there is not a conflict with an external driver. Preferably use the internal reset configuration word. If using an external reset configuration word, do not rely on the internal pull-downs to operate (refer to CDR_AR_454) and ensure that RSTCONF is asserted until SRESET is negated. After the part exits reset with the system running via the backup clock, validate the clock control registers settings and the PLL status. If the PLL is slow on locking, or the register settings indicate the MODCK pins are incorrect, address the board issues listed above. To avoid risk of system failure for no start, enable limp mode, allowing the system to boot using the backup clock even though lock is not yet indicated. After booting, switch from backup clock to PLL clock under software control after the PLL has gained lock.

CDR_AR_687 Customer Information USIU.CDR1UBUS_01_0

USIU: Program reserved bits in PDMCR to preserve compatibility

DESCRIPTION:
Future revisions of the PDMCR will have additional bits to control enabling and disabling of pad pull-up / pull-down resistors. Software should be written so that it is compatible with these changes. In this revision, PDMCR[8] (TPRDS) does not change the function of the TPU T2CLK pull-up resistors -- the pull-ups remain enabled.

WORKAROUND:
To ensure identical control in future revisions, when programming the PDMCR. PDMCR[8] should remain cleared. PDMCR[9:13] should be programmed to the same value as PRDS (PDMCR[6]). PDMCR[16:17] should be programmed to the same value as SPRDS (PDMCR[7]). The future function of PDMCR[14:15] has not been determined, and should be programmed to 0. For this revision, software should ignore any the read values of PDMCR[8:15].