Advanced CUSTOMER ERRATA AND INFORMATION SHEET
MCU Part: 68331.E Mask Set: 00H17A
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68331.E 00H17A Modules	
MODULE	VERSION
SIM	16.3.0
VCO	11.3.0
QSM	12.0
CPU32	16.0
GPT	02.0D
STDPORT	22.0

MODULAR_AR_857 Customer Information 68331.E

DESCRIPTION:

After power-up (Vdd greater than Vdd min.) of the MCU, input/output and output-only port pins on the CPU module and the output only PWM pins (PWMA, PWMB) on the GPT module may be in an indeterminate state for up to 15 ms (depends on ramp up conditions). Input/output pins may be in output mode (instead of high impedance) for this time, which may create a conflict with external drive logic. Output only pins may not be in the defined reset state during this time.

WORKAROUND:

If a known state is required on these pins, before the 15 ms port initialization period, external reset control logic must condition these lines.

MODULAR_AR_800 Customer Information VCO.11.3

DESCRIPTION:

In some Phase Lock Loop (PLL) documentation a three component filter from XFC to VDDSYN is recommended (18K resistor in series with 0.01 uF capacitor between VDDSYN and XFC, the series combination in parallel with a 3300 pF capacitor for a loop multiplier of N = 512). It has been determined with this three component filter, in the presence of external leakage (in excess of that provided by ~50 M Ohm) on the XFC pin, may result in the MCU not exiting RESET at power up. During this condition, the output frequency on CLKOUT is at the target value, but the PLL lock detect logic does not detect lock and continues to cause RESET assertion. Versions of the integration module that are configured for either a slow or fast (Typ. 32.768 kHz or 4.194 MHz) crystal source use the same filter component values (was VCO:051).

WORKAROUND:

Do not use the three component filter on XFC. Use the originally documented filter (single 0.1 uF capacitor from the XFC pin to the VDDSYN supply pin).

MODULAR_AR_986 Customer Information VCO.11.3

DESCRIPTION:

The "PLL Lock Time" (tlpll) specification is documented as 20 ms. This value applies to the time for the PLL to lock after changing the W or Y bits in the synthesizer control reqister (SYNCR) while the PLL is running, and to the period required for the PLL to lock after LPSTOP is exited. This specification does not apply at warm start-up (with VDDSYN applied and crystal stable, followed by VDD power application). The warm start-up period is a maximum of 50 ms. (This was previously IM:098, VCO:059, AR_806 and in some cases AR_987).

WORKAROUND:

Use 50 ms for "PLL Lock Time" (tlpll) specification.

MODULAR_AR_930 Customer Information SIM.16.3

DESCRIPTION:

Several conditions combined may introduce apparent Periodic Interrupt Timer (PIT) clock errors. The clock error occurs if LPSTOP mode is entered and exited periodically using the PIT, and the system clock is set to minimum (PLL control bits in SYNCR register set to: Y=0, and W =0) prior to entry of LPSTOP mode and system clock set to maximum at LPSTOP exit (STSIM=0, VCO off in LPSTOP, therefore the PLL must re-lock). Also, on exiting from LPSTOP, the CPU will be held off of the bus until the PLL is re-locked. Variations in the PIT clock period may appear as the PIT counter missing clocks (the PIT is clocked by the EXTAL reference clock in LPSTOP, if STSIM = 0). During normal operation (not in LPSTOP) the PIT counter clock source (EXTAL) is synchronized by logic to the system clock (CLKOUT). The combination of PLL re-lock time, low frequency clock source (too near the internal PLL reference), and the synchronization, results in this behaviour. (Previously IM:097 and Issue #653).

WORKAROUND:

Restrict the minimum PLL frequency to at least 2 times the minimum possible reference frequency (PLL control bits in SYNCR register set to: Y=0, and W =%01) or higher. This restriction applies if the system clock is toggled from a low frequency prior to LPSTOP entry (if STSIM = 0) and back to maximum on exit of LPSTOP periodically using the PIT as the controlling source. The problem is only seen when switching the PLL clock to a frequency that is too close to the reference (EXTAL) clock frequency.

MODULAR_AR_975 Customer Information CPU32.16.0

DESCRIPTION:

When a spurious interrupt awakens the MCU from LPSTOP, the spurious interrupt handler is not called, and the CPU sits idle until another IRQ is detected. The effect is the same as if the STOP instruction was actually executed, from the point that the spurious interrupt occurs, instead of the LPSTOP instruction.

WORKAROUND:

If power consumption is important and LPSTOP is used, do not allow any spurious interrupts to occur during the LPSTOP state.

MODULAR_AR_823 Customer Information CPU32.16.0

DESCRIPTION:

In previous versions of this module, when exiting BDM, FREEZE negated after the DSI/FETCH signal turns around from an input to an output. This meant that an external development system could be driving DSI while the MPU was still driving IFETCH. The timing has been changed to insure that on exit of BDM FREEZE is negated prior to IFETCH changing to an output. Also, on entry to BDM, the DSI/IFETCH pin goes to a high impedance state prior to asserting FREEZE. (Previous related versions of this issue were CPU32:062 and AR_221).

WORKAROUND:

None required.

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