Advanced CUSTOMER ERRATA AND INFORMATION SHEET
MCU Part: 68331.D Mask Set: 01G91H
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68331.D 01G91H Modules	
MODULE	VERSION
CPU32	16.0
SIM	16.0
VCO	11.0B
GPT	02.0D
QSM	12.0
STDPORT	22.0

MODULAR_AR_951 Customer Erratum 68331.D

DESCRIPTION:

Under certain circumstances, the MCU may not exit the LPSTOP mode. When the Phase Lock Loop (PLL) is enabled (MODCK = 1 at RESET negation), the following PLL control configuration may result in a problem. If the STSIM bit in the SYNCR register is set to “0” and the LPSTOP instruction is executed, the MCU may not always fully “wake up” from LPSTOP.

WORKAROUND:

When using LPSTOP, make sure to keep STSIM set to a “1” (PLL runs in LPSTOP mode). This causes higher power consumption than using STSIM=0. The power can be reduced by half if the X bit in the SYNCR is cleared immediately before entering LPSTOP, and set immediately after exiting LPSTOP. This assumes that the X bit is set during normal operation.

MODULAR_AR_857 Customer Information 68331.D

DESCRIPTION:

After power-up (Vdd greater than Vdd min.) of the MCU, input/output and output-only port pins on the CPU module and the output only PWM pins (PWMA, PWMB) on the GPT module may be in an indeterminate state for up to 15 ms (depends on ramp up conditions). Input/output pins may be in output mode (instead of high impedance) for this time, which may create a conflict with external drive logic. Output only pins may not be in the defined reset state during this time.

WORKAROUND:

If a known state is required on these pins, before the 15 ms port initialization period, external reset control logic must condition these lines.

MODULAR_AR_800 Customer Information VCO.11.0B

DESCRIPTION:

In some Phase Lock Loop (PLL) documentation a three component filter from XFC to VDDSYN is recommended (18K resistor in series with 0.01 uF capacitor between VDDSYN and XFC, the series combination in parallel with a 3300 pF capacitor for a loop multiplier of N = 512). It has been determined with this three component filter, in the presence of external leakage (in excess of that provided by ~50 M Ohm) on the XFC pin, may result in the MCU not exiting RESET at power up. During this condition, the output frequency on CLKOUT is at the target value, but the PLL lock detect logic does not detect lock and continues to cause RESET assertion. Versions of the integration module that are configured for either a slow or fast (Typ. 32.768 kHz or 4.194 MHz) crystal source use the same filter component values (was VCO:051).

WORKAROUND:

Do not use the three component filter on XFC. Use the originally documented filter (single 0.1 uF capacitor from the XFC pin to the VDDSYN supply pin).

MODULAR_AR_986 Customer Information VCO.11.0B

DESCRIPTION:

The “PLL Lock Time” (tlpll) specification is documented as 20 ms. This value applies to the time for the PLL to lock after changing the W or Y bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the PLL to lock after LPSTOP is exited. This specification does not apply at warm start-up (with VDDSYN applied and crystal stable, followed by VDD power application). The warm start-up period is a maximum of 50 ms. (This was previously IM:098, VCO:059, AR_806 and in some cases AR_987).

WORKAROUND:

Use 50 ms for “PLL Lock Time” (tlpll) specification.

MODULAR_AR_825 Customer Erratum SIM.16.0

DESCRIPTION:

Certain conditions will produce Periodic Interrupt Timer (PIT) timeout period errors. The worst case error occurs if LPSTOP mode is entered and exited using the PIT, and the system clock is set to minimum PLL control bits in SYNCR register set to: Y=0, and W =0) prior to entry into

LPSTOP and then set to maximum at LPSTOP exit (STSIM=0, VCO off in LPSTOP, therefore the PLL must re-lock). Also, on exiting from LPSTOP, the CPU will be held off of the bus until the PLL is re-locked. PIT period variations may appear as PIT counter missing or gaining clocks (the PIT is clocked by the EXTAL reference clock in LPSTOP, if STSIM = 0). Furthermore, a PIT period error is introduced whenever the PLL frequency is changed (whether LPSTOP is involved or not). (Previously AR_653).

WORKAROUND:

To increase timeout accuracy for the PIT when switching to a low system frequency before entering LPSTOP, restrict minimum PLL frequency before going into LPSTOP. The minimum PLL frequency must be determined by experimentation.

MODULAR_AR_956 Customer Erratum SIM.16.0

DESCRIPTION:

When operating in PLL mode (MODCK = 1 at RESET negation), if the PIT or software watchdog prescalars are enabled, neither prescalar control bit may be changed again. In PLL mode, the reset state of the PTP (PITR register) and SWP (SYPCR register) bits is “0” (prescalars disabled). If either bit is written to a “1”, subsequent writes to either bit will have no effect.

WORKAROUND:

If a prescalar is to be used, choose either the PIT prescalar or the software watchdog prescalar and set the appropriate prescalar enable bit. Only 1 prescalar may be used, and the control bit, once written, cannot be turned off. If no prescalar is to be used, be careful to ensure that neither prescalar enable bit is inadvertently set - once set, it cannot be cleared.

MODULAR_AR_876 Customer Information SIM.16.0

DESCRIPTION:

When the internal PLL clock system is not used (MODCK=0) at RESET negation) then the following behavior may occur. During power down, if the external clock degrades such that it no longer meets the AC Timing Specification for the External Clock Input High/Low Time (tXCHL), then the Input/Output and Output-only pins of the integration module and other modules may become active. Assertion of the external RESET pin under these conditions does not guarantee the level on the RESET pin will be internally recognized and the internal RESET signal may be negated under these anomalous conditions. The internal RESET signal is used to hold the Input/Output and Output-only pins in their respective high impedance mode. If the on-chip PLL is used for the clock source there is no problem as the PLL will meet the specifications to the minimum Vdd.

WORKAROUND:

If an External Clock is used, then insure that the External Clock signal does not degrade and violate the specifications as power goes down. Alternately, protect external devices that may be damaged (ex: non-volatile memories).

MODULAR_AR_658 Customer Information SIM.16.0

DESCRIPTION:

The loss of clock reference feature is not supported and may not function. Disregard bit position 4 in the SYNCR register (previously the SLIMP bit), this bit is now reserved. Insure that the bit position 2 (previously the RSTEN bit) in the SYNCR register is always written to it's RESET state of %0. (This was previously IM:077).

WORKAROUND:

Do not rely on the loss of clock LIMP mode feature.

MODULAR_AR_908 Customer Information SIM.16.0

DESCRIPTION:

The documentation for the state of the RMC/PE3, SIZ[1:0]/PE[7:6] and DS/PE4 pins is inconsistent between the users manuals (MC68...USM) and the SIM/SCIM reference manuals (Module..RM). The users manuals indicate the pins are in a high impedance state while RESET is asserted, which is correct. The SCIM/SIM manuals indicate the pin state is determined by the data bus configuration while RESET is asserted, which is not correct.

WORKAROUND:

Refer to documentation in the users manuals for the RESET state of these pins.

MODULAR_AR_975 Customer Information CPU32.16.0

DESCRIPTION:

When a spurious interrupt awakens the MCU from LPSTOP, the spurious interrupt handler is not called, and the CPU sits idle until another IRQ is detected. The effect is the same as if the STOP instruction was actually executed, from the point that the spurious interrupt occurs, instead of the LPSTOP instruction.

WORKAROUND:

If power consumption is important and LPSTOP is used, do not allow any spurious interrupts to occur during the LPSTOP state.

MODULAR_AR_823 Customer Information CPU32.16.0

DESCRIPTION:

In previous versions of this module, when exiting BDM, FREEZE negated after the DSI/FETCH signal turns around from an input to an output. This meant that an external development system could be driving DSI while the MPU was still driving IFETCH. The timing has been changed to insure that on exit of BDM FREEZE is negated prior to IFETCH changing to an output. Also, on entry to BDM, the DSI/IFETCH pin goes to a high impedance state prior to asserting FREEZE. (Previous related versions of this issue were CPU32:062 and AR_221).

WORKAROUND:

None required.

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