ES_LPC134x

Errata sheet LPC1342/43

Rev. 6.2 — 13 September 2013 **Errata sheet**

Document information

Info	Content
Keywords	LPC1342FBD48, LPC1342FHN33, LPC1343FBD48, LPC1343FHN33 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
6.2	20130913	• Added I2C.1.
6.1	20120823	• Added VDD.1.
6	20120111	• Added ISP.1, ISP.2, and ADC.2.
5	20110525	• Added USB.1.
4	20110401	• Combined LPC1342/43 errata into one document. • Added Errata Note.1.
3	20101110	• Added ADC.1.
2	20100701	• Corrected top-side marking information.
1	20091209	• Initial version.

Contact information

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1. Product identification

The LPC134x devices typically have the following top-side marking:

LPC134xx

xxxxxxx

xxYYWWxR[x]

The last/second to last letter in the third line (field 'R') identifies the device revision. This Errata Sheet covers the following revisions of the LPC134x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	External sync inputs not operational.	'A'	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	'A'	Section 3.2
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'A'	Section 3.3
ISP.1	In USB ISP mode, Code Read Protection levels CRP1 or CRP2 do not function as expected.	'A'	Section 3.4
ISP.2	If the USB ISP mode is entered on power-up, the LPC134x might not always enumerate as a Mass Storage Class (MSC) device.	'A'	Section 3.5
USB.1	The host receives zero bytes on the bulk endpoint instead of the expected 13 bytes.	'A'	Section 3.6
VDD.1	The minimum voltage of the power supply ramp must be 200 mV or below	'A'	Section 3.7

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
Note.1	On the LPC134x, for USB operation, the supply voltage (V_{DD}) range must be 3.0 V ≤ V_{DD} ≤ 3.6 V.	'A'	Section 5.1

3. Functional problems detail

3.1 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (use this value when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0.	
		0x3	Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0.	
		0x4	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0.	
		0x5	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1.	
		0x6	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0.	
		0x7	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1.	

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0_2 or PIO1_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing an ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 100 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error does not affect the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC134x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.3 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I^2C-bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I^2C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100 % non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.4 ISP.1: In USB ISP mode, Code Read Protection levels CRP1 or CRP2 do not function as expected

Introduction:

The LPC134x boot ROM contains software which enables on-chip flash programming via USB. In USB ISP mode, the LPC134x is enumerated as a Mass Storage Class (MSC) device to a PC or another embedded system. The entire available user flash is mapped to a file of the size of the LPC134x flash. The file is visible in the root folder with the default name 'firmware.bin'. The 'firmware.bin' file can be deleted and a new file can be copied into the directory, thereby updating the user code in flash. The Code Read Protection (CRP) level determines how the flash is reprogrammed. One of the three Code Read Protection (CRP) levels can be enabled for flash images. When the CRP enabled part is updated through USB ISP:

1. If CRP1 or CRP2 is enabled, the user flash is erased when the file is deleted.
2. If CRP1 is enabled or no CRP is selected, the user flash is erased and reprogrammed when the new file is copied. However, only the area occupied by the new file is erased and reprogrammed.
3. If CRP3 is enabled, the ISP mode cannot be forced via ISP entry pin; hence the user flash content cannot be read or updated. The bootloader always executes the user application if valid. ISP mode can also be activated by user code by making appropriate (In-Application Programming) IAP function call.

Problem:

Only in USB ISP mode, the Code Read Protection levels CRP1 or CRP2 does not function as expected. In USB ISP mode, Code Read Protection level CRP3 functions as expected.

Work-around:

If the user application cannot use CRP3, additional action is needed for CRP1 and CRP2. To use CRP1 or CRP2, the application should permanently lock sector 0 against write/erase operation. Sector lock can be performed in software by calling appropriate functions in the library provided by NXP. Details on how to use the library can be found in the technical note (TN00004) available on www.nxp.com. Sector locking code can be made part of the application being protected or introduced in production flow where sector locking is performed once flash is programmed. Failure to lock sector 0 could render the CRP1 and CRP2 levels ineffective. Locking sector 0 is an irreversible action which implies that the code in sector 0 cannot be changed again in future. Also, once sector 0 is locked, CRP2 enabled parts cannot be updated using UART ISP mode.

3.5 ISP.2: If the USB ISP mode is entered on power-up, the LPC134x might not always enumerate as a Mass Storage Class (MSC) device

Introduction:

On the LPC134x, the boot ROM contains a USB driver which supports development of the Human Interface Devices (HID) and the Mass Storage Class (MSC) devices. The MSC class driver implements a disk drive which can accept file reads and writes from a host. Upon entry to USB ISP mode, the LPC134x device will enable the on-chip USB full-speed interface as a mass storage class (MSC) device. This disk device will contain a FAT12 filesystem which will appear as a standard disk device in most operating systems.

Problem:

For the LPC134x device with bootloader version 5.2, if the USB ISP mode is entered on power-up, the memory is not initialized. As a result, no user code is executed which could write to this memory location, and the LPC134x might not always enumerate as a Mass Storage Class (MSC) device.

Work-around:

None.

3.6 USB.1: The host receives zero bytes on the bulk endpoint instead of the expected 13 bytes

Introduction:

Section 6.7.2 of the Universal Serial Bus Mass Storage Class Bulk-Only Transport specification states that in the case where the host expects to receive a certain number of bytes from the device over a Bulk-In endpoint after a Data In operation, and the device returns less data that what the host was expecting, the device must stall the pipe. Once the host reads the data that was sent, the pipe is reset by sending an ENDPOINT HALT (Clear Feature).

The specific host requirements are:

1. The host shall send a valid and meaningful CBW.
2. The host shall attempt to receive data from the device.
3. On a STALL condition receiving data, then:
   - The host shall accept the data received.
   - The host shall clear the Bulk-In pipe.
4. The host shall attempt to receive a CSW.

The specific device requirements are:

1. The device shall receive a CBW.
2. When the CBW is valid and meaningful, then:
   - The device shall attempt the command.

   If the device actually transfers less data than the host indicated, then:
   - The device **may** end the transfer with a short packet.
   - The device shall STALL the Bulk-In pipe.
   - The device shall set bCSWStatus to 00h or 01h.
   - The device shall set dCSWDataResidue to the difference between dCBWDataTransferLength and the actual amount of relevant data sent.

Problem:

In this specific situation where the host sends the ENDPOINT HALT command to the device the firmware responds by programming two packets in the USB device buffers in this order:

1. A 13 byte packet containing the CSW for the DATAIN command to the Bulk-In endpoint buffer
2. A zero byte packet (a control status phase packet for the Clear Feature command) to the control endpoint buffer

The problem occurs when the host receives zero bytes on the bulk endpoint instead of the programmed 13 bytes. Since it was expecting 13 bytes, it interprets this as an error and performs an SE0 on the bus resulting in the device being reset.

When this errata was written, the example code located in the file usbcore.c provided by NXP for these parts performed the operations in this order.

Work-around:

Reverse the order of the two operations to prevent this error from happening.

1. Progam a zero byte packet (a control status phase packet for the Clear Feature command) to the control endpoint buffer.
2. Progam a 13 byte packet containing the CSW for the DATAIN command to the Bulk-In endpoint buffer.

3.7 VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below

Introduction:

The datasheet specifies that the power supply (on the V_{DD} pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the V_{DD} pin) needs to be below 400 mV or below before ramping up is 12 us.

Problem:

The device might not always start-up if the power supply (on the V_{DD} pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the V_{DD} pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

Work-around:

None.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes

5.1 Note.1

On the LPC134x, for USB operation, the supply voltage (V_{DD}) range must be 3.0 V $\leq V_{DD} \leq$ 3.6 V.

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