MOTOROLA

Chip Errata
DSP56166 Digital Signal Processor
Mask: E52N

ERRATA

Errata Description	Applies to Mask
There is only one version of the DSP56166 silicon mask number E52N that runs at 60 MHz. This version is tested as shown in the table below:	E45H E19K E52N

Table 1: Testing Conditions

Characteristic	Symbol	60 MHz		Unit
		Min	Max	
Supply Voltage	V_{CC}	4.5	5.5	V
Junction Temperature	T_J	- 40	115	°C

The PLL is functional and tested at 60 MHz. — E45H, E19K, E52N

The PLL SXFC by-pass capacitor should be connected to GND. — E45H, E19K, E52N

The codec is functional and tested with a 20 MHz external clock with 0 dB gain on the A/D input and D/A output using a 128 decimation ratio. The A/D is tested with a 0.4 Vrms input signal at 1.5 KHz and the D/A is tested with a digitally generated sine wave with an amplitude of 50% full scale at 2 KHz. Under those conditions, the SNR and THD of the A/D and D/A are better than 65 dB.

The best codec performance can be obtained with the following conditions: — E52N

a. The codec clock should have an approximately 50% duty cycle. An approximately 50% duty cycle codec clock can be achieved when the input clock to the codec is divided by an even number External Divider as set by the ED[5:0] bits in the Codec Control Register 0 (CCR0).

b. When the audio gain bits, VC[3:0], of the D/A section are set to more than 5 dB gain and the output signals reach the saturation limit, instead of clipping, these outputs will oscillate.

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1. During power-up, if the SXFC by-pass capacitor is connected to V_{CC}, the PLL may drift to the maximum VCO frequency.

   It is recommended that the SXFC by-pass capacitor is connected to GND to prevent this condition from occurring.

2. During STOP mode, a floating node exist in the PLL which allows the SXFC voltage to drift up to V_{DD}. This increase the risk of the PLL to be locked at the maximum VCO frequency coming out of STOP mode.

   The work-around is to place a 10 MΩ resistor from the SXFC pin to GND.

3. The PLL lock bit detection circuitry failed to operate correctly in an over-damped system where the SXFC external capacitor is larger than or equal to 1000 pF. This causes the lock bit to not be asserted even though the PLL still lock properly.

   The recommended work around is to use a software time loop of 5 ms or more instead of the "lock bit assertion" polling loop.

   The hardware work-around is to use a smaller capacitance value (around 220 pF for lock bit assertion)) for the capacitor from the SXFC to GND and then switch to a larger capacitance value (bigger or equal to 1000 pF for stability) once the lock bit has been asserted.

4. The CHKAAU instruction does not operate correctly if there is a killed instruction between the last valid AALU update and the CHKAAU instruction.

   This is true where CHKAAU follows a conditional instruction such as BRKcc, REPcc and REP 0.

   For example:

```
clr     a
move    #$800,x0
move    x0,a
move    #3,r0
andi    #0,ccr
asl     a           (r0)-
repnr                       ; condition true, do not rep
asl     a           (r0)-   ; this instruction is killed
chkaau                      ; problem occurs here
```

   There is no software work around for this problem.

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5. If the second read of a dual read instruction is from the on-chip or internal memory and the dual read instruction is immediately preceded by the conditional transfer instruction where the condition is false (the transfer is aborted), then the incorrect data will be read to the register.

   For example:

```
move     #$400,r0
move     #$c000,r1
move     #$c030,r3
tlt      x0,b    r0,r2       ;condition false, do not transfer
add      y0,b    x:(r1)+,y1   x:(r3)+,x1   ; problem here
```

   Adding an instruction, such as NOP, between the Tcc instruction and the dual read instruction would fix the problem.

6. The RSSI receive/transmit interrupts occur when the interrupt is enabled even though the transmit/receive enable are cleared.

   For example:

   TE = 0, TIE = 1, TDE = 1: The transmit interrupt will occur even though the transmitter is disabled.

7. In gated clock mode, the RSSI receiver does not operate unless the transmitter is also enabled. So in order to receive data, in gated clock mode, both RE and TE must be set.
8. In external gated clock mode, the data on the RSSI STD pin can occur 2 bit periods late. If this problem occurs, then the observable effect is that the STD pin remains three-stated during the first two bit periods of a transmit word.
9. In external gated clock mode, the RSSI STD pin can be three-stated in the middle of a word by clearing the TE bit. This is not consistent with other RSSI operating modes where clearing the TE bit in the middle of a transmit word causes the STD pin to be three-stated at the end of the transmit word.
10. In the RSSI, when TUE has been set for more than one word period, while the transmitter is operating, TUE can be incorrectly set again after it has been cleared by reading SR and then writing TX or TSR. This problem occurs when the clear operation is performed during the last half bit period of one word or the first half bit period of the next word. When this happens, the TDE and TUE flags will be asserted at the same time after the clear operation.

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NOTES

1. An over-bar (i.e. $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56166 mask numbers apply.
3. Manuals and data sheets may also have errata that is documented on the appropriate errata sheet as discovered.

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