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MC68HC08QTx/QYx Conversion Guidelines

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1 Introduction

This engineering bulletin describes the MC68HC08QTx/QYx (ROM QYx). The 08QTx/QYx is a read only memory version of the Q family series of devices (referred to as the QY Classic in this document). Customer requests have led to the advanced design of the ROM QYx that has added adaptability, new features, and contains lead-free packaging.

This document:

- Provides information needed to convert from QY Classic to the ROM QYx
- Highlights the benefits of making this change

Sections:

- Benefits of the Enhanced ROM QYx
- Conversion Considerations
- Code Changes Checklist
- Development Tools
- Differences in Packaging

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Development hardware used for QYx can be used with ROM QYx. The ROM QYx is pin-for-pin compatible with QY Classic and can be placed on existing QY4 Classic hardware. However, the best device for creating application code for the ROM QYx is the HC908QY8. Existing cyclone/multilink tools and any programming or evaluation boards work for the ROM QYx. Emulation can be done using the EML08QCBLTYE.

2 Benefits of the Enhanced ROM QYx

The ROM QYx contains new and enhanced modules that add more flexibility and new features to the QY Classic. These benefits can improve the operation of an application or lead to new features for an application. For more information regarding these features, refer to the MC68HC08QY4 data sheet.

2.1 New Analog-to-Digital Converter Module (ADC)

The ROM QYx contains a 10-bit ADC that replaces the 8-bit ADC on the QY Classic. This module allows 10-bit and 8-bit conversion modes. The increased precision for ADC readings can be useful in many applications.

Features of the ADC new 10-bit module include:

- Two new ADC channels have been placed on PTB0 and PTB1, allowing added flexibility when debugging in monitor mode.
  - A limitation of QY Classic debugging is that access to the ADC channels is limited because many of the QY Classic pins are multiplexed. Having extra ADC channels on the PTB pins resolves this limitation.
- The ADC on the ROM QYx can operate while the MCU is in stop mode, allowing lower power operation. This also adds a lower noise environment for precise ADC results.
- Enabling an ADC channel no longer overrides the digital I/O function of the associated pin. To prevent the digital I/O from interfering with the ADC read of the pin, the data direction bit associated with the port pin must be set as input.
- Finally, the new ADC can be configured to select two different reference clock sources:
  - The internal bus x 4
  - An internal asynchronous source

    The internal asynchronous clock source allows the ADC to be clocked for operation in stop mode.

2.1.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 1. ADC10 Status and Control Register (ADSCR)

The ADCHx bits can be used to select additional ADC channels or bandgap measurement.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	AD9	AD8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2. ADC10 Data Register High (ADRH), 10-Bit Mode

The 10-bit ADC uses the new ADRH register for the upper 2 bits.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADLPC	ADIV1	ADIV0	ADICLK	MODE1	MODE0	ADLSMP	ACLKEN
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 3. ADC10 Clock Register (ADCLK)

A long sample time option has been added to conserve power at the expense of longer conversion times. This option is selected using the new ADLSMP bit in the ADCLK register. (The bit location was previously reserved.)

The ADC now runs in stop mode if the ACLKEN bit is set to enable the asynchronous clock inside the ADC module. Utilizing stop mode for an ADC conversion gives the quietest operating mode to get extremely accurate ADC readings. (This bit location now used by ACLKEN was reserved — it always read as a 0 and writes to that location had no affect.)

2.2 Enhanced Oscillator Module (OSC)

The ROM QYx contains a much enhanced oscillator module that allows more options than the QY Classic.

- The ICFS bits in the oscillator status and control register (OSCSC) allow the internal oscillator to be configured for 1, 2, or 3.2 MHz operation. Also, the ECFS bits in the same register allow a low-, medium-, or high-crystal frequency range to be selected for the source of the system clock. With this option, you can choose to use a 32 kHz (low range) or a 16 MHz (high range) crystal.

- Another improvement to the oscillator module design is that you can switch between internal and external oscillator options at any time. For example, if you want the low power advantage of running from a 32 kHz crystal, but need some processing power to perform math calculations, you could switch between internal and external clock. The same is true for switching between 1, 2, and 3.2 MHz internal oscillator options.

2.2.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	OSCOPT1	OSCOPT0	ICFS1	ICFS0	ECFS1	ECFS0	ECGON	ECGST
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4. Oscillator Status and Control Register (OSCSC)

The OSCOPT bits are no longer in the CONFIG2 register and now reside in the OSCSC register. Also, the ICFSx and ECFSx bits now reside in this register.

The IFS bits are used to select different internal oscillator speeds.

The ECFS bits are used to select the range of crystal that should be used to provide the reference clock.

2.3 Improved Auto Wakeup Module (AWU)

The ROM QYx contains an AWU that has improved accuracy across voltage and temperature for typical testing.

- A new feature provides ability to run the AWU from an alternate source (internal oscillator or external crystal). This is an advantage for an application that needs more accurate AWU operation.
- On the ROM QYx AWU approximate timeout is 16 ms for short timeout and 512 ms for long timeout when running from the internal 32 kHz RC source.
- Finally, at lower voltages typical measurements have shown lower power consumption by the ROM QYx AWU.

2.3.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQPUD	IRQEN	R	R	R	R	OSCENINSTOP	RSTEN
Write:								
Reset:	0	0	0	0	0	0	0	U
POR:	0	0	0	0	0	0	0	0

R = Reserved U = Unaffected

Figure 5. Configuration Register 2 (CONFIG2)

Setting the OSCENINSTOP bit forces the AWU to use bus clock x 4 as the source to this timeout.

2.4 New Power-on Reset Module (POR)

The ROM QYx POR re-arm voltage has a minimum specification of 0.7 V while the QYx Classic POR re-arm was 0.1 V. The higher POR re-arm voltage provides added protection against brown out conditions.

2.5 Keyboard Interface Module (KBI) Functionality

The KBI module for the ROM QYx has the added capability of:

- Triggering a KBI interrupt on the rising or falling edge of an input while the QYx Classic has the capability of triggering on falling edges only.
  - A new register (keyboard interrupt polarity register) determines the polarity of KBI. The default state of this register configures the ROM QYx for triggering on falling edges to be compatible with QYx Classic.
  - The ROM QYx now has pulldown resistors for the input pins configured for rising edge operation.

2.5.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6. Keyboard Interrupt Polarity Register (KBIPR)

The KBIPR allows the selection of polarity. If any of these bits are set, the corresponding interrupt pin is configured for rising edge and a pulldown resistor is added to the pin.

2.6 Operating Voltage Range

The operating voltage range for the ROM QYx includes 1.8 to 3.6 V operation. This is in addition to 3 V and 5 V operation available on the QY classic.

- Maximum internal operating frequency for 1.8 to 3.6 V operation is 2.1 MHz.
- The low-voltage inhibit reset trip point is typically 1.95 V. For 1.8 V operation, this reset should be disabled.
- Finally, typical run current at 2 V and 2 MHz bus speed is around 1.2 mA.

3 Conversion Considerations

Enhancements lead to slight differences in operation from QY Classic to the ROM QYx. A few points should be considered in the conversion process.

- The ROM QYx contains new modules such as the 10-bit ADC and OSC. In rare cases, new modules could cause customers to have to modify a few instructions in their application code. For example, if ADC code was written so entire registers are configured without respect to reserve bits, the ADC code needs to be revised to work correctly on the ROM QYx.
- The reference clock for ADC conversions has changed from the bus clock to the system clock (Bus Clock times 4). A change to the divide register may be necessary to set the reference clock to a specified value.
- The default internal oscillator speed for the ROM QYx is 1 MHz, the default for QY Classic is 3.2 MHz. The ICFS bits in the oscillator status and control register (OSCSC) can be changed by application software so the internal oscillator is set to 3.2 MHz after reset.
- The ROM QYx trim value (0xFFC0) can only be programmed at the factory. The ROM order form is used to select the frequency and voltage that this trim value is correlated to.
- The ROM QYx LVI trip points can typically be set to 1.95 V or typically 4.2 V. The QY Classic supports 2.55 V and 4.2 V trip points. On the ROM QYx, the only trip point available is the 1.95 V trip point. There is a bandgap voltage reference available to calculate values of Vdd. This can be used to do a software low-voltage interrupt (LVI).

4 Code Changes Checklist

Below is a checklist that should be reviewed in the conversion process. This checklist points out all the issues that should be addressed as your code is ported from QY Classic to ROM QYx.

- Does the application use the 3.2MHz internal oscillator?

  If so, the ICFS bits in the oscillator status and control register (OSCSC) can be changed by application software so the internal oscillator is set to 3.2 MHz after reset.
- Does the code use the auto wakeup timer and does the application depend on the typical auto wake timeout?

  Because timeout has been improved for ROM QYx, it may be necessary to modify software to compensate for the change in timeout.
- Bits changed in the OSCSC, CONFIG2, and ADC registers?

  Any code that writes to these registers should be reviewed to ensure the writes are not affecting the changed bits.
- Does the application use the 3V LVI reset?

  If so, the 3 V LVI reset setting now configures a 2 V LVI. If this is not acceptable for the application, a software LVI should be created.
- Does the code use the factory provided trim value at 0xFFC0?

  If so, the desired trim value needs to be selected on the ROM order form.

- Does the code use external OSC, crystal, or RC?

  If so, because the OSCOPT bits have changed locations, code has to be updated to update these bits in their proper locations.
- Does the code use the ADC?

  If so, because on ROM QYx the ADC clock is driven from 4XBUSCLK instead of BUSCLK, changes to the ADC clock divider bits may be needed to maintain proper operation.

5 Development Tools

Development hardware used for QYx can be used with ROM QYx. The ROM QYx is pin-for-pin compatible with QY Classic and can be placed on existing QY4 Classic hardware. However, the best device for creating application code for the ROM QYx is the HC908QY8. When using CodeWarrior IDE, create a new project selecting the HC908QY8. This allows you to create code for the ROM QYx device.

For in circuit debugging, existing cyclone/multilink tools and associated hardware can be used. You can achieve emulation by using the EML08QCBLTYE.

6 Differences in Packaging

All ROM QYx packages are lead free. All packages the QYx classic supported are not supported by the ROM QYx. The ROM QYx supports the 8-pin SOIC package, the 16-pin SOIC, and the TSSOP.

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