



# RF Power GaN Transistor

This 32 W RF power GaN transistor is designed for cellular base station applications covering the frequency range of 1800 to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 1800 to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

## 2100 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 48$  Vdc,  $I_{DQ} = 150$  mA,  $P_{out} = 32$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	19.6	38.0	7.2	-30.3	-20
2140 MHz	19.9	38.3	7.1	-30.0	-23
2170 MHz	20.0	39.0	7.1	-29.7	-19

## 1800 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 48$  Vdc,  $I_{DQ} = 150$  mA,  $P_{out} = 32$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

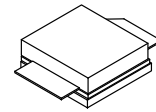
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.2	36.9	7.1	-33.4	-11
1840 MHz	18.5	37.4	7.1	-33.0	-16
1880 MHz	18.6	38.2	7.0	-32.5	-16

## Features

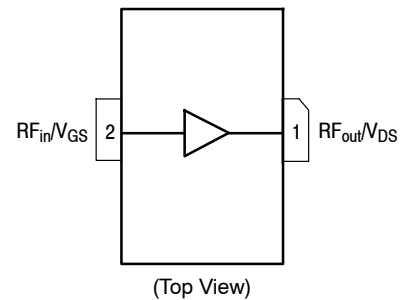
- High Terminal Impedances for Optimal Broadband Performance
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

**A2G22S160-01SR3**

**1800–2200 MHz, 32 W AVG., 48 V  
 AIRFAST RF POWER GaN  
 TRANSISTOR**



**NI-400S-2S**



**Figure 1. Pin Connections**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	125	Vdc
Gate-Source Voltage	$V_{GS}$	-8, 0	Vdc
Operating Voltage	$V_{DD}$	0 to +55	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-55 to +150	°C
Operating Junction Temperature Range (1)	$T_J$	-55 to +225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 32 W CW, 48 Vdc, $I_{DQ} = 150$ mA, 2140 MHz	$R_{\theta JC}$	1.7	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22- A114)	1B
Machine Model (per EIA/JESD22- A115)	A
Charge Device Model (per JESD22- C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Drain-Source Leakage Current ( $V_{GS} = -8$ Vdc, $V_{DS} = 55$ Vdc)	$I_{DSS}$	—	—	5	mAdc
Drain-Source Breakdown Voltage ( $V_{GS} = -8$ Vdc, $I_D = 16.2$ mAdc)	$V_{(BR)DSS}$	150	—	—	Vdc

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 16.2$ $\mu$ Adc)	$V_{GS(th)}$	-3.8	-3.0	-2.3	Vdc
Gate Quiescent Voltage ( $V_{DD} = 48$ Vdc, $I_D = 150$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	-3.6	-3.0	-2.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1)</sup> (In NXP Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$ , $I_{DQ} = 150\text{ mA}$ , $P_{out} = 32\text{ W Avg.}$ , $f = 2110\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset. <b>[See note on correct biasing sequence.]</b>					
Power Gain	$G_{ps}$	18.8	19.6	21.8	dB
Drain Efficiency	$\eta_D$	35.5	38.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-30.3	-28.0	dBc
Input Return Loss	IRL	—	-20	-9	dB

**Load Mismatch** (In NXP Test Fixture, 50 ohm system)  $I_{DQ} = 150\text{ mA}$ ,  $f = 2140\text{ MHz}$ 

VSWR 10:1 at 55 Vdc, 125 W CW Output Power (3 dB Input Overdrive from 125 W CW Rated Power)	No Device Degradation
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**Typical Performance** (In NXP Test Fixture, 50 ohm system)  $V_{DD} = 48\text{ Vdc}$ ,  $I_{DQ} = 150\text{ mA}$ , 2110–2170 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	125	—	W
$P_{out}$ @ 3 dB Compression Point <sup>(2)</sup>	P3dB	—	160	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	$\Phi$	—	-21.8	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	150	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 32\text{ W Avg.}$	$G_F$	—	0.4	—	dB
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.02	—	dB/°C
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta P_{1dB}$	—	0.02	—	dB/°C

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A2G22S160-01SR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13- inch Reel	NI-400S-2S

1. Part internally input matched.

2. P3dB =  $P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.**NOTE: Correct Biasing Sequence for GaN Depletion Mode Transistors****Turning the device ON**

1. Set  $V_{GS}$  to the pinch-off ( $V_P$ ) voltage, typically  $-5\text{ V}$
2. Turn on  $V_{DS}$  to nominal supply voltage (50 V)
3. Increase  $V_{GS}$  until  $I_{DS}$  current is attained
4. Apply RF input power to desired level

**Turning the device OFF**

1. Turn RF power off
2. Reduce  $V_{GS}$  down to  $V_P$ , typically  $-5\text{ V}$
3. Reduce  $V_{DS}$  down to 0 V (Adequate time must be allowed for  $V_{DS}$  to reduce to 0 V to prevent severe damage to device.)
4. Turn off  $V_{GS}$

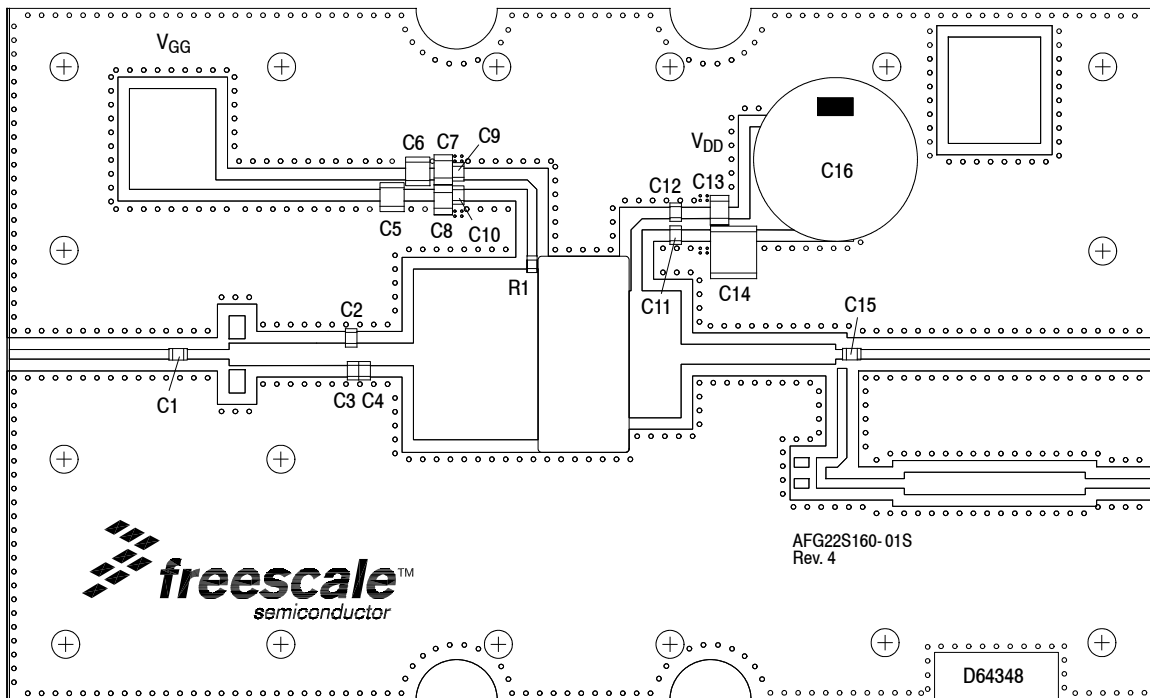


Figure 2. A2G2S160-01SR3 Test Circuit Component Layout — 2110–2170 MHz

Table 6. A2G2S160-01SR3 Test Circuit Component Designations and Values — 2110–2170 MHz

Part	Description	Part Number	Manufacturer
C1, C9, C10, C11, C12, C15	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C2, C3	1.8 pF Chip Capacitors	ATC600F1R8BT250XT	ATC
C4	1.2 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C5	470 pF Chip Capacitor	ATC100B471JT200XT	ATC
C6	1000 pF Chip Capacitor	ATC100B102JT50XT	ATC
C7, C13	1 $\mu$ F Chip Capacitors	GRM32ER72A105KA01L	Murata
C8	10 $\mu$ F Chip Capacitor	GRM31CR61H106KA12L	Murata
C14	10 $\mu$ F Chip Capacitor	C5750X7S2A106M230KB	TDK
C16	220 $\mu$ F, 100 V Electrolytic Capacitor	EEV-FK2A221M	Panasonic-ECG
R1	2.37 $\Omega$ , 1/4 W Chip Resistor	CRCW12062r37FNEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D64348	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHz

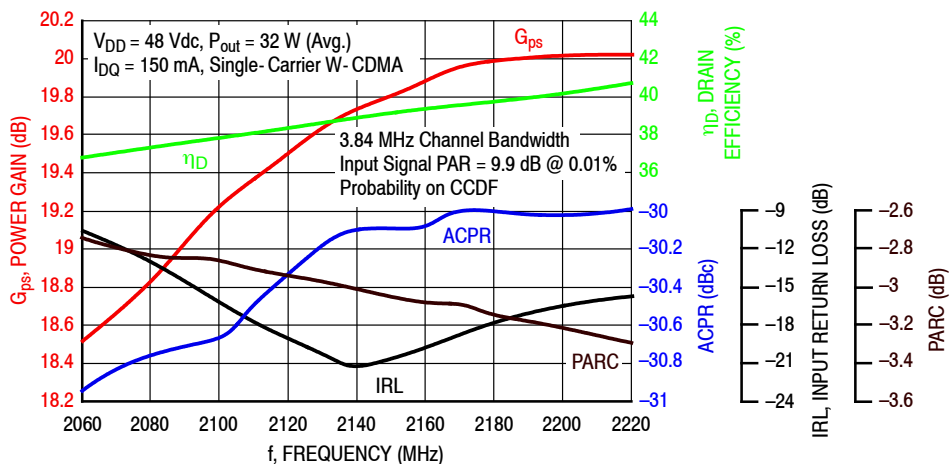


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P<sub>out</sub> = 32 Watts Avg.

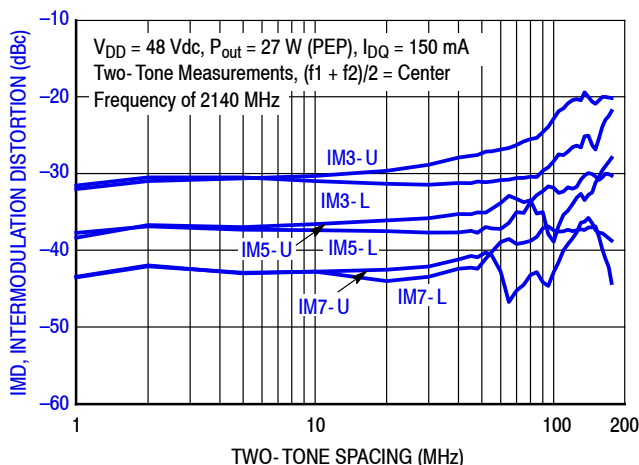


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

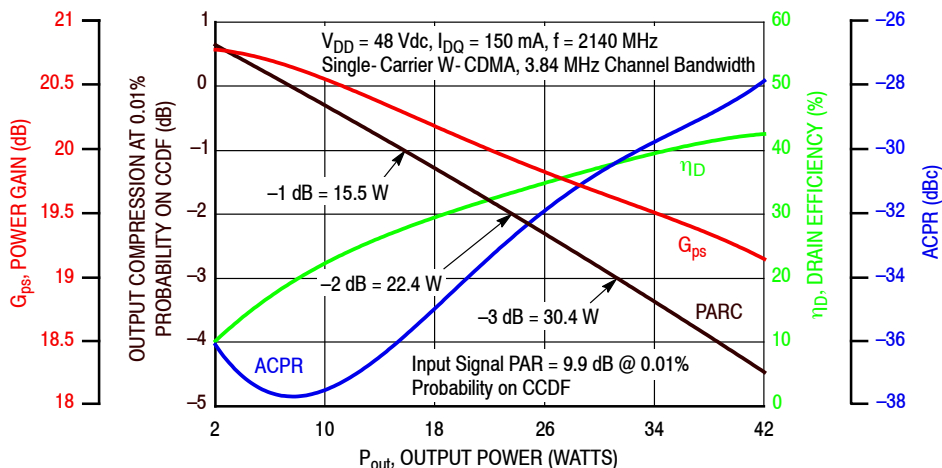


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

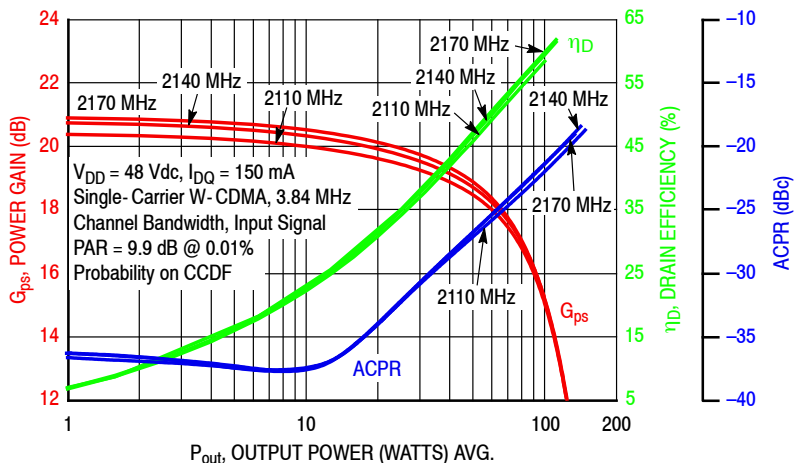


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

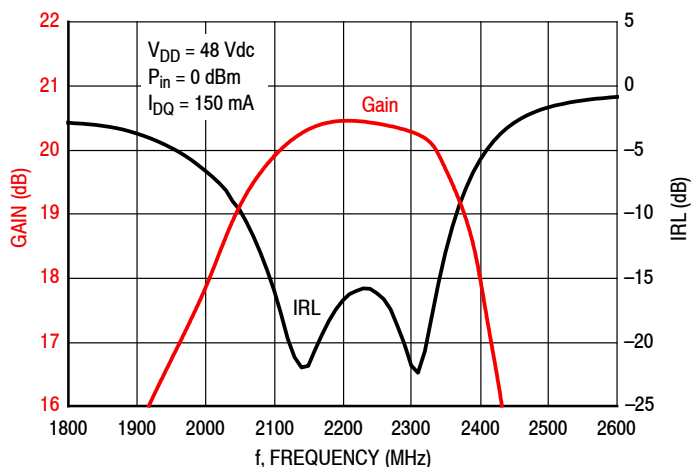


Figure 7. Broadband Frequency Response

**Table 7. Load Pull Performance — Maximum Power Tuning** $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 136 \text{ mA}$ , Pulsed CW,  $10 \mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	$4.15 - j6.27$	$5.00 + j5.62$	$8.53 - j8.62$	20.2	50.3	106	52.3	-24
2140	$4.07 - j5.17$	$4.98 + j4.73$	$10.0 - j9.31$	20.2	50.4	110	52.9	-26
2170	$4.09 - j4.55$	$4.50 + j4.20$	$12.0 - j9.99$	19.9	50.3	108	53.2	-18

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	$4.15 - j6.27$	$5.06 + j5.47$	$10.3 - j7.91$	18.0	51.7	147	61.3	-28
2140	$4.07 - j5.17$	$5.10 + j4.68$	$10.6 - j8.37$	18.2	51.7	148	61.1	-29
2170	$4.09 - j4.55$	$4.76 + j3.87$	$12.0 - j9.08$	18.2	51.8	150	60.8	-21

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

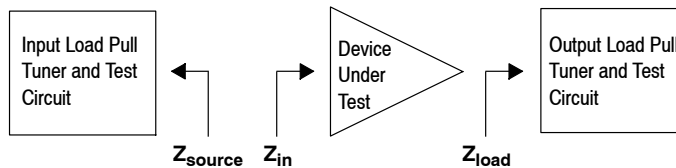
 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane. $Z_{\text{in}}$  = Impedance as measured from gate contact to ground. $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.**Table 8. Load Pull Performance — Maximum Drain Efficiency Tuning** $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 136 \text{ mA}$ , Pulsed CW,  $10 \mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	$4.15 - j6.27$	$6.23 + j5.33$	$6.50 - j4.70$	21.9	49.3	86	60.3	-25
2140	$4.07 - j5.17$	$7.85 + j2.84$	$4.69 - j4.08$	23.1	48.5	71	61.5	-31
2170	$4.09 - j4.55$	$4.69 + j3.48$	$9.05 - j4.91$	21.6	49.2	83	59.6	-15

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2110	$4.15 - j6.27$	$6.45 + j3.06$	$5.89 - j2.96$	20.8	49.9	97	72.2	-34
2140	$4.07 - j5.17$	$5.06 + j2.23$	$6.46 - j2.95$	21.0	49.9	99	72.8	-29
2170	$4.09 - j4.55$	$4.10 + j2.54$	$8.12 - j3.23$	20.2	50.4	110	71.1	-22

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane. $Z_{\text{in}}$  = Impedance as measured from gate contact to ground. $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

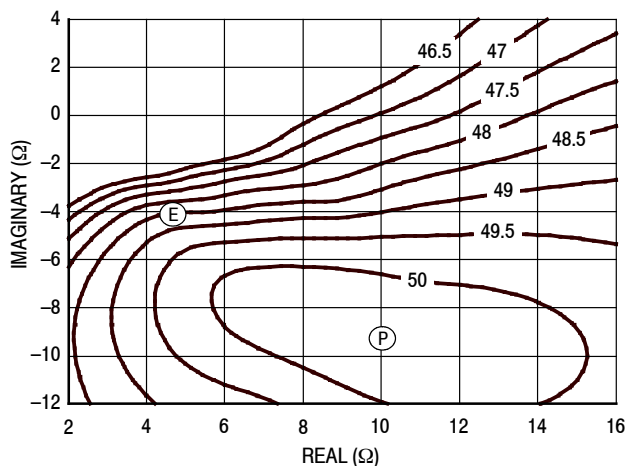


Figure 8. P1dB Load Pull Output Power Contours (dBm)

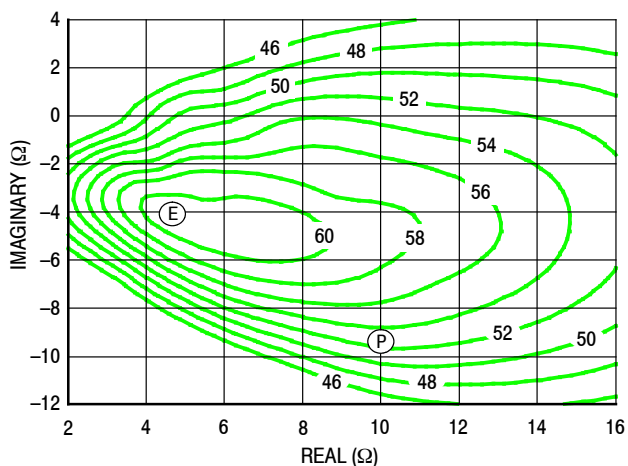


Figure 9. P1dB Load Pull Efficiency Contours (%)

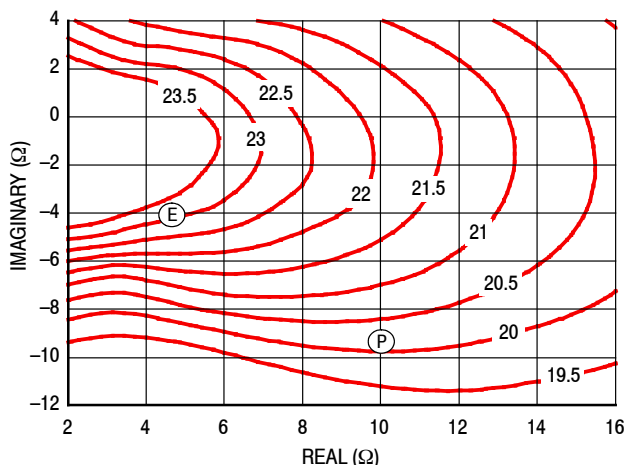


Figure 10. P1dB Load Pull Gain Contours (dB)

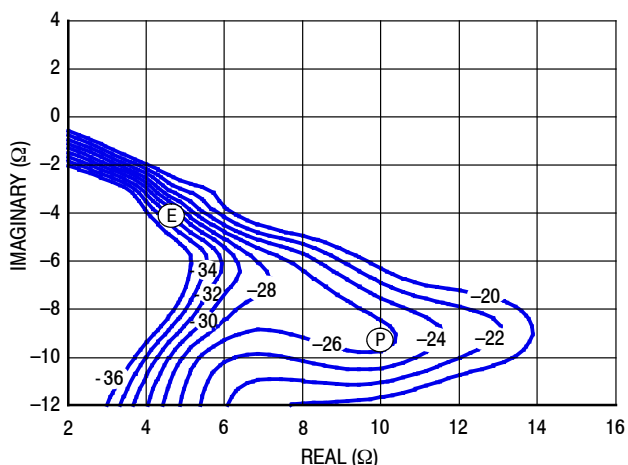


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power



### P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

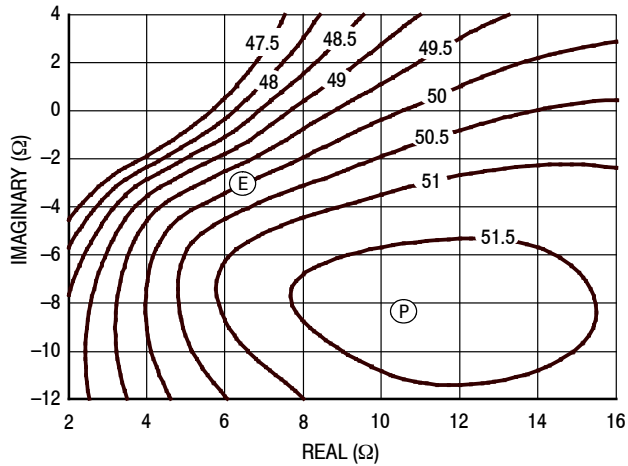


Figure 12. P3dB Load Pull Output Power Contours (dBm)

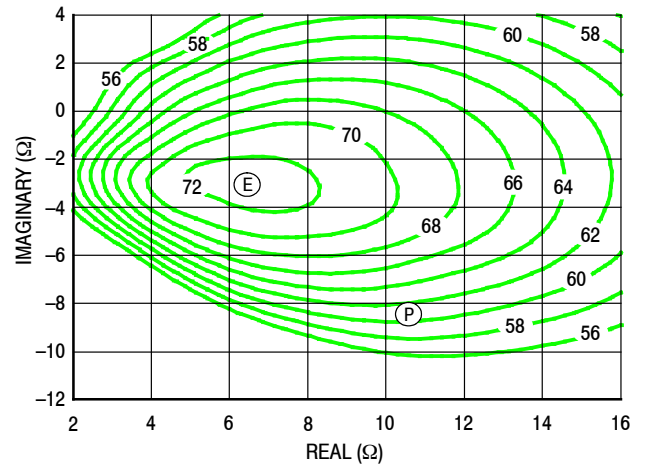


Figure 13. P3dB Load Pull Efficiency Contours (%)

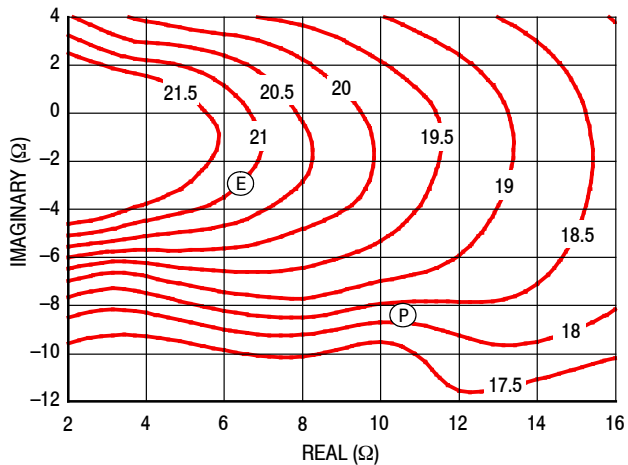


Figure 14. P3dB Load Pull Gain Contours (dB)

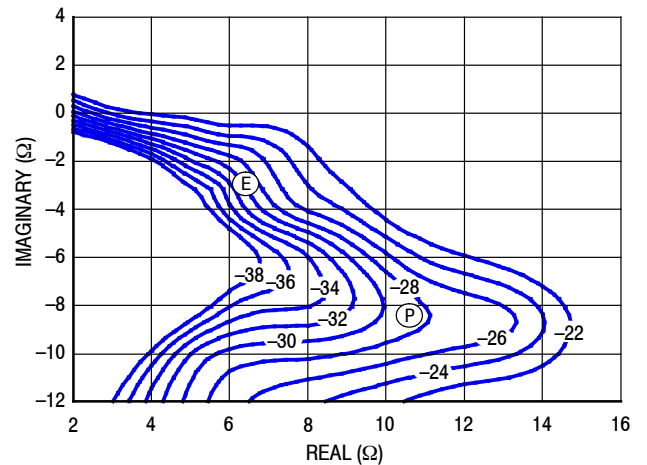


Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

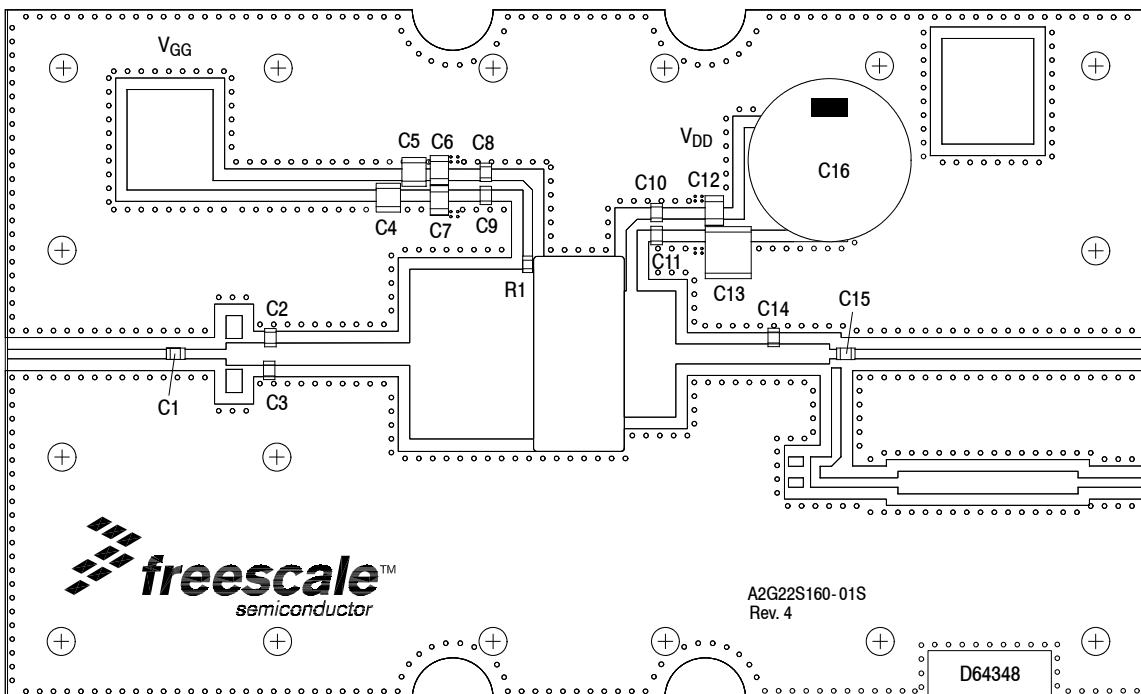
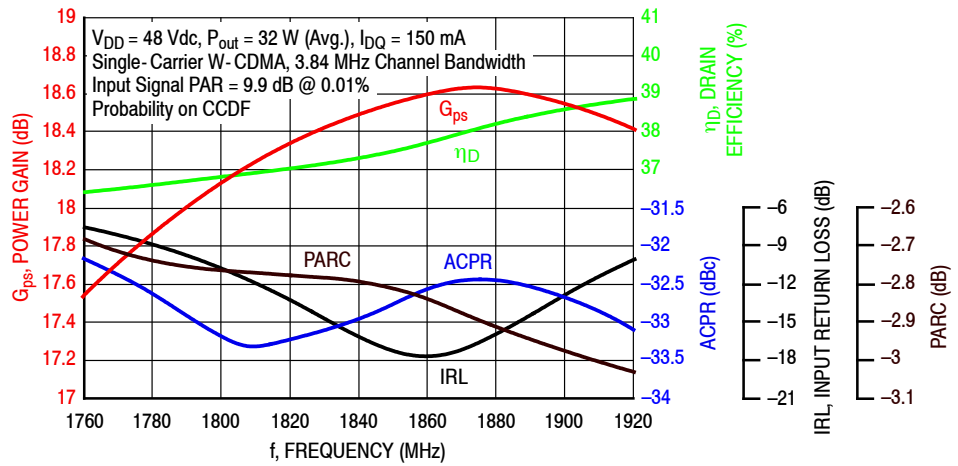


Figure 16. A2G22S160-01SR3 Test Circuit Component Layout — 1805–1880 MHz

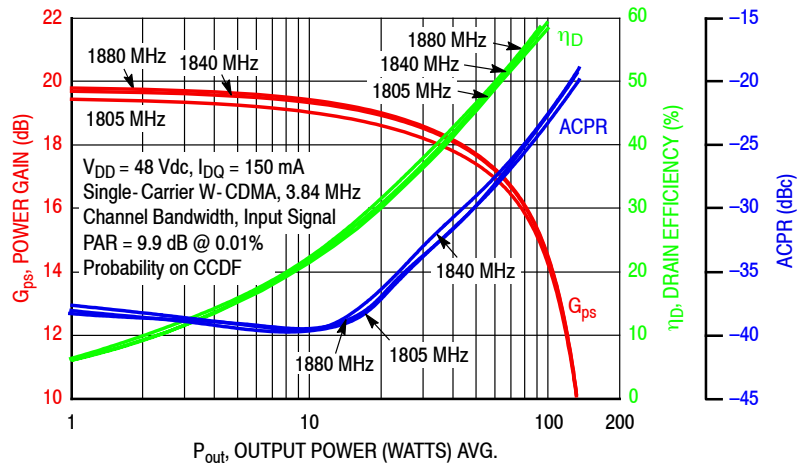
Table 9. A2G22S160-01SR3 Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1, C8, C9, C10, C11, C15	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C2	1.1 pF Chip Capacitor	ATC600F1R2BT250XT	ATC
C3	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C4	470 pF Chip Capacitor	ATC100B471JT200XT	ATC
C5	1000 pF Chip Capacitor	ATC100B102JT50XT	ATC
C6, C12	1 $\mu$ F Chip Capacitors	GRM32ER72A105KA01L	Murata
C7	10 $\mu$ F Chip Capacitor	GRM31CR61H106KA12L	Murata
C13	10 $\mu$ F Chip Capacitor	C5750X7S2A106M230KB	TDK
C14	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C16	220 $\mu$ F, 100 V Electrolytic Capacitor	EEV-FK2A221M	Panasonic-ECG
R1	2.37 $\Omega$ , 1/4 W Chip Resistor	CRCW12062R37FNEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D64348	MTL

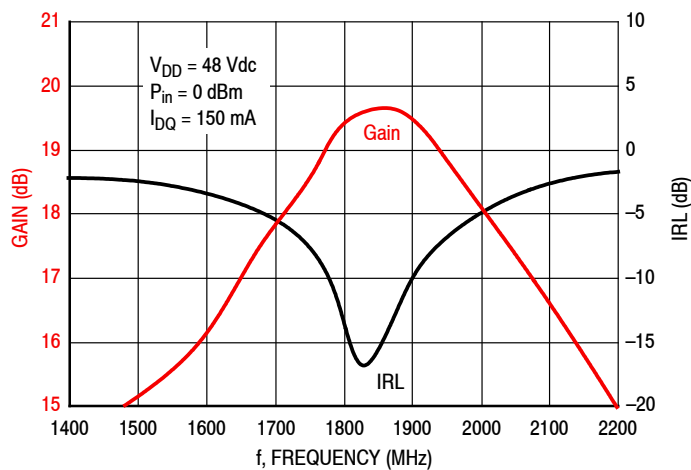
### TYPICAL CHARACTERISTICS — 1805–1880 MHz



**Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 32$  Watts Avg.**



**Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 19. Broadband Frequency Response**

**Table 10. Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQ} = 140$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.26 – j5.77	1.57 + j5.91	8.58 – j5.21	19.9	51.6	145	60.9	–41
1840	1.64 – j5.93	1.84 + j6.11	9.10 – j5.90	19.9	51.4	137	59.2	–38
1880	1.97 – j6.03	2.06 + j6.39	8.40 – j6.54	19.7	51.1	129	56.5	–34

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.26 – j5.77	1.46 + j5.88	9.56 – j3.93	18.3	52.2	167	68.4	–34
1840	1.64 – j5.93	1.64 + j6.03	9.50 – j4.67	17.7	52.1	163	67.1	–32
1880	1.97 – j6.03	1.98 + j6.41	9.42 – j5.46	17.8	51.9	156	64.2	–29

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 11. Load Pull Performance — Maximum Drain Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQ} = 140$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.26 – j5.77	1.51 + j6.34	6.08 – j0.80	21.8	50.3	107	70.2	–38
1840	1.64 – j5.93	1.71 + j6.74	5.51 – j1.09	22.1	50.0	100	69.9	–36
1880	1.97 – j6.03	2.05 + j7.16	5.18 – j1.44	22.1	49.6	92	68.8	–34

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1805	1.26 – j5.77	1.58 + j6.43	6.86 – j0.08	20.0	51.2	130	77.2	–36
1840	1.64 – j5.93	1.91 + j6.84	6.28 – j0.28	20.3	50.8	120	77.5	–35
1880	1.97 – j6.03	2.42 + j7.30	5.75 – j0.50	20.3	50.3	108	77.0	–37

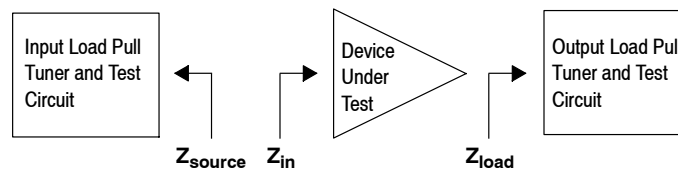
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.



## P1dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

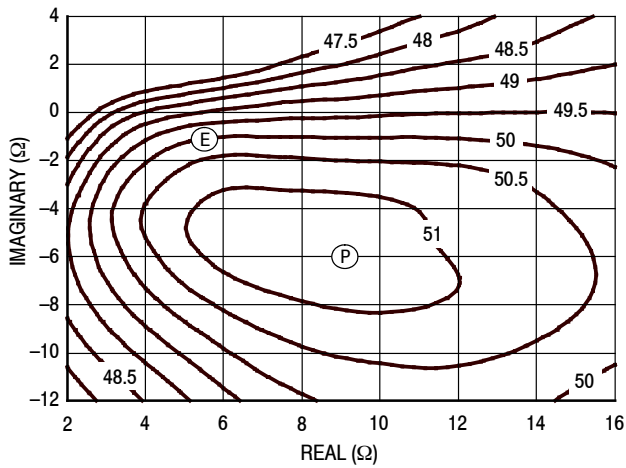


Figure 20. P1dB Load Pull Output Power Contours (dBm)

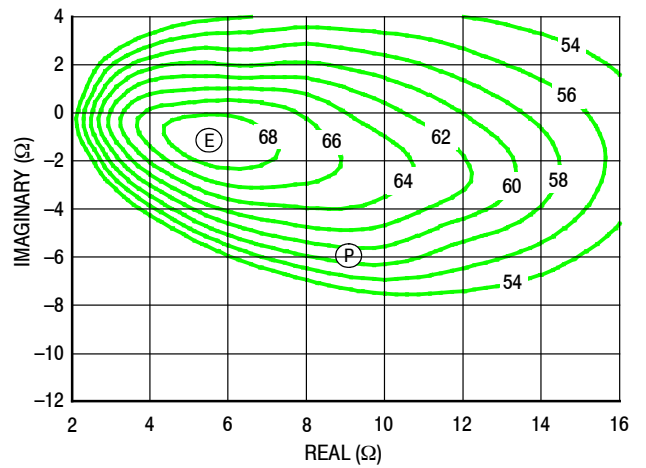


Figure 21. P1dB Load Pull Efficiency Contours (%)

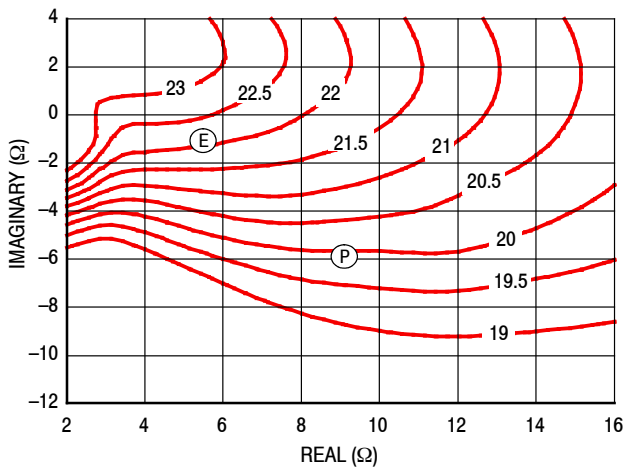


Figure 22. P1dB Load Pull Gain Contours (dB)

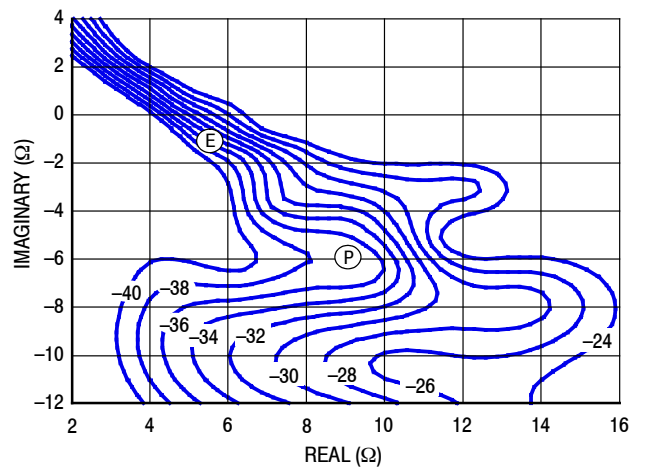


Figure 23. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

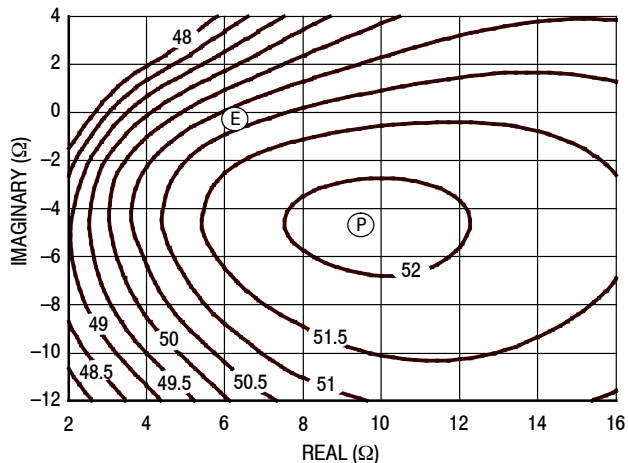


Figure 24. P3dB Load Pull Output Power Contours (dBm)

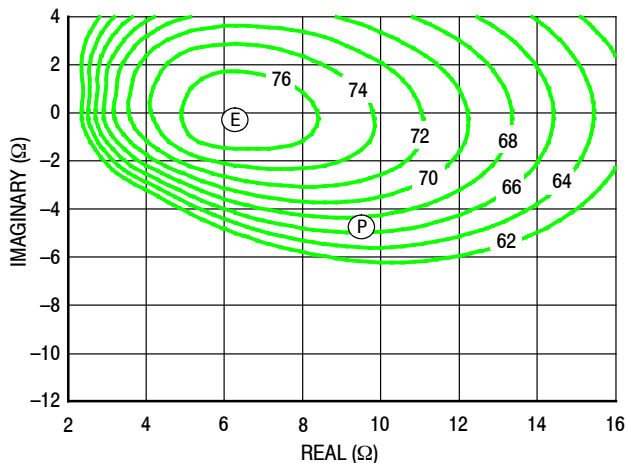


Figure 25. P3dB Load Pull Efficiency Contours (%)

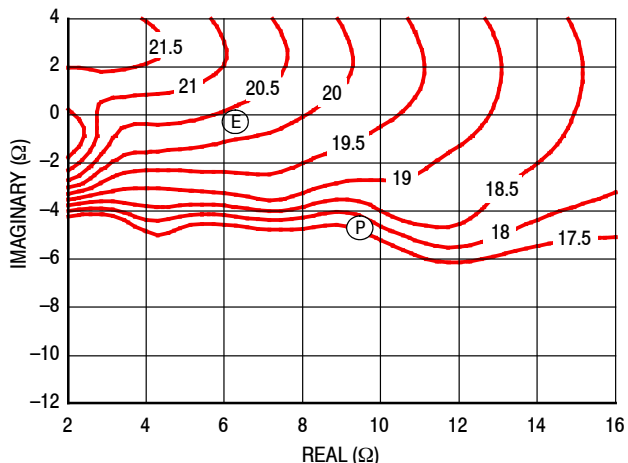


Figure 26. P3dB Load Pull Gain Contours (dB)

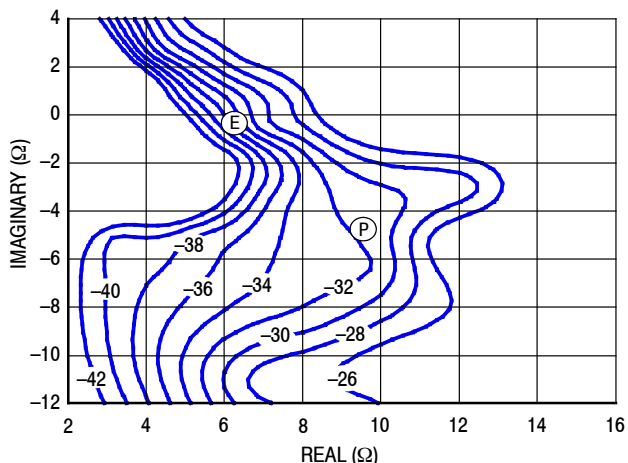
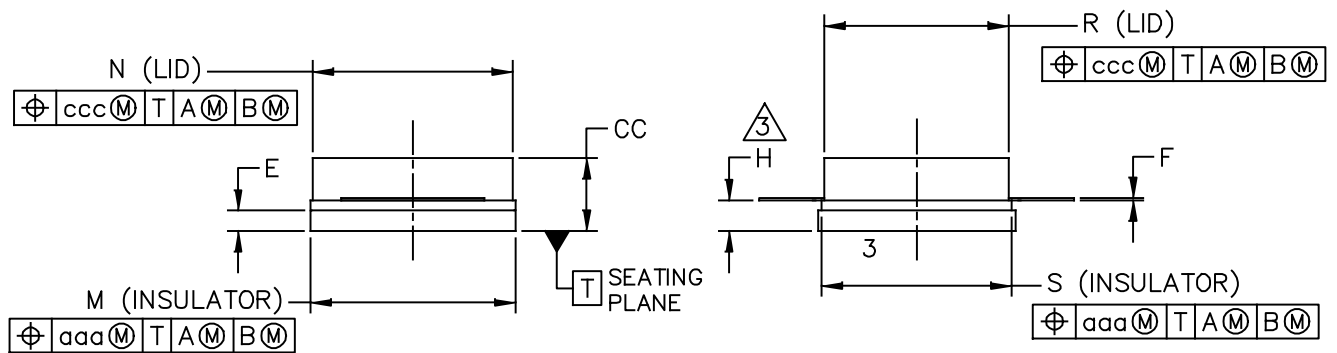
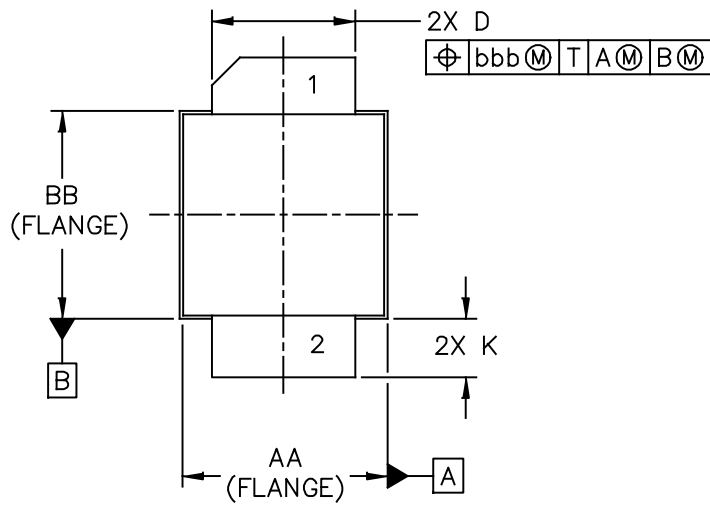


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

## PACKAGE INFORMATION



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TITLE:  NI-400S-2S	DOCUMENT NO: 98ASA10732D	REV: C
	STANDARD: NON-JEDEC	
	SOT1828-1	13 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

③ DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM THE FLANGE TO CLEAR THE EPOXY FLOW OUT REGION PARALLEL TO DATUM B.

4. INPUT & OUTPUT LEADS (PIN 1 & 2) MAY HAVE SMALL FEATURES SUCH AS SQUARE HOLES OR NOTCHES FOR MANUFACTURING CONVENIENCE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.395	.405	10.03	10.29	aaa	.005		0.13	
BB	.382	.388	9.70	9.86	bbb	.010		0.25	
CC	.125	.163	3.18	4.14	ccc	.015		0.38	
D	.275	.285	6.98	7.24					
E	.035	.045	0.89	1.14					
F	.004	.006	0.10	0.15					
H	.057	.067	1.45	1.70					
K	.0995	.1295	2.53	3.29					
M	.395	.405	10.03	10.29					
N	.385	.395	9.78	10.03					
R	.355	.365	9.02	9.27					
S	.365	.375	9.27	9.53					
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TITLE:  NI-400S-2S					DOCUMENT NO: 98ASA10732D		REV: C		
					STANDARD: NON-JEDEC				
					SOT1828-1		13 JAN 2016		

Note: Input and output leads (pin 1 and pin 2) have a small square hole that is used as a reference location in the manufacturing process.



## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- RF High Power Model
- s2p File

### Development Tools

- Printed Circuit Boards

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	<ul style="list-style-type: none"><li>• Initial release of data sheet</li></ul>
1	Jan. 2022	<ul style="list-style-type: none"><li>• Package Outline Drawing: 98ASA10732D package outline updated to Rev. C, pp. 15–16; added a note describing package feature used for manufacturing process, p. 16.</li></ul>

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