NXP 2/4/8/16-bit I²C/SMBus LED dimmers PCA9530/31/32/33

LED dimming with GPIO expansion

These I²C/SMBus-compatible GPIO expanders, optimized for dimming LEDs, support two user-programmable blink and dimming rates, programmable up to 256 levels of brightness, without overloading the I²C-bus or tying up the I²C-bus master.

Key features

- Compatible with I²C-bus and SMBus
- Two user-programmable blink rates and duty cycles
  - Blink rate: 0.625 to 1.6 sec (160 to 0.656 Hz)
  - Duty cycle: 0 to 99.6% allows fade to black
- 256 programmable brightness levels
- Internal oscillator accurate to ±10% and requires no external components
- Open-drain outputs can drive LEDs directly (25 mA max sink per bit)
- High maximum device limits (50, 100, or 200 mA)
- I/O states readable via I²C/SMBus
- Any bit not used to drive an LED can be used as normal GPIO
- Active-low hardware reset saves power and simplifies design
- Low standby current (ISTB): 1.5 µA (max)
- Operating voltage: 2.3 to 5.5 V
- All I/O tolerant to 5.5 V
- Temperature range: -40 to +85 °C
- I²C-bus clock frequency: 0 to 400 kHz
- ESD protection exceeds JEDEC standards
- High-volume CMOS process
- Package options: SO, TSSOP, HVQFN

Applications

- LED backlighting
- LED color mixing
- LED status

The NXP PCA9530, PCA9531, PCA9532, and PCA9533 are used to dim LEDs in I²C-bus and SMBus applications. Each LED can be off, on, or set to two different blink or dim settings (with 256 levels of control), without overloading the I²C-bus or tying up the I²C-bus master.

The blink rate can vary from 0.625 to 1.6 seconds (160 to 0.625 Hz) in 256 steps. The duty cycle is programmable in 256 steps. To dim the LEDs, change the duty cycle between 0% (dark) and 99.6% (bright) when the frequency is set to 160 Hz.

Any bits that aren't used to control LEDs can be used as general-purpose I/O (GPIO), for a quick, easy to add sensors, push-buttons, alarm monitors, LEDs, fans, and more.

On the PCA9531 and PCA9532, three hardware pins (A0, A1, As) let up to eight identical devices share the same I²C/SMBus. On the PCA9530, a single hardware pin (A0), supports up to two devices on the same I²C/SMBus. Due to hardware pin

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limitations, the PCA9533 doesn't have address pins so only one is allowed on the bus.

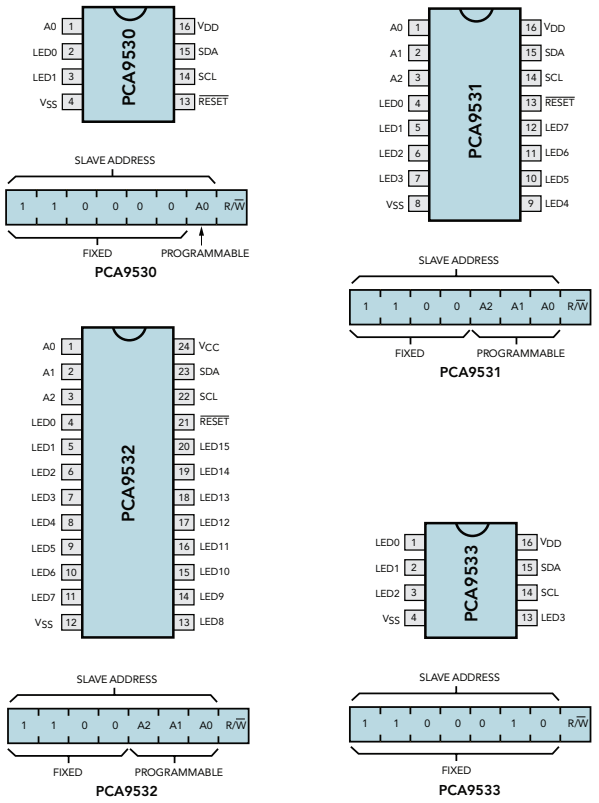
Each device features open-drain outputs that sink 25 mA per bit. The PCA9530 supports a maximum of 50 mA, the PCA9531 and PCA9533 a maximum of 100 mA, and the PCA9532 a maximum of 200 mA (100 mA per 8-bit group).

On the PCA9530, PCA9531, and PCA9532, an external active-low reset hardware pin ($\overline{\text{RESET}}$) returns registers to their default states, without having to cycle power to the equipment, if the I²C-bus locks up.

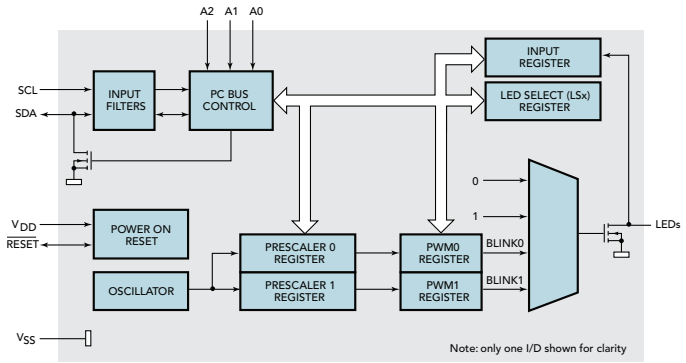
ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101. JESDEC Standard JESD78 latch-up testing exceeds 100 mA.

Except for the number of bits and address pins, the functional diagram and I/O schematic are the same for all of the devices.

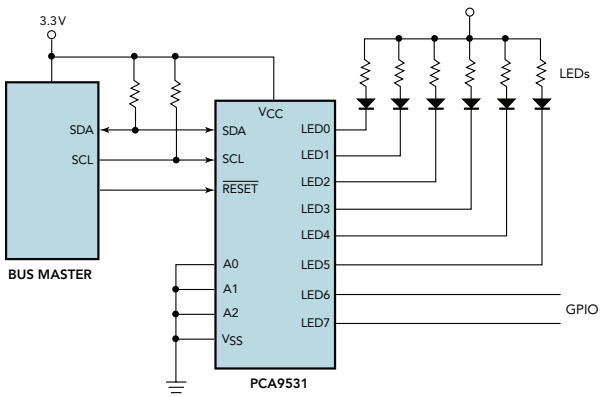
More information on NXP LED blinkers and dimmers can be found in application note AN264.



Pin configurations



Block diagram



Typical application

Order information

Package	Container	PCA9530	PCA9531	PCA9532	PCA9533/01
SO	Tube T&R	PCA9530D PCA9530D-T	PCA9531D PCA9531D-T	PCA9532D PCA9532D-T	PCA9533D/01 PCA9533D/01-T
TSSOP	Tube T&R	PCA9530DP-T	PCA9551PW PCA9531PW-T	PCA9532PW PCA9532PW-T	PCA9533DP/01-T
HVQFN	T&R		PCA9531BS-T	PCA9532BS-T	

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