Freescale Semiconductor
Application Note

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Single Phase Two-Channel Interleaved PFC Operating in CrM

Using the MC56F82xxx Family of Digital Signal Controllers

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Contents

1 Introduction

This application note describes the digital implementation of an interleaved power factor correction (PFC) operating in boundary conduction mode (BCM) for the Freescale MC56F82xxx digital signal controllers (DSC). Peripherals available on this DSC enable easy implementation of power conversion applications.

Two-channel interleaved PFC operating in BCM (also called Critical conduction mode CrM) is used for low and middle power AC to DC conversion with compensating power factor (PF). Interleaved topology used to compare a single channel increases power density, reduces ripple currents, and improves overall efficiency.

The purpose of this application note is to describe in detail the implementation of BCM on the MC56F82316 and enable application engineers to speed up implementation of PFC.

This document includes the control scheme, the system design concept, peripheral configuration, and software design.

The MC56F82316 is member of DSC family which is based on the 56800E core. The primary advantages and features of this controller are described in the following section.

2 MC56F82316 DSC advantages and features

The MC56F82xxx digital signal controller family combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, it is well-suited for many applications. The MC56F82316 includes many peripherals, that are suitable for cost-sensitive applications.

The MC56F82316 provides the following peripherals:

- 32-bit 56800EX core–50 MIPS at 50 MHz core frequency
- 16KB flash memory, 4KB RAM
- One flex pulse width modulator (eFlexPWM) with 8 PWM outputs
- Two independent high-speed, 5-channel, 12-bit analog-to-digital converters (ADCs)
- Two inter-crossbar switches (XBAR)
- Three analog comparators (HSCMPs) with integrated 6-bit DAC reference
- Two 12-bit digital-to-analog converters (12-bit DAC)
- One 4-channel, 16-bit multi-purpose timer (TMR) module
- Two periodic interval timers (PITs)
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
- One queued serial peripheral interface (QSPI) module
- One inter-integrated circuit (I^2C) port
- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
- Power supervisor (PS)
- Phase-lock loop (PLL) providing a high-speed clock to the core and peripherals
- Clock source
- Cyclic redundancy check (CRC) generator
- External watchdog monitor (EWM)
- DMA controller
- JTAG EOnCE debug programming interface for real-time debugging

The interleaved two-channel PFC system benefits from the eFlexPWM module, the high-speed comparator (HSCMP) module, the timer (TMR) module, and the analog-to-digital converters (ADC). These modules provide configuration flexibility to enable efficient two-channel interleaved PFC control in boundary conduction mode. The configuration of each peripheral is described in Section 4.4, “Peripheral configuration.”

3 Interleaved PFC control scheme

The system interleaving and key waveforms are shown in Figure 1. Each switch is turned on when the inductor current reaches zero. High current and voltage ripples are available during the BCM operation. The interleaving operation is used to reduce current and voltage stress. For converters operating in critical conduction mode the interleaving is complicated to perform due to the converter’s variable switching

frequency. The interleaving signal can be generated from the turn-on or turn-off signal by shifting these signals with half of the switching period. The interleaving control scheme used here shifts the slave's turn-on signal to achieve interleaving. The master phase is turned-on by zero current detectors. Turn-on time is given by the voltage controller. It is presumed that the difference between the two adjacent switching periods can be omitted. When the converter is operating with high switching frequency, this assumption is feasible. The slave leg time shift is therefore calculated from previous switching period.

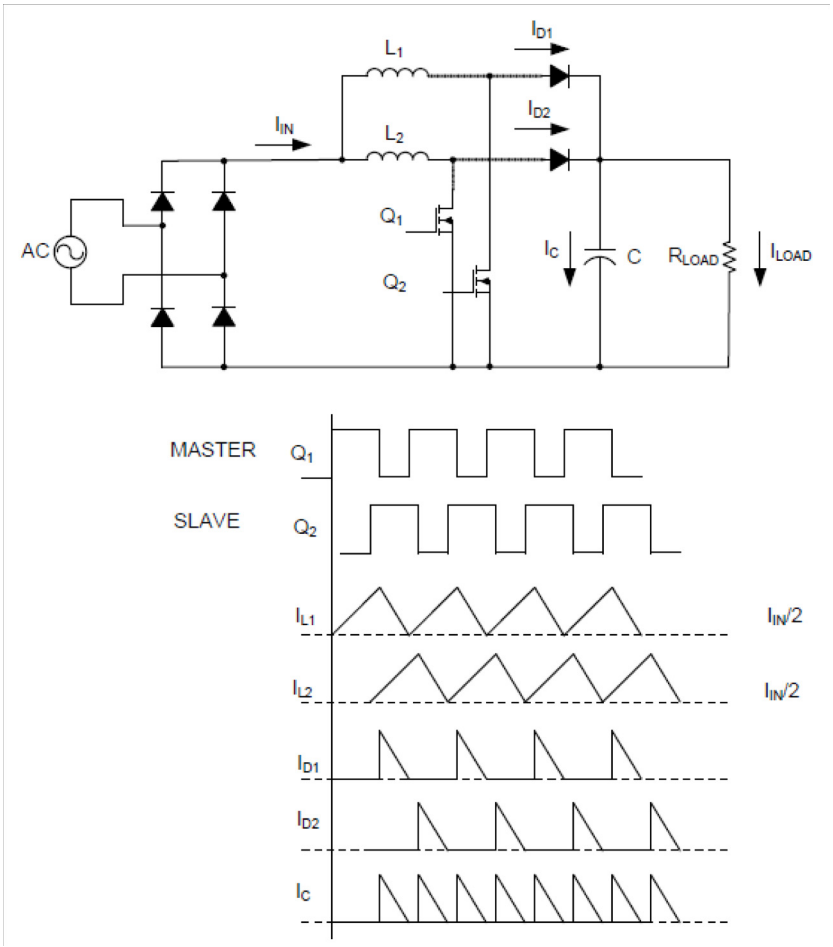


Figure 1. Signal interleaving and key waveforms

The slave leg switch is turned-on by shifting the driving signal at about half of the switching period. Turn-on times for both legs are nearly identical. If the slave leg has different parameters than the master, the slave leg might be operating in continuous conduction mode (CCM) or discontinuous mode (DCM). However, CCM operation is undesirable. An algorithm for master or slave leg identification is used to satisfy master leg operation in the CrM and slave leg operation in CrM or when operating in DCM.

Because the inductor currents are 180 degrees out of phase, they cancel each other to reduce the input ripple current. The input ripple current and the inductor current vary with the duty cycle change. Duty cycle of the step-up converter operating from AC input voltage varies with the voltage. Based on this, the inductor ripple current cancellation will not be 100% in the entire AC grid period within the PFC circuit.

The inductor ripple current cancellation enables reduction of the boost inductor size. This is due to the energy storage requirement of the two interleaved inductors being half that of a single stage converter designed for the same parameters.

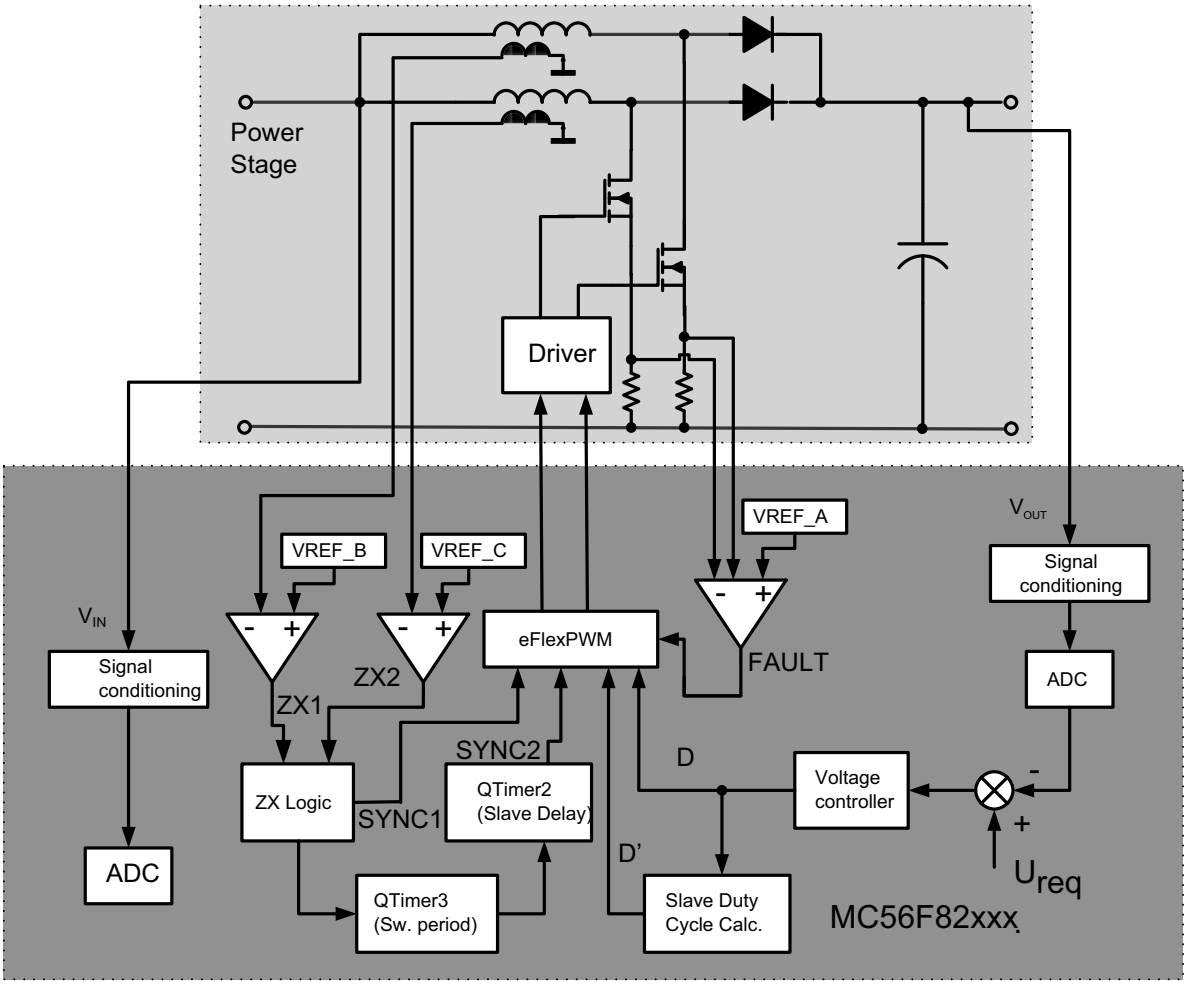
Interleaving reduces the output capacitor ripple current as a function of duty cycle. Because the duty cycle is 0 percent, 50 percent, and 100 percent, the sum of the two diode currents approaches the DC. Therefore, the output capacitor must only filter the inductor ripple current. This reduction in RMS current will reduce electrical stress in the output capacitor and improve the converter's reliability.

Because of these benefits, the power density of the system can be significantly increased. Small drawbacks of the interleaved approach are more components, and a more complicated control. However, these are not serious disadvantages when considering that the control algorithm is easily implemented and the component parameter limits are smaller.

4 System design concept

4.1 System architecture

The application system incorporates the high voltage power stage, signal conditioning, auxiliary power supply, and the MC56F82316 controller. The system design architecture is depicted in Figure 2.



ZX1, ZX2 – zero crossing signals
D – duty cycle MASTER
D' - duty cycle SLAVE
SYNC1 – MASTER synchronization signal
SYNC2 – SLAVE synchronization signal

Figure 2. System Design Architecture

As previously discussed, the power stage consists of two parallel connected boost converters operating in BCM. The interleaved boost converter contains twice the amount of components of a single boost converter and the control algorithm is more complex, however, the components are smaller, they operate with lower limits, are more efficient, and have an increased power density. The EMI filter and bridge rectifier are not described but they are necessary parts of the complete PFC circuit.

The sensing circuitries are used for sensing input voltage, output voltage, and assuring the controller reaches the acceptable voltage level.

The drivers are used for amplification of driving PWM signal for boost converters MOSFET transistors. The core of the control system is the MC56F82316 controller.

4.2 System specification

The application meets the following performance specifications:

- Hardware used:
  - Two parallel connected boost converters
- Control technique incorporated:
  - Constant on-time control (voltage control)
  - Voltage loop (32 kHz control frequency, variable switching frequency)
- Fault protection:
  - DC-bus under-voltage and over-voltage
  - Input under-voltage and over-voltage
  - Start-up fault
  - Overcurrent

4.3 System control process

The system control process describes the interleaved boost converter operation in master/slave mode. This determines that the next switching cycle in master leg begins immediately when the current reaches zero. The slave leg has nearly the same duty cycle as the master leg and the switching cycle is nearly the same, however, the slave leg driving signal is shifted by half of the switching period of the master leg driving signal. Accordingly, the system control is the same as for single-channel converter. The control of such a converter operating in voltage mode control is to control the output voltage and to maintain stability during load variation. Therefore, only one voltage control loop is required in the system control. To achieve good performance of the DC bus voltage loop, the PI controller is used. Figure 3 illustrates the system control scheme of a single-phase two-channel interleaved boost converter. After applying the AC input voltage, the filtered input voltage is checked for the limits. If it is within the limits, the master leg starts to switch with constant duty cycle to boost output voltage. When minimum bus voltage is reached the voltage controller is enabled and starts to minimize the voltage error between the reference bus voltage (e.g. 400 V) and the actual measured DC bus voltage. Based on the error, the voltage controller generates the duty cycle for both channels of the PWM. For the master leg, the PWM switching cycle begins at zero of the PWM timer and the slave switching cycle begins after half of the switching period of the master leg. When the DC bus required value is reached, then the DC bus controller maintains the output voltage at the required level.

As boost converter is operating in master/slave mode and to keep correct operation of the slave leg and to avoid continuous conduction mode operation the auxiliary computation is needed. Firstly, slave leg duty cycle signal is all the time slightly lower than master leg duty cycle. Difference is linearly proportional to the master leg duty cycle. Secondly, slave leg phase shift is calculated based on master leg duty cycle, input and output voltage and each 1ms during PWM update the slave leg is shifted about this value. Normally, the slave leg is shifted about half of the switching period of master leg each PWM update.

From Figure 3 you can see which peripherals are used for interleaved PFC operation and interconnection between these modules. The PWM submodule 2 and 3 is used for generating driving signals for MOSFET transistors. The PWM2B driving signal is used for switching master leg and PWM3B is driving signal for slave leg. The PWM2A

signal is auxiliary signal for correct operation of master leg in critical conduction mode. QTimer2 generate synchronization signal for PWM3 submodule and represent second leg phase shift signal. QTimer3 measure switching period of master leg. Second leg phase shift signal (SDC2) is computed based on switching period. Synchronization signal for QTimer3 and for PWM2 submodule is generated from AOI (AND-OR-INVERT) module by means of logical AND of PFC1_zero_crossing signal and auxiliary PWM2A signal. This synchronization signal represent true zero crossing signal for starting next switching cycle in master leg. Analog to Digital converter (ADC) sense input voltage and bus voltage. Input voltage filtered value is used for limit checking and therefore it is not displayed in control structure.

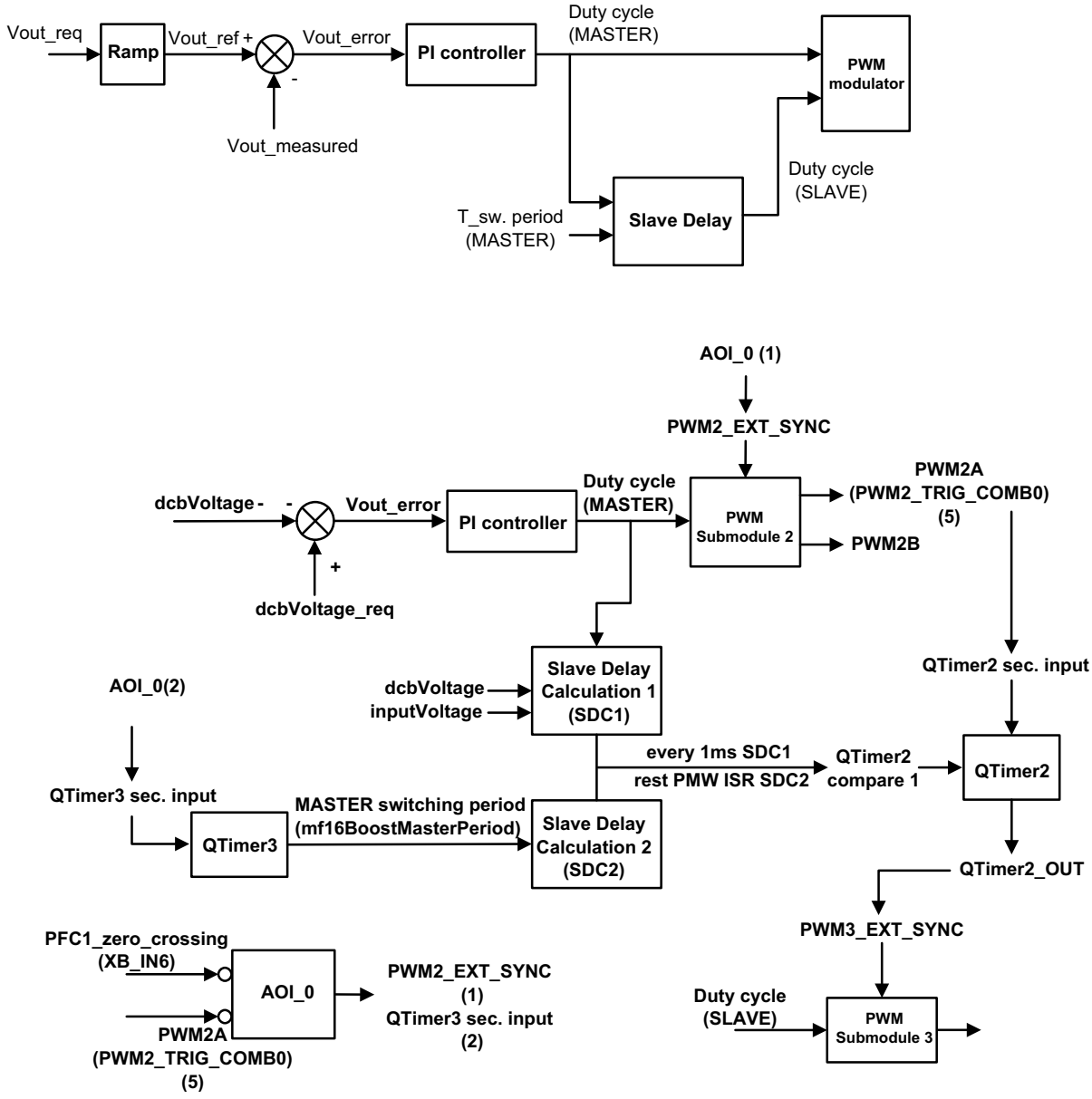


Figure 3. System Control Scheme

Because the converter is operating in either master or slave mode, an identification routine to determine between the two legs is required. This routine is executed during every start-up of the converter operation. The parameters of each leg of the boost converter are not exactly identical. The inductances, MOSFET transistors, resistors, and the control circuits which generate the PWM signals can vary and therefore generating the same PWM signals for each leg does not generated same output voltage. The master/slave identification routine identifies which converter leg switching period is longer for the same duty cycle to determine which is selected as the master leg.

During algorithm execution the hundreds values of the switching period are captured in Timer B0 for leg 1. The switching period is averaged and compared to the switching period for leg 2, which is then captured with Timer B1. The average switching period that is greater will be selected as the master leg. The master leg is then operating in critical conduction mode and the slave leg in discontinuous mode. This master/slave operation avoids operation of the slave leg in continuous conduction mode.

When both legs of the converter are operating, the slave leg is synchronized with master leg. The driving signal for the slave leg is the lagging master signal of about half of the switching period. In BCM the switching period can vary with each switching cycle when the software support is required for the correct operation of synchronization. The synchronization is based upon capturing the switching period of the master leg and shifting the slave leg turn-on pulse by half of switching period.

When output power is below 20% of nominal power, the slave leg stops operation and only the master leg is running. When power jumps above 40%, the second leg begins to operate.

Nominal power is proportional to the switching period and therefore the threshold values for operation—only one leg or both legs, are based on the switching period. The phase management is useful for operating during light loads when one leg can be disabled and a higher converter efficiency is reached.

4.4 Peripheral configuration

The presented application uses only essential peripherals for the control technique implemented in the application code—these are, QTIMER, XBAR_A, AOI, eFlexPWM, ADC, and HSCMP. Other peripherals are disabled. The Freescale QuickStart tool initializes these peripherals using a single interface for all settings. The following sections contain the configuration details of the peripherals. Figure 3 depicts the graphical interpretation of peripheral interconnection.

4.4.1 QTIMER

The MC56F82316 contains one timer module with four timers. Each timer can operate as a timer or as a counter. The counter provides the ability to count internal or external events. QTIMER_3 is used to operate in count mode, and counts the switching period of the MASTER leg of the boost converter. QTIMER_3 is configured as follows:

- Operate at a frequency of 100 MHz (IPB clock/1)
- Capture rising edges of input T0 (bus clock signal)
- Input capture on a secondary source
- Secondary source is AOI_0 output connected via XBAR_A

QTIMER_2 is used for slave leg phase shift. It is set to run in triggered mode until compare. The compare 1 value represents phase shift which is half of the switching period. QTIMER_2 is configured as follows:

- Operate at a frequency of 100 MHz (IPB clock/1)
- Output mode is set on compare, cleared on secondary source input edge
- Secondary source is PWMA2_TRIG0 connected via XBAR_A

4.4.2 XBAR_A

The crossbar switch module implements an array of 41 outputs and 32 inputs of combinational digital multiplexes. All 41 multiplexes share the same 32 inputs in the same order, however, each multiplex has its own independent select field. This module is designed to provide a flexible crossbar switching matrix that enables any input (typically from external GPIO or internal module outputs) to be connected to any output (typically to external GPIO or internal module inputs) under user control. This is used to enable user configuration of data paths between internal modules and between internal modules and GPIO.

The application configuration is as follows:

- Channel 12, ADCA Trigger:
  - PWM0_TRIG_COMB signal is used for ADC synchronization
- Channel 26, PWM submodule 0 external synchronization signal:
  - AOI_0 signal is used for PWM synchronization when boost converter leg 1 is master leg
- Channel 27, PWM submodule 1 external synchronization signal:
  - QTIMER_2 output is used for PWM synchronization when boost converter leg 2 is master leg
- Channel 31, PWM module Fault2:
  - CMPA_OUT log. 1 detects over-current on one or both boost legs
- Channel 36, Quad Timer 0 Input:
  - PWMA2_TRIG0 signal is used as secondary source input signal
- Channel 37, Quad Timer 1 Input:
  - AOI_0 signal is used as secondary source input signal

4.4.3 XBAR_B

XBAR_B implements an array of 26 inputs for AND-OR_INVERT (AOI) logic. XBAR_B is configured as follows:

- AOI EVENT0 input A is linked with XB_IN6
- AOI EVENT0 input B is linked with PWMA2_TRIG0

4.4.4 AND-OR_INVERT

AND-OR-INVERT module (AOI) provides boolean logic function operation among on-chip peripherals. Input signals are linked over XBAR_B module. AOI EVENT0 is used for generating external synchronization signal for boost master leg.

AOI is configured as follows:

- AOI EVENT0 input A is linked with XB_IN6 representing zero crossing signal from boost converter leg 1
- AOI EVENT0 input B is linked with auxiliary zero crossing signal (PWM2A)

4.4.5 eFlexPWM

Enhanced Flex Pulse Width Modulator is a dedicated peripheral enabling generation of driving PWM signals for MOSFET transistors (PWM submodules 2 and 3). PWM submodule 2 is used for application timing. PWM_B driving signal from PWM submodule 0 is used for driving MOSFET for leg 1 and PWM_A driving signal from PWM submodule 3 is used for driving MOSFET for leg 2.

Two PWM submodules are configured as follows:

- PWM submodule 0
  - Clock source IPBus clock
  - Running at constant frequency
  - INIT value = 0
  - VAL1 modulo 3332 - resolution 11bits
  - VAL 0 set to 1666
  - PWM full cycle reload generated every period (PWM interrupt)
  - Trigger 0 enabled to provide trigger signal for ADC
- PWM submodule 2/PWM submodule 3
  - Clock source IPBus clock
  - Running at variable frequency
  - INIT value = 0
  - VAL1 modulo 2499—resolution 11bits
  - Independent mode
  - PWM_B output in positive polarity is driving signal for MOSFET transistor
  - PWM middle cycle reload is generated every period
  - External synchronization signal is selected—see Section 4.4.2, “XBAR_A”
  - PWMA2 is selected as a trigger source for PWMA2_TRIG0
- PWM Fault2
  - Fault signals with high level detection
  - Fault clearing manual
  - Fault input filter disabled

4.4.6 ADC

The analog-to-digital (ADC) converter function consists of two separate 12-bit analog-to-digital converters, each with five analog inputs and its own sample and hold circuit.

Fast analog-to-digital converter module is configured as follow:

- Input clock IPBus/5 = 10 MHz
- Sample 0 set to DC-bus voltage–ANA3
- Sample 8 set to input voltage–ANB3
- Scan mode–triggered parallel
- Trigger source–SYNC0 input (PWM trigger connected via XBAR_A – channel 12)

4.4.7 HSCMP

The high speed comparator module (HSCMP) provides a circuit to compare two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation). Only one comparator is used for over-current detection.

- HSCMP_A
  - over-current detection in boost converter leg 1 and 2
  - 6-bit VREF_DAC is selected as a reference threshold for over-current detection

5 Software design

This section describes the software design of the one-phase two-channel interleaved PFC operating in BCM. The system processing is interrupt driven with the application state machine running in background. Code can be easily incorporated into the target application as a part of the whole system because the PFC application is independent of other tasks. The entire control algorithm was implemented in PWM interrupt service routine (ISR)—see Section 5.1, “PWM reload interrupt description” for details. Attention should be given to the correct timing of this algorithm if the PFC algorithm is implemented as a part of a more complex control system.

After a reset the application performs core, peripheral, and application initialization and then enters the endless (main()) loop. The application background main() loop contains the application state machine which incorporates six states:

- Init state
  - Application initialization
- Stop state
  - Checking all quantities except average input voltage if are within limits, and waiting for user input to start PFC
- VinCheck state
  - Average input voltage value checking and jumps to the Start state if within limits
- Start state
  - Master/slave identification
  - Boost converter switches with constant duty cycle and when dc bus voltage is over 200V then the voltage controller starts to regulate dc bus voltage to the required level (e.g. 400V) according to the load
- Run state

  - Normal operation—the voltage controller maintains the DC-bus voltage at the required level
- Error state
  - Disable PWM outputs in case of fault
  - When overcurrent or any other fault occurs, the application jumps to the Error state

5.1 PWM reload interrupt description

The entire control algorithm is performed in the PWM interrupt service routine. The control algorithm consists of the following:

- Read ADC quantities–input voltage, output voltage
- Input voltage average filter
- Slave leg delay calculation
- Voltage proportional-integral (PI) controller
- Correct CrM operation routine
- Slave duty cycle calculation
- Limit checking of all measured quantities
- Update to PWM registers

The PWM ISR is executed regularly every 32µs. ADC conversion begins in the middle of period defined by the VAL0 register for PWM submodule 0. Conversion runs in the background. Input voltage average filter, read ADC quantities and update PWM registers are executed at every interrupt. Rest algorithms are executed every 30th ISR (1ms). The PWM ISR flow chart is illustrated in Figure 4.

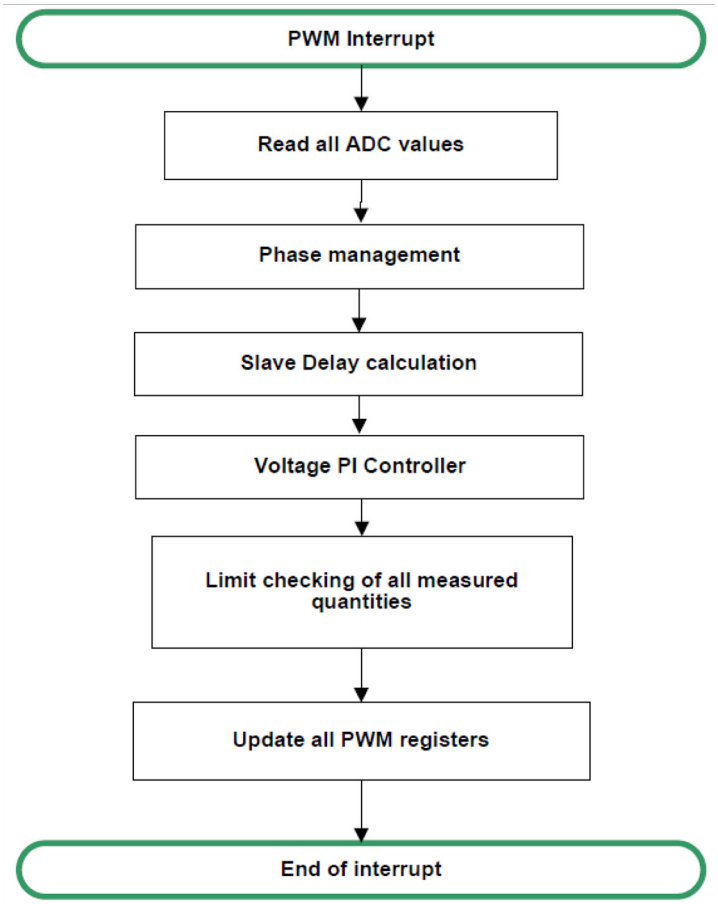


Figure 4. Slave duty cycle calculation

6 Conclusion

This application note describes implementation of a digital single-phase interleaved power factor correction that operates in boundary conduction mode. As shown, using full digital control, the PFC becomes flexible and can realize complex control arithmetic which can replace analog control and can also be implemented into other tasks such as SMPS, motor control, lighting, and more. A digital signal controller-based power factor correction system integrates high-performance digital signal processing with power electronics, providing typical high-level control. This application uses the Freescale MC56F82316 DSC to perform the power factor correction with excellent efficiency, low cost, and design flexibility. The application source code is part of this application note.

7 Revision history

Table 7-1. Revision history

Revision	Change description
0	Initial release.
1	• Substantial updates to Figure 3, minor updates to the rest of the figures. • Section Section 4.3, “System control process” replaced with new content. • Updates to QTIMER description in Section 4.4.1, “QTIMER”. • Changes to signal references and channel numbers in Section 4.4.2, “XBAR_A”. • Changes to description of PWM, additional information provided on PWM submodule 0 in Section 4.4.5, “eFlexPWM”. • Changes to sample settings in Section 4.4.6, “ADC”. • Additional state descriptions added to Section 5, “Software design”. • Control algorithm description updates in Section 5.1, “PWM reload interrupt description”.

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